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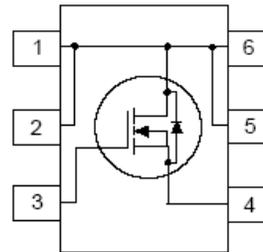
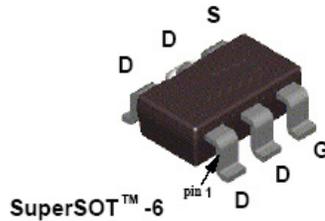
September 2015

FDC5661N_F085

N-Channel Logic Level PowerTrench[®] MOSFET 60V, 4A, 60mΩ

Features

- $R_{DS(on)} = 47m\Omega$ at $V_{GS} = 10V$, $I_D = 4.3A$
- $R_{DS(on)} = 60m\Omega$ at $V_{GS} = 4.5V$, $I_D = 4A$
- Typ $Q_{g(TOT)} = 14.5nC$ at $V_{GS} = 10V$
- Low Miller Charge
- UIS Capability
- RoHS Compliant
- Qualified to AEC Q101



Applications

- DC/DC converter
- Motor Drives

MOSFET Maximum Ratings $T_A = 25^\circ C$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain to Source Voltage	60	V
V_{GS}	Gate to Source Voltage	± 20	V
I_D	Drain Current Continuous ($V_{GS} = 10V$)	4.3	A
	Pulsed	20	
E_{AS}	Single Pulse Avalanche Energy (Note 1)	81	mJ
P_D	Power Dissipation	1.6	W
T_J, T_{STG}	Operating and Storage Temperature	-55 to +150	$^\circ C$
$R_{\theta JC}$	Thermal Resistance Junction to Case	30	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient TO-263, 1in ² copper pad area	78	$^\circ C/W$

Notes:

1: E_{AS} of 81 mJ is 100% test at $L = 14mH$, $I_{AS} = 3.4A$, starting $T_J = 25^\circ C$

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
.661N	FDC5661N	SSOT-6	7"	8mm	3000 units

FDC5661N_F085 N-Channel Logic Level PowerTrench[®] MOSFET

Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

$B_{V_{DSS}}$	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	60	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 48\text{V},$ $V_{GS} = 0\text{V}$	-	-	1	μA
		$T_A = 150^\circ\text{C}$	-	-	250	
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{V}$	-	-	± 100	nA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	1	2.0	3	V
$r_{DS(on)}$	Drain to Source On Resistance	$I_D = 4.3\text{A}, V_{GS} = 10\text{V}$	-	38	47	m Ω
		$I_D = 4\text{A}, V_{GS} = 4.5\text{V}$	-	46	60	
		$I_D = 4.3\text{A}, V_{GS} = 10\text{V}$	-	69	86	
		$T_J = 150^\circ\text{C}$	-			

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{V}, V_{GS} = 0\text{V},$ $f = 1\text{MHz}$	-	763	-	pF
C_{oss}	Output Capacitance		-	68	-	pF
C_{rss}	Reverse Transfer Capacitance		-	36	-	pF
R_G	Gate Resistance	$f = 1\text{MHz}$	-	2.6	-	Ω
$Q_{g(TOT)}$	Total Gate Charge at 10V	$V_{GS} = 0$ to 10V	-	14.5	19	nC
Q_{gs}	Gate to Source Gate Charge	$V_{DD} = 30\text{V}$ $I_D = 4.3\text{A}$	-	2.4	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		-	2.9	-	nC

Switching Characteristics

t_{on}	Turn-On Time	$V_{DD} = 30\text{V}, I_D = 4.3\text{A}$ $V_{GS} = 10\text{V}, R_{GS} = 6\Omega$	-	-	17.6	ns
$t_{d(on)}$	Turn-On Delay Time		-	7.2	-	ns
t_r	Rise Time		-	1.6	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	19.3	-	ns
t_f	Fall Time		-	3.1	-	ns
t_{off}	Turn-Off Time		-	-	36	ns

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Voltage	$I_{SD} = 4.3\text{A}$	-	0.8	1.25	V
		$I_{SD} = 2.1\text{A}$	-	0.8	1.0	
t_{rr}	Reverse Recovery Time	$I_{SD} = 4.3\text{A}, dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	18.4	24	ns
Q_{rr}	Reverse Recovery Charge		-	10.0	13	nC

Typical Characteristics

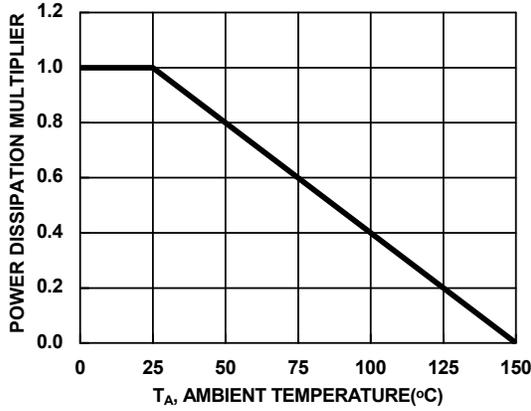


Figure 1. Normalized Power Dissipation vs Ambient Temperature

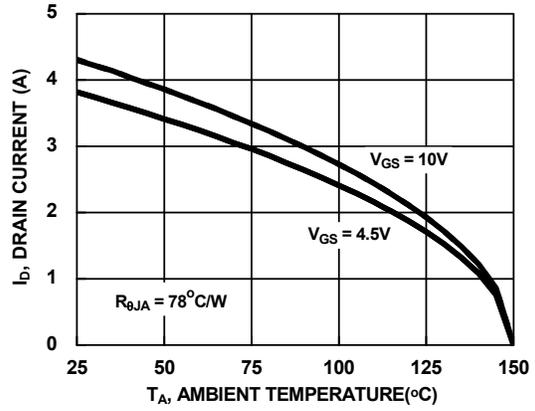


Figure 2. Maximum Continuous Drain Current vs Ambient Temperature

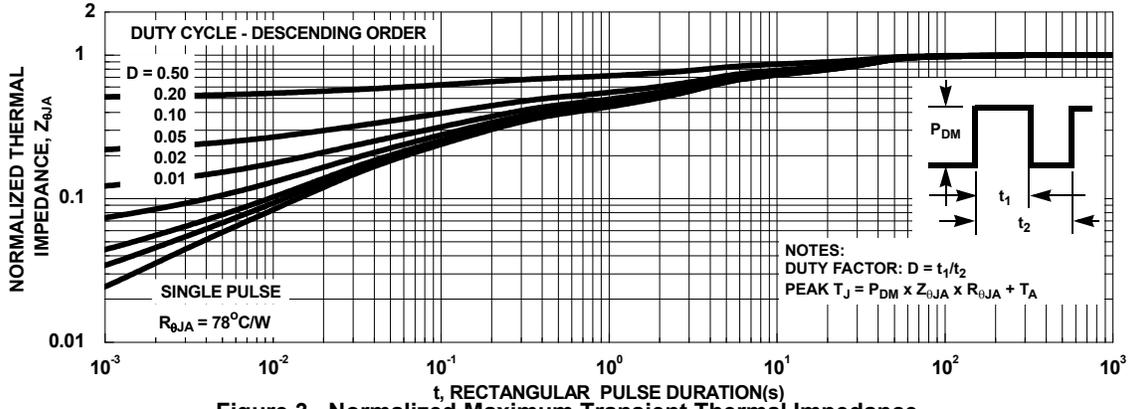


Figure 3. Normalized Maximum Transient Thermal Impedance

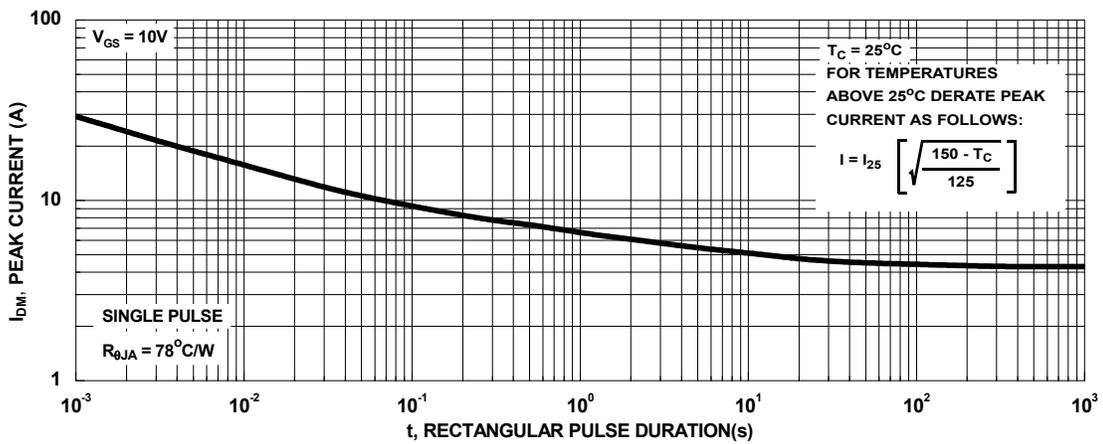


Figure 4. Peak Current Capability

Typical Characteristics

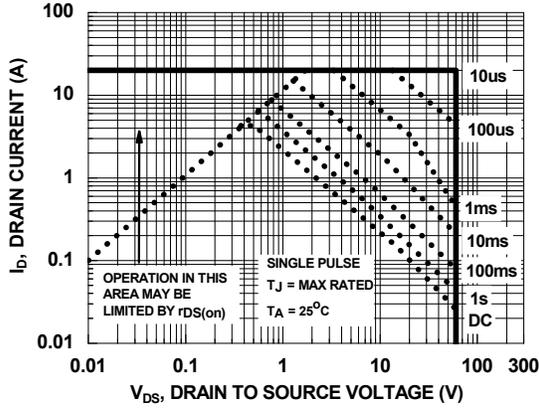


Figure 5. Forward Bias Safe Operating Area

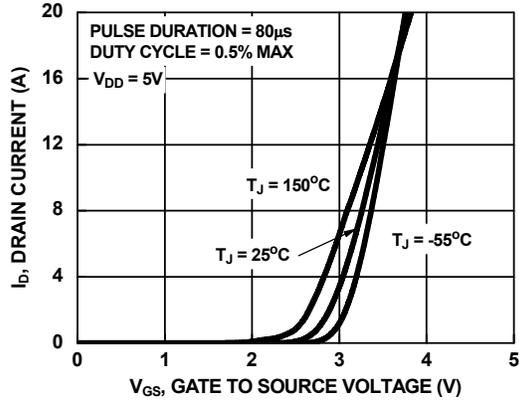


Figure 6. Transfer Characteristics

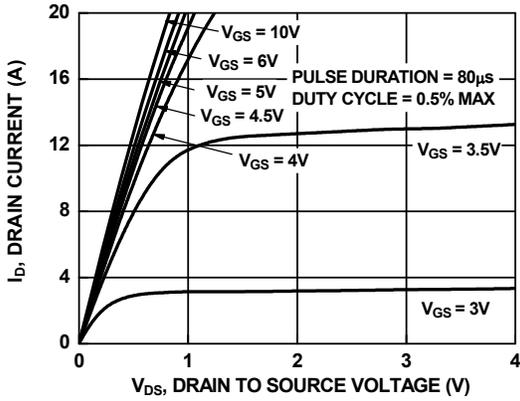


Figure 7. Saturation Characteristics

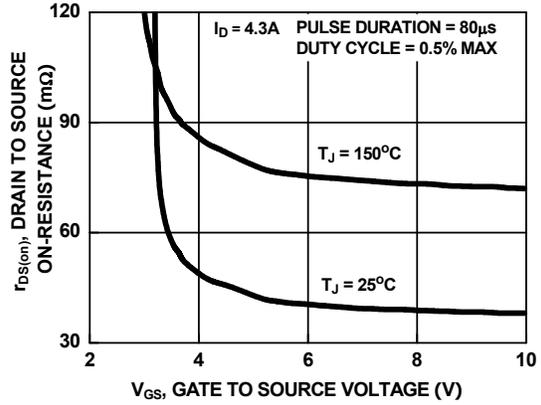


Figure 8. Drain to Source On-Resistance Variation vs Gate to Source Voltage

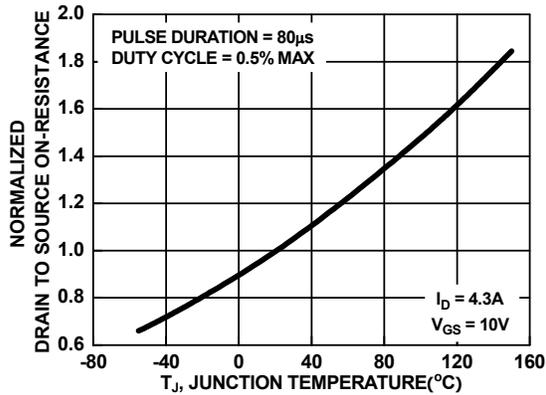


Figure 9. Normalized Drain to Source On-Resistance vs Junction Temperature

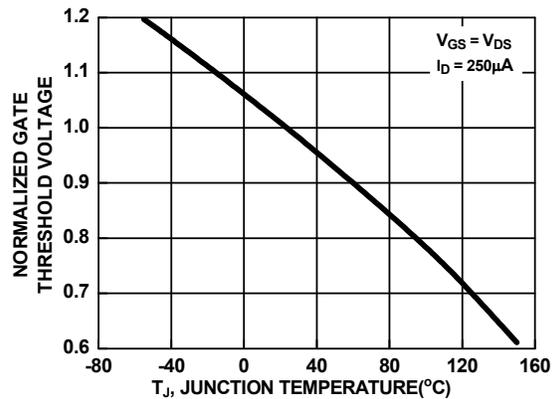


Figure 10. Normalized Gate Threshold Voltage vs Junction Temperature

Typical Characteristics

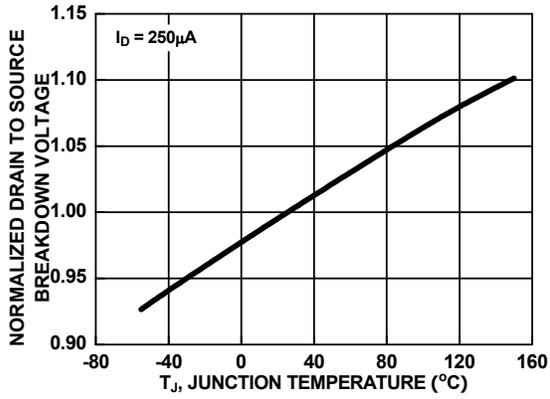


Figure 11. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

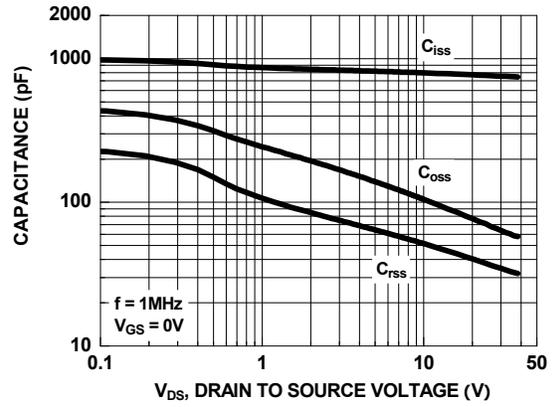


Figure 12. Capacitance vs Drain to Source Voltage

Figure 14.

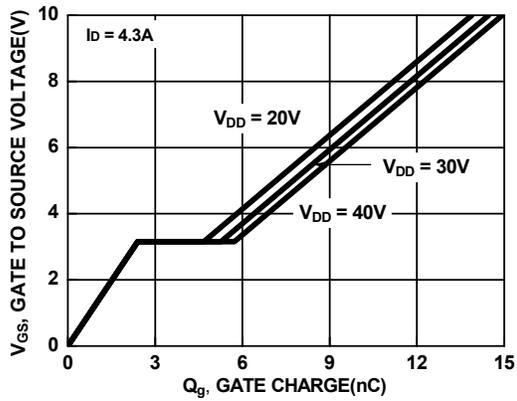
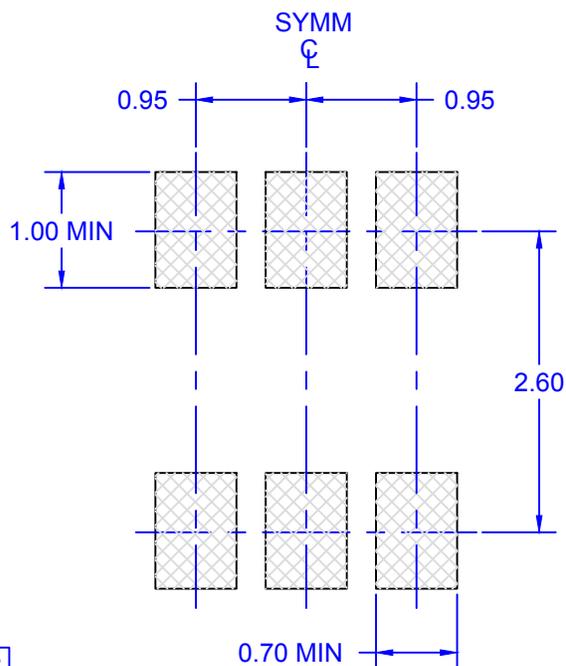
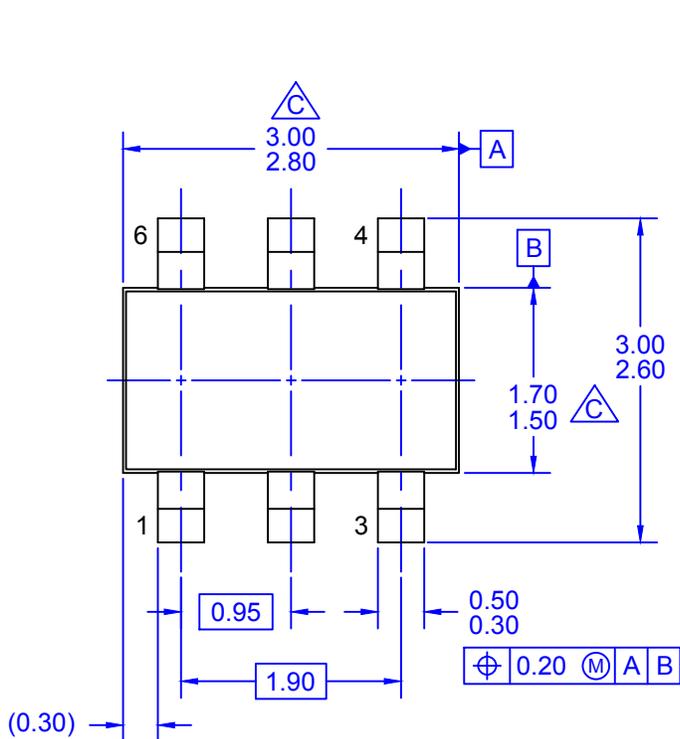
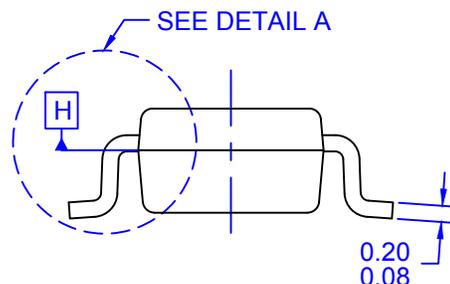
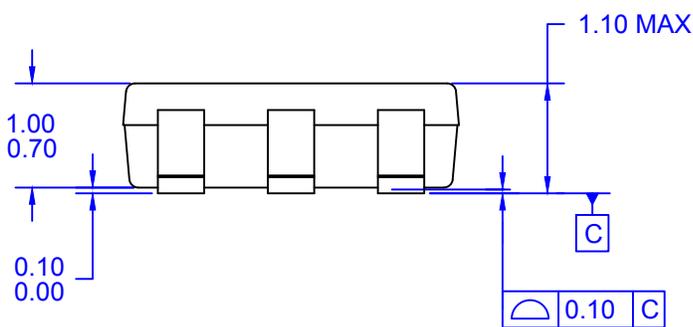


Figure 13. Gate Charge vs Gate to Source Voltage



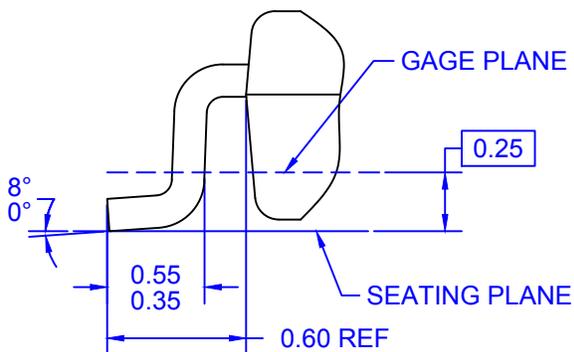
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C PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.25mm PER END. PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25mm PER SIDE. PACKAGE LENGTH AND WIDTH DIMENSIONS ARE DETERMINED AT DATUM H.

D) DRAWING FILE NAME: MKT-MA06AREVF



DETAIL A
 SCALE: 50X

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