

### BATTERY PROTECTION IC FOR 3-SERIAL-CELL PACK

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Rev.5.1\_00

The S-8233B is a series of lithium-ion rechargeable battery protection ICs incorporating high-accuracy ( $\pm 25$  mV) voltage detection circuits and delay circuits. It is suitable for a 3-serial-cell lithium-ion rechargeable battery pack.

#### ■ Features

- (1) Internal high-accuracy voltage detection circuit
  - Overcharge detection voltage  $3.80 \pm 0.025$  V to  $4.40 \pm 0.025$  V  
5 mV - step
  - Overcharge release voltage  $3.45 \pm 0.100$  V to  $4.40 \pm 0.100$  V  
5 mV - step  
(The overcharge release voltage can be selected within the range where a difference from overcharge detection voltage is 0 to 0.35 V with 50 mV - step)
  - Overdischarge detection voltage  $2.00 \pm 0.08$  V to  $2.80 \pm 0.08$  V  
50 mV - step
  - Overdischarge release voltage  $2.00 \pm 0.10$  V to  $4.00 \pm 0.10$  V  
50 mV - step  
(The overdischarge release voltage can be selected within the range where a difference from overdischarge detection voltage is 0 to 1.2 V with 50 mV - step)
  - Overcurrent detection voltage 1  $0.15 \pm 0.015$  V to  $0.5 \pm 0.05$  V  
50 mV - step
- (2) High input-voltage device (absolute maximum rating: 26 V)
- (3) Wide operating voltage range: 2 V to 24 V
- (4) The delay time for every detection can be set via an external capacitor.
- (5) Three overcurrent detection levels (protection for short-circuiting)
- (6) Internal charge/discharge prohibition circuit via the control pin
- (7) The function for charging batteries from 0 V is available.
- (8) Low current consumption
  - Operation 50  $\mu$ A max. (+25°C)
  - Power-down 0.1  $\mu$ A max. (+25°C)
- (9) Lead-free, Sn 100%, halogen-free<sup>\*1</sup>

\*1. Refer to "■ Product Name Structure" for details.

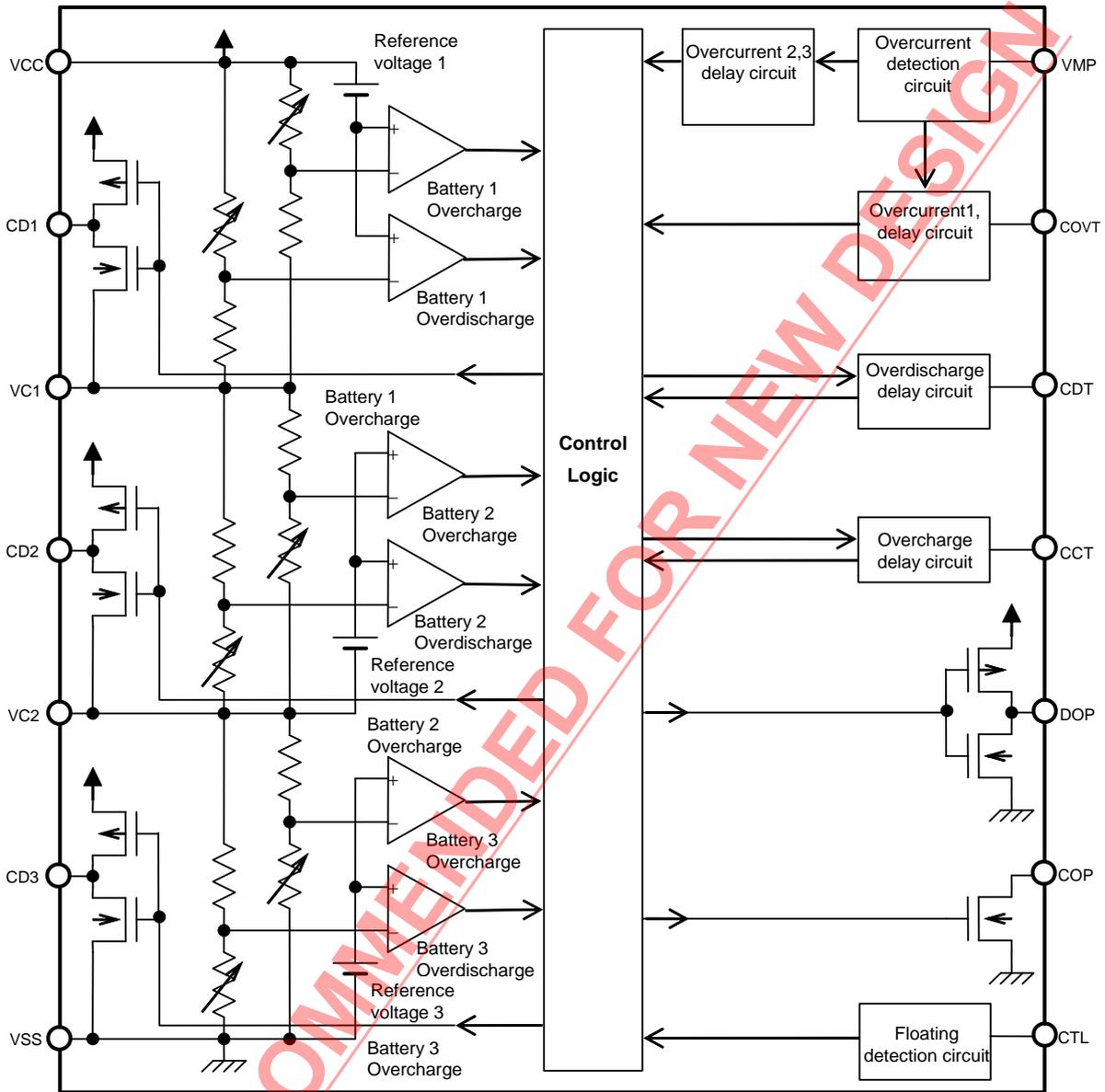
#### ■ Applications

- Lithium-ion rechargeable battery packs
- Lithium polymer rechargeable battery packs

#### ■ Package

- 16-Pin TSSOP

■ **Block Diagram**

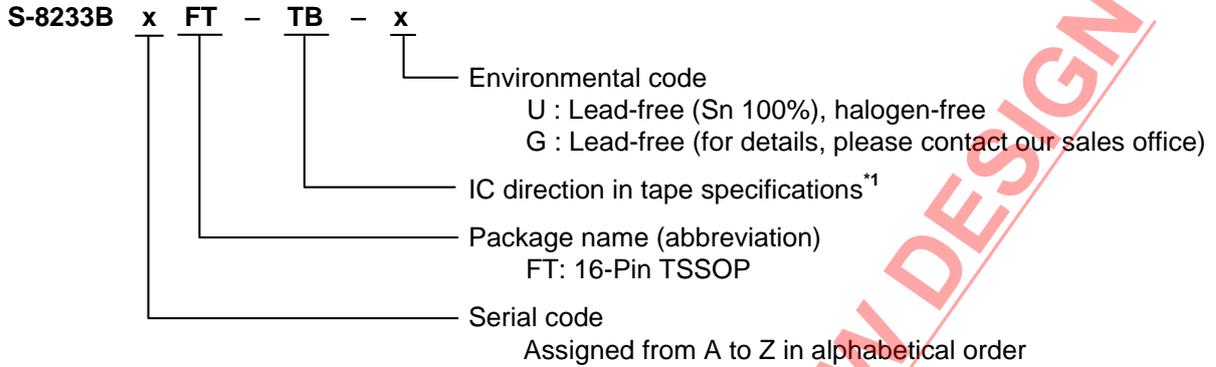


**Remark** The delay time for overcurrent detection 2 and 3 is fixed by an internal IC circuit. The delay time cannot be changed via an external capacitor.

**Figure 1**

■ **Product Name Structure**

1. **Product name**



\*1. Refer to the tape specifications.

2. **Package**

Package Name	Drawing Code		
	Package	Tape	Reel
16-Pin TSSOP	FT016-A-P-SD	FT016-A-C-SD	FT016-A-R-SD

3. **Product name list**

**Table 1**

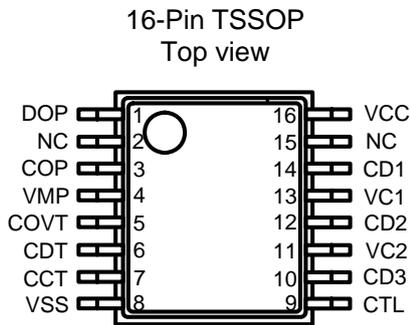
Product name / Item	Overcharge detection voltage $V_{CU}$	Overcharge release voltage $V_{CD}$	Overdischarge detection voltage $V_{DD}$	Overdischarge release voltage $V_{DU}$	Overcurrent detection voltage <sup>1</sup> $V_{IOV1}$	0V battery charging function	Conditioning function	CTL logic <sup>*1</sup>
S-8233BAFT-TB-x	4.225 V	4.225 V	2.30 V	2.70 V	0.20 V	–	Available	normal
S-8233BBFT-TB-x	4.325 V	4.150 V	2.30 V	2.70 V	0.20 V	–	Unavailable	reverse
S-8233BCFT-TB-x	4.200 V	4.200 V	2.80 V	3.30 V	0.25 V	Available	Available	normal
S-8233BDFT-TB-x	4.325 V	4.150 V	2.00 V	2.70 V	0.50 V	–	Unavailable	reverse
S-8233BEFT-TB-x	4.080 V	3.900 V	2.50 V	2.75 V	0.20 V	Available	Available	normal
S-8233BFFT-TB-U	4.200 V	4.050 V	2.40 V	2.70 V	0.30 V	Available	Available	normal

\*1. The input voltage of CTL for normal status is changed by the CTL logic. (Please refer to “**Operation**”).

**Remark 1.** Please contact our sales office for the products with the detection voltage value other than those specified above.

2. x: G or U
3. Please select products of environmental code = U for Sn 100%, halogen-free products.

■ **Pin Configuration**



**Figure 2**

**Table 2**

Pin No.	Symbol	Description
1	DOP	Connects FET gate for discharge control (CMOS output)
2	NC	Non connect <sup>*1</sup>
3	COP	Connects FET gate for charge control (Nch open-drain output)
4	VMP	Detects voltage between VCC to VMP (Overcurrent detection pin)
5	COVT	Connects capacitor for overcurrent detection delay circuit
6	CDT	Connects capacitor for overdischarge detection delay circuit
7	CCT	Connects capacitor for overcharge detection delay circuit
8	VSS	Negative power input, and connects negative voltage for battery 3
9	CTL	Charge/discharge control signal input
10	CD3	Battery 3 conditioning signal output
11	VC2	Connects battery 2 negative voltage and battery 3 positive voltage
12	CD2	Battery 2 conditioning signal output
13	VC1	Connects battery 1 negative voltage and battery 2 positive voltage
14	CD1	Battery 1 conditioning signal output
15	NC	Non connect <sup>*1</sup>
16	VCC	Positive power input and connects battery 1 positive voltage

\*1. The NC pin is electrically open. The NC pin can be connected to VCC or VSS.

NOT RECOMMENDED FOR NEW DESIGN

■ **Absolute Maximum Ratings**

**Table 3**

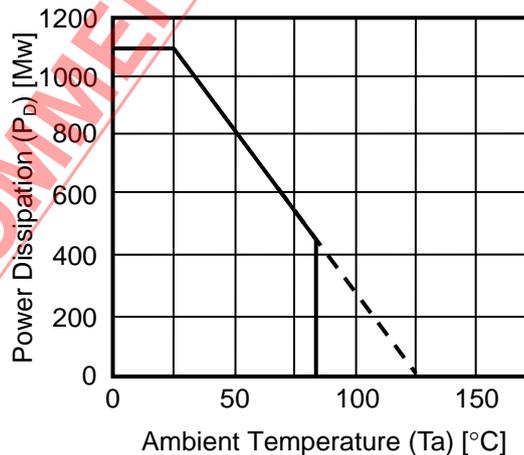
(Ta = 25°C unless otherwise specified)

Item	Symbol	Applied Pins	Absolute Maximum Ratings	Unit
Input voltage between VCC and VSS	V <sub>DS</sub>	-	V <sub>SS</sub> -0.3 to V <sub>SS</sub> +26	V
Input pin voltage	V <sub>IN</sub>	VC1, VC2, CTL, CCT, CDT, COVT	V <sub>SS</sub> -0.3 to V <sub>CC</sub> +0.3	V
VMP Input pin voltage	V <sub>VMP</sub>	VMP	V <sub>SS</sub> -0.3 to V <sub>SS</sub> +26	V
CD1 output pin voltage	V <sub>CD1</sub>	CD1	V <sub>C1</sub> -0.3 to V <sub>CC</sub> +0.3	V
CD2 output pin voltage	V <sub>CD2</sub>	CD2	V <sub>C2</sub> -0.3 to V <sub>CC</sub> +0.3	V
CD3 output pin voltage	V <sub>CD3</sub>	CD3	V <sub>SS</sub> -0.3 to V <sub>CC</sub> +0.3	V
DOP output pin voltage	V <sub>DOP</sub>	DOP	V <sub>SS</sub> -0.3 to V <sub>CC</sub> +0.3	V
COP output pin voltage	V <sub>COP</sub>	COP	V <sub>SS</sub> -0.3 to V <sub>VMP</sub> +0.3	V
Power dissipation	P <sub>D</sub>	-	300 (When not mounted on board)	mW
		-	1100*1	mW
Operating ambient temperature	T <sub>opr</sub>	-	-20 to +70	°C
Storage temperature	T <sub>stg</sub>	-	-40 to +125	°C

\*1. When mounted on board  
 [Mounted board]

- (1) Board size : 114.3 mm × 76.2 mm × t1.6 mm
- (2) Board name : JEDEC STANDARD51-7

**Caution** The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.



**Figure 3 Power Dissipation of Package (When Mounted on Board)**

■ **Electrical Characteristics**

**Table 4 (1 / 2)**

(Ta = 25°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test condition	Test circuit
<b>Detection voltage</b>								
Overcharge detection voltage 1	V <sub>CU1</sub>	3.80 to 4.40 Adjustment	V <sub>CU1</sub> -0.025	V <sub>CU1</sub>	V <sub>CU1</sub> +0.025	V	1	1
Overcharge release voltage 1	V <sub>CD1</sub>	3.45 to 4.40 Adjustment	V <sub>CD1</sub> -0.10	V <sub>CD1</sub>	V <sub>CD1</sub> +0.10	V	1	1
Overdischarge detection voltage 1	V <sub>DD1</sub>	2.00 to 2.80 Adjustment	V <sub>DD1</sub> -0.08	V <sub>DD1</sub>	V <sub>DD1</sub> +0.08	V	1	1
Overdischarge release voltage 1	V <sub>DU1</sub>	2.00 to 4.00 Adjustment	V <sub>DU1</sub> -0.10	V <sub>DU1</sub>	V <sub>DU1</sub> +0.10	V	1	1
Overcharge detection voltage 2	V <sub>CU2</sub>	3.80 to 4.40 Adjustment	V <sub>CU2</sub> -0.025	V <sub>CU2</sub>	V <sub>CU2</sub> +0.025	V	2	1
Overcharge release voltage 2	V <sub>CD2</sub>	3.45 to 4.40 Adjustment	V <sub>CD2</sub> -0.10	V <sub>CD2</sub>	V <sub>CD2</sub> +0.10	V	2	1
Overdischarge detection voltage 2	V <sub>DD2</sub>	2.00 to 2.80 Adjustment	V <sub>DD2</sub> -0.08	V <sub>DD2</sub>	V <sub>DD2</sub> +0.08	V	2	1
Overdischarge release voltage 2	V <sub>DU2</sub>	2.00 to 4.00 Adjustment	V <sub>DU2</sub> -0.10	V <sub>DU2</sub>	V <sub>DU2</sub> +0.10	V	2	1
Overcharge detection voltage 3	V <sub>CU3</sub>	3.80 to 4.40 Adjustment	V <sub>CU3</sub> -0.025	V <sub>CU3</sub>	V <sub>CU3</sub> +0.025	V	3	1
Overcharge release voltage 3	V <sub>CD3</sub>	3.45 to 4.40 Adjustment	V <sub>CD3</sub> -0.10	V <sub>CD3</sub>	V <sub>CD3</sub> +0.10	V	3	1
Overdischarge detection voltage 3	V <sub>DD3</sub>	2.00 to 2.80 Adjustment	V <sub>DD3</sub> -0.08	V <sub>DD3</sub>	V <sub>DD3</sub> +0.08	V	3	1
Overdischarge release voltage 3	V <sub>DU3</sub>	2.00 to 4.00 Adjustment	V <sub>DU3</sub> -0.10	V <sub>DU3</sub>	V <sub>DU3</sub> +0.10	V	3	1
Overcurrent detection voltage 1 <sup>1</sup>	V <sub>IOV1</sub>	0.15 to 0.50V Adjustment	V <sub>IOV1</sub> ×0.9	V <sub>IOV1</sub>	V <sub>IOV1</sub> ×1.1	V	4	2
Overcurrent detection voltage 2	V <sub>IOV2</sub>	V <sub>CC</sub> Reference	0.54	0.6	0.66	V	4	2
Overcurrent detection voltage 3	V <sub>IOV3</sub>	V <sub>SS</sub> Reference	1.0	2.0	3.0	V	4	2
Voltage temperature factor 1 <sup>2</sup>	T <sub>COE1</sub>	Ta = -20 to 70°C <sup>4</sup>	-1.0	0	1.0	mV/°C	-	-
Voltage temperature factor 2 <sup>3</sup>	T <sub>COE2</sub>	Ta = -20 to 70°C <sup>4</sup>	-0.5	0	0.5	mV/°C	-	-
<b>Delay time</b>								
Overcharge detection delay time 1	t <sub>CU1</sub>	C <sub>CCT</sub> = 0.47 μF	0.5	1.0	1.5	s	9	6
Overcharge detection delay time 2	t <sub>CU2</sub>	C <sub>CCT</sub> = 0.47 μF	0.5	1.0	1.5	s	10	6
Overcharge detection delay time 3	t <sub>CU3</sub>	C <sub>CCT</sub> = 0.47 μF	0.5	1.0	1.5	s	11	6
Overdischarge detection delay time 1	t <sub>DD1</sub>	C <sub>CDT</sub> = 0.1 μF	20	40	60	ms	9	6
Overdischarge detection delay time 2	t <sub>DD2</sub>	C <sub>CDT</sub> = 0.1 μF	20	40	60	ms	10	6
Overdischarge detection delay time 3	t <sub>DD3</sub>	C <sub>CDT</sub> = 0.1 μF	20	40	60	ms	11	6
Overcurrent detection delay time 1	t <sub>IOV1</sub>	C <sub>COVT</sub> = 0.1 μF	10	20	30	ms	12	7
Overcurrent detection delay time 2	t <sub>IOV2</sub>	-	2	4	8	ms	12	7
Overcurrent detection delay time 3	t <sub>IOV3</sub>	FET gate capacitor = 2000 pF	100	300	550	μs	12	7
<b>Operating voltage</b>								
Operating voltage between VCC and VSS <sup>5</sup>	V <sub>D50P</sub>	-	2.0	-	24	V	-	-
<b>Current consumption</b>								
Current consumption (during normal operation)	I <sub>OPe</sub>	V1 = V2 = V3 = 3.5 V	-	20	50	μA	5	3
Current consumption for cell 1	I <sub>CELL1</sub>	V1 = V2 = V3 = 3.5 V	-300	0	300	nA	5	3
Current consumption for cell 2	I <sub>CELL2</sub>	V1 = V2 = V3 = 3.5 V	-300	0	300	nA	5	3
Current consumption for cell 3	I <sub>CELL3</sub>	V1 = V2 = V3 = 3.5 V	-300	0	300	nA	5	3
Current consumption at power down	I <sub>PdN</sub>	V1 = V2 = V3 = 1.5 V	-	-	0.1	μA	5	3
<b>Internal resistance with 0V battery charging function type</b>								
Resistance between VCC and VMP	R <sub>VCM</sub>	V1 = V2 = V3 = 3.5 V	0.20	0.50	0.80	MΩ	6	3
Resistance between VSS and VMP	R <sub>VSM</sub>	V1 = V2 = V3 = 1.5 V	0.20	0.50	0.80	MΩ	6	3
<b>Internal resistance without 0V battery charging function type</b>								
Resistance between VCC and VMP	R <sub>VCM</sub>	V1 = V2 = V3 = 3.5 V	0.40	0.90	1.40	MΩ	6	3
Resistance between VSS and VMP	R <sub>VSM</sub>	V1 = V2 = V3 = 1.5 V	0.40	0.90	1.40	MΩ	6	3
<b>Input voltage</b>								
CTL"H" Input voltage	V <sub>CTL(H)</sub>	-	V <sub>CC</sub> × 0.8	-	-	V	16	1
CTL"L" Input voltage	V <sub>CTL(L)</sub>	-	-	-	V <sub>CC</sub> × 0.2	V	16	1

**BATTERY PROTECTION IC FOR 3-SERIAL-CELL PACK  
S-8233B Series**

Rev.5.1\_00

**Table 4 (2 / 2)**

(Ta = 25 °C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test condition	Test circuit
<b>Output voltage</b>								
DOP"H" voltage	V <sub>DO(H)</sub>	I <sub>OUT</sub> = 10 μA	V <sub>CC</sub> -0.5	-	-	V	7	4
DOP"L" voltage	V <sub>DO(L)</sub>	I <sub>OUT</sub> = 10 μA	-	-	V <sub>SS</sub> +0.1	V	7	4
COP"L" voltage	V <sub>CO(L)</sub>	I <sub>OUT</sub> = 10 μA	-	-	V <sub>SS</sub> +0.1	V	8	5
COP OFF LEAK current	I <sub>COL</sub>	V1 = V2 = V3 = 4.5 V	-	-	100	nA	14	9
CD1"H" voltage	V <sub>CD1(H)</sub>	I <sub>OUT</sub> = 0.1 μA	V <sub>CC</sub> -0.5	-	-	V	13	8
CD1"L" voltage	V <sub>CD1(L)</sub>	I <sub>OUT</sub> = 10 μA	-	-	V <sub>C1</sub> +0.1	V	13	8
CD2"H" voltage	V <sub>CD2(H)</sub>	I <sub>OUT</sub> = 0.1 μA	V <sub>CC</sub> -0.5	-	-	V	13	8
CD2"L" voltage	V <sub>CD2(L)</sub>	I <sub>OUT</sub> = 10 μA	-	-	V <sub>C2</sub> +0.1	V	13	8
CD3"H" voltage	V <sub>CD3(H)</sub>	I <sub>OUT</sub> = 0.1 μA	V <sub>CC</sub> -0.5	-	-	V	13	8
CD3"L" voltage	V <sub>CD3(L)</sub>	I <sub>OUT</sub> = 10 μA	-	-	V <sub>SS</sub> +0.1	V	13	8
<b>0V battery charging function<sup>*6</sup></b>								
0V charging start voltage	V <sub>0CHAR</sub>	V1 = V2 = V3 = 0 V	-	-	1.4	V	15	10

- \*1. If overcurrent detection voltage 1 is 0.50 V, both overcurrent detection voltages 1 and 2 are 0.54 to 0.55 V, but V<sub>IOV2</sub> > V<sub>IOV1</sub>.
- \*2. Voltage temperature factor 1 indicates overcharge detection voltage, overcharge release voltage, overdischarge detection voltage, and overdischarge release voltage.
- \*3. Voltage temperature factor 2 indicates overcurrent detection voltage.
- \*4. Since products are not screened at high and low temperature, the specification for this temperature range is guaranteed by design, not tested in production.
- \*5. The DOP and COP logic must be established for the operating voltage.
- \*6. This spec applies for only 0 V battery charging function available type.

## ■ Test Circuits

**Caution** At the Test circuit from (1) to (16).

If the device's CTL logic is "normal" (S-8233BA, S-8233BC, S-8233BE, S-8233BF) then set the CTL voltage at  $V_{SS}$  ( $V4 = 0V$ ).

If the device's CTL logic is "reverse" (S-8233BB, S-8233BD) then set the CTL voltage at  $V_{CC}$  ( $V4 = V1+V2+V3$ ).

### (1) Test condition 1 Test circuit 1

Set  $V1$ ,  $V2$ , and  $V3$  to 3.5 V under normal status. Increase  $V1$  from 3.5 V gradually. The  $V1$  voltage when COP = 'H' is overcharge detection voltage 1 ( $V_{CU1}$ ). Decrease  $V1$  gradually. The  $V1$  voltage when COP = 'L' is overcharge release voltage 1 ( $V_{CD1}$ ). Further decrease  $V1$ . The  $V1$  voltage when DOP = 'H' is overdischarge voltage 1 ( $V_{DD1}$ ). Increase  $V1$  gradually. The  $V1$  voltage when DOP = 'L' is overdischarge release voltage 1 ( $V_{DU1}$ ).

**Remark** The voltage change rate is 150 V/s or less.

### (2) Test condition 2 Test circuit 1

Set  $V1$ ,  $V2$ , and  $V3$  to 3.5 V under normal status. Increase  $V2$  from 3.5 V gradually. The  $V2$  voltage when COP = 'H' is overcharge detection voltage 2 ( $V_{CU2}$ ). Decrease  $V2$  gradually. The  $V2$  voltage when COP = 'L' is overcharge release voltage 2 ( $V_{CD2}$ ). Further decrease  $V2$ . The  $V2$  voltage when DOP = 'H' is overdischarge voltage 2 ( $V_{DD2}$ ). Increase  $V2$  gradually. The  $V2$  voltage when DOP = 'L' is overdischarge release voltage 2 ( $V_{DU2}$ ).

**Remark** The voltage change rate is 150 V/s or less.

### (3) Test condition 3 Test circuit 1

Set  $V1$ ,  $V2$ , and  $V3$  to 3.5 V under normal status. Increase  $V3$  from 3.5 V gradually. The  $V3$  voltage when COP = 'H' is overcharge detection voltage 3 ( $V_{CU3}$ ). Decrease  $V3$  gradually. The  $V3$  voltage when COP = 'L' is overcharge release voltage 3 ( $V_{CD3}$ ). Further decrease  $V3$ . The  $V3$  voltage when DOP = 'H' is overdischarge voltage 3 ( $V_{DD3}$ ). Increase  $V3$  gradually. The  $V3$  voltage when DOP = 'L' is overdischarge release voltage 3 ( $V_{DU3}$ ).

**Remark** The voltage change rate is 150 V/s or less.

### (4) Test condition 4 Test circuit 2

Set  $V1$ ,  $V2$ ,  $V3$  to 3.5 V and  $V5$  to 0 V under normal status. Increase  $V5$  from 0 V gradually. The  $V5$  voltage when DOP = 'H' and COP = 'H', is overcurrent detection voltage 1 ( $V_{IOV1}$ ).

Set  $V1$ ,  $V2$ , and  $V3$  to 3.5 V and  $V5$  to 0 V under normal status. Fix the COVT pin at  $V_{SS}$ , increase  $V5$  from 0 V gradually. The  $V5$  voltage when DOP = 'H' and COP = 'H' is overcurrent detection voltage 2 ( $V_{IOV2}$ ).

Set  $V1$ ,  $V2$ , and  $V3$  to 3.5 V and  $V5$  to 0 V under normal status. Fix the COVT pin at  $V_{SS}$ , increase  $V5$  gradually from 0 V at 400  $\mu$ s to 2 ms. The  $V5$  voltage when DOP = 'H' and COP = 'H' is overcurrent detection voltage 3 ( $V_{IOV3}$ ).

### (5) Test condition 5 Test circuit 3

Set S1 to ON,  $V1$ ,  $V2$ , and  $V3$  to 3.5 V, and  $V5$  to 0 V under normal status and measure current consumption. I1 is the normal status current consumption ( $I_{OPE}$ ), I2, the cell 2 current consumption ( $I_{CELL2}$ ), and I3, the cell 3 current consumption ( $I_{CELL3}$ ).

Set S1 to ON,  $V1$ ,  $V2$ , and  $V3$  to 1.5 V, and  $V5$  to 4.5 V under overdischarge status. Current consumption I1 is power-down current consumption ( $I_{PDN}$ ).

**(6) Test condition 6 Test circuit 3**

Set S1 to ON, V1, V2, and V3 to 3.5 V, and V5 to 10.5 V under normal status.  $V5/I5$  is the internal resistance between VCC and VMP ( $R_{VCM}$ ).

Set S1 to ON, V1, V2, and V3 to 1.5 V, and V5 to 4.1 V under overdischarge status.  $(4.5-V5)/I5$  is the internal resistance between VSS and VMP ( $R_{VCM}$ ).

**(7) Test condition 7 Test circuit 4**

Set S1 to ON, S2 to OFF, V1, V2, and V3 to 3.5 V, and V5 to 0 V under normal status. Increase V6 from 0 V gradually. The V6 voltage when  $I6 = 10 \mu\text{A}$  is DOP'L' voltage ( $V_{DO(L)}$ ).

Set S1 to OFF, S2 to ON, V1, V2, V3 to 3.5 V, and V5 to  $V_{IOV2}+0.1$  V under overcurrent status. Increase V7 from 0 V gradually. The V7 voltage when  $I7 = 10 \mu\text{A}$  is the DOP'H' voltage ( $V_{DO(H)}$ ).

**(8) Test condition 8 Test circuit 5**

Set V1, V2, V3 to 3.5 V and V5 to 0 V under normal status. Increase V6 from 0 V gradually. The V6 voltage when  $I1 = 10 \mu\text{A}$  is the COP'L' voltage ( $V_{C0(L)}$ ).

**(9) Test condition 9 Test circuit 6**

Set V1, V2, V3 to 3.5 V under normal status. Increase V1 from 3.5 V to 4.5 V immediately (within 10  $\mu\text{s}$ ). The time after V1 becomes 4.5 V until COP goes 'H' is the overcharge detection delay time 1 ( $t_{CU1}$ ).

Set V1, V2, V3 to 3.5 V under normal status. Decrease V1 from 3.5 V to 1.9 V immediately (within 10  $\mu\text{s}$ ). The time after V1 becomes 1.9 V until DOP goes 'H' is the overdischarge detection delay time 1 ( $t_{DD1}$ ).

**(10) Test condition 10 Test circuit 6**

Set V1, V2, V3 to 3.5 V under normal status. Increase V2 from 3.5 V to 4.5 V immediately (within 10  $\mu\text{s}$ ). The time after V2 becomes 4.5 V until COP goes 'H' is the overcharge detection delay time 2 ( $t_{CU2}$ ).

Set V1, V2, V3 to 3.5 V under normal status. Decrease V2 from 3.5 V to 1.9 V immediately (within 10  $\mu\text{s}$ ). The time after V2 becomes 1.9 V until DOP goes 'H' is the overdischarge detection delay time 2 ( $t_{DD2}$ ).

**(11) Test condition 11 Test circuit 6**

Set V1, V2, V3 to 3.5 V under normal status. Increase V3 from 3.5 V to 4.5 V immediately (within 10  $\mu\text{s}$ ). The time after V3 becomes 4.5 V until COP goes 'H' is the overcharge detection delay time 3 ( $t_{CU3}$ ).

Set V1, V2, V3 to 3.5 V under normal status. Decrease V3 from 3.5 V to 1.9 V immediately (within 10  $\mu\text{s}$ ). The time after V3 becomes 1.9 V until DOP goes 'H' is the overdischarge detection delay time 3 ( $t_{DD3}$ ).

**(12) Test condition 12 Test circuit 7**

Set V1, V2, V3 to 3.5 V and S1 to OFF under normal status. Increase V5 from 0 V to 0.55 V immediately (within 10  $\mu\text{s}$ ). The time after V5 becomes 0.55 V until DOP goes 'H' is the overcurrent detection delay time 1 ( $t_{IOV1}$ ).

Set V1, V2, V3 to 3.5 V and S1 to OFF under normal status. Increase V5 from 0 V to 0.75 V immediately (within 10  $\mu\text{s}$ ). The time after V4 becomes 0.75 V until DOP goes 'H' is the overcurrent detection delay time 2 ( $t_{IOV2}$ ).

Set S1 to ON to inhibit overdischarge detection. Set V1, V2, V3 to 4.0 V and increase V5 from 0 V to 6.0 V immediately (within 1  $\mu\text{s}$ ) and decrease V1, V2, and V3 to 2.0 V at a time. The time after V5 becomes 6.0 V until DOP goes 'H' is the overcurrent detection delay time 3 ( $t_{IOV3}$ ).

**(13) Test condition 13 Test circuit 8**

Set S4 to ON, S1, S2, S3, S5, and S6 to OFF, V1, V2, V3 to 3.5 V and V6, V7, and V8 to 0 V under normal status. Increase V5 from 0 V gradually. The V5 voltage when  $I_5 = 10 \mu\text{A}$  is the CD1'L' voltage ( $V_{\text{CD1(L)}}$ ).

Set S5 to ON, S1, S2, S3, S4, and S6 to OFF, V1, V2, and V3 to 3.5 V and V5, V7, and V8 to 0 V under normal status. Increase V6 from 0 V gradually. The V6 voltage when  $I_6 = 10 \mu\text{A}$  is the CD2'L' voltage ( $V_{\text{CD2(L)}}$ ).

Set S6 to ON, S1, S2, S3, S4, and S5 to OFF, V1, V2, and V3 to 3.5 V and V5, V6, and V8 to 0 V under normal status. Increase V7 from 0 V gradually. The V7 voltage when  $I_7 = 10 \mu\text{A}$  is the CD3'L' voltage ( $V_{\text{CD3(L)}}$ ).

Set S1 to ON, S2, S3, S4, S5, and S6 to OFF, V1 to 4.5 V, V2 and V3 to 3.5 V and V5, V6, and V7 to 0 V under overcharge status. Increase V8 from 0 V gradually. The V8 voltage when  $I_8 = 0.1 \mu\text{A}$  is the CD1'H' voltage ( $V_{\text{CD1(H)}}$ ).

Set S2 to ON, S1, S3, S4, S5, and S6 to OFF, V2 to 4.5 V, V1 and V3 to 3.5 V and V5, V6, and V7 to 0 V under overcharge status. Increase V4 from 0 V gradually. The V4 voltage when  $I_1 = 0.1 \mu\text{A}$  is the CD2'H' voltage ( $V_{\text{CD2(H)}}$ ).

Set S3 to ON, S1, S2, S4, S5, and S6 to OFF, V3 to 4.5 V, V1 and V2 to 3.5 V and V5, V6, and V7 to 0 V under overcharge status. Increase V8 from 0 V gradually. The V8 voltage when  $I_8 = 0.1 \mu\text{A}$  is the CD3'H' voltage ( $V_{\text{CD3(H)}}$ ).

**(14) Test condition 14 Test circuit 9**

Set V1, V2, and V3 to 4.5 V under overcharge status. The current  $I_1$  flowing to COP pin is COP OFF LEAK current ( $I_{\text{COL}}$ ).

**(15) Test condition 15 Test circuit 10**

Set V1, V2, and V3 to 0 V, and V5 to 2 V, and decrease V5 gradually. The V5 voltage when COP = 'H' ( $V_{\text{SS}} + 0.3 \text{ V}$  or higher) is the 0 V charge start voltage ( $V_{\text{OCHAR}}$ ).

**(16) Test condition 16 Test circuit 1**

**Test condition will be changed by the CTL logic**

<1> **If the CTL logic is "normal"**

Set V1, V2, and V3 to 3.5 V, and V4 to 0 V, and increase V4 gradually. The V4 voltage when COP = 'H' ( $V_{\text{SS}} + 0.3 \text{ V}$  or higher) and DOP = 'H' ( $V_{\text{SS}} + 0.3 \text{ V}$  or higher) is the CTL 'H' input voltage ( $V_{\text{CTL(H)}}$ ).

After that decrease V4 gradually. The V4 voltage when COP = 'L' ( $V_{\text{CC}} - 0.3 \text{ V}$  or lower) and DOP = 'L' ( $V_{\text{CC}} - 0.3 \text{ V}$  or lower) is the CTL'L' input voltage ( $V_{\text{CTL(L)}}$ ).

<2> **If the CTL logic is "reverse"**

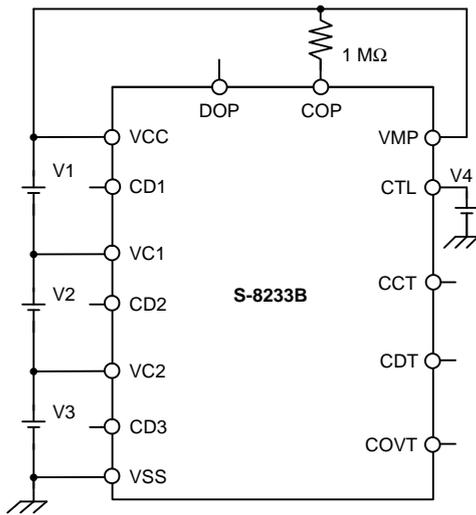
Set V1, V2, and V3 to 3.5 V, and V4 to 10.5 V, and decrease V4 gradually. The V4 voltage when COP = 'H' ( $V_{\text{SS}} + 0.3 \text{ V}$  or higher) and DOP = 'H' ( $V_{\text{SS}} + 0.3 \text{ V}$  or higher) is the CTL'L' input voltage ( $V_{\text{CTL(L)}}$ ).

After that increase V4 gradually. The V4 voltage when COP = 'L' ( $V_{\text{VMP}} - 0.3 \text{ V}$  or lower) and DOP = 'L' ( $V_{\text{CC}} - 0.3 \text{ V}$  or lower) is the CTL'H' input voltage ( $V_{\text{CTL(H)}}$ ).

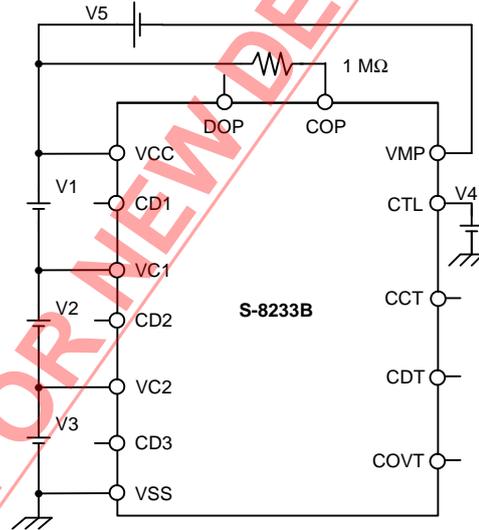
**Caution** At the Test circuit from 1 to 10.

If the device's CTL logic is "normal" (S-8233BA, S-8233BC, S-8233BE, S-8233BF) then set the CTL voltage at  $V_{SS}$  ( $V4 = 0\text{ V}$ ).

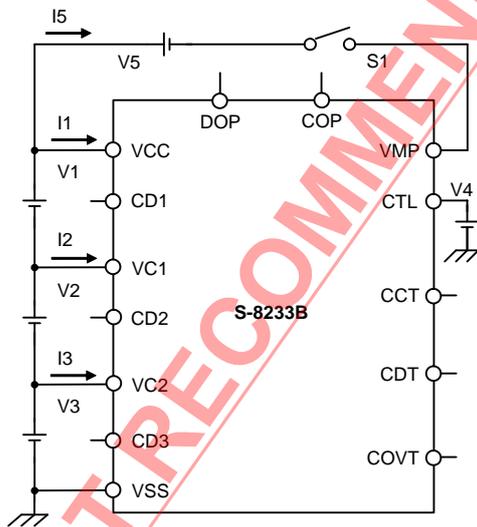
If the device's CTL logic is "reverse" (S-8233BB, S-8233BD) then set the CTL voltage at  $V_{CC}$  ( $V4 = V1+V2+V3$ ).



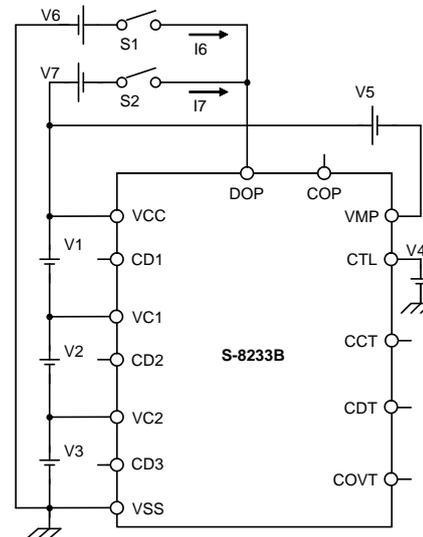
Test circuit 1



Test circuit 2

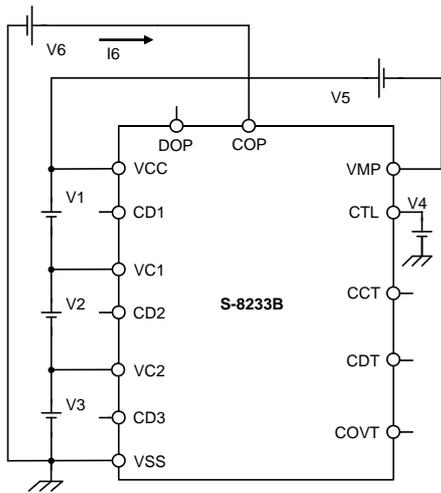


Test circuit 3

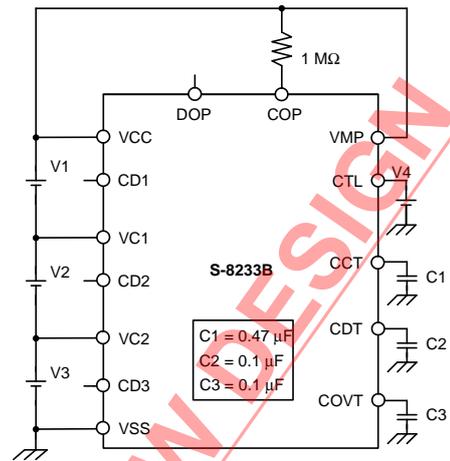


Test circuit 4

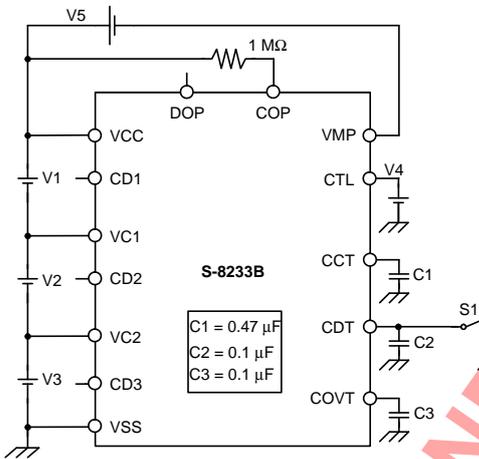
Figure 4 (1 / 2)



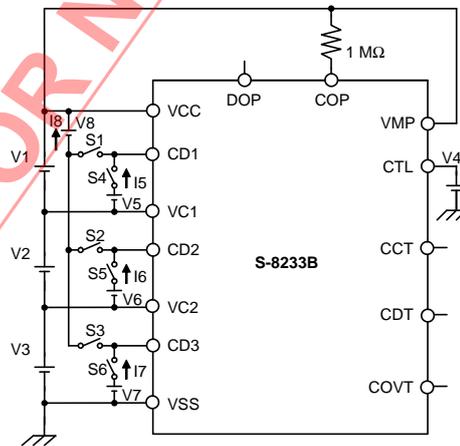
**Test circuit 5**



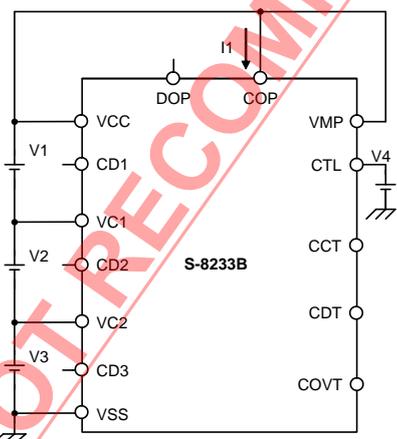
**Test circuit 6**



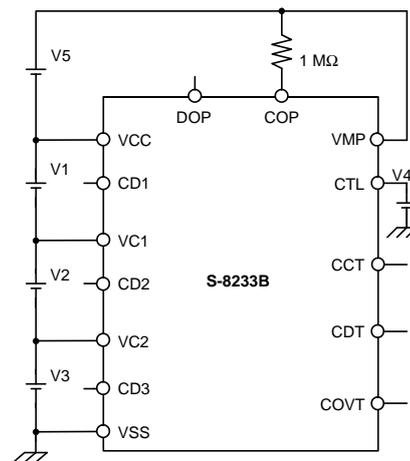
**Test circuit 7**



**Test circuit 8**



**Test circuit 9**



**Test circuit 10**

**Figure 4 (2 / 2)**

## ■ Operation

**Remark** Refer to “**Battery Protection IC Connection Example**”.

### Normal status

This IC monitors the voltages of the three serially-connected batteries and the discharge current to control charging and discharging. If the voltages of all the three batteries are in the range from the overdischarge detection voltage ( $V_{DD}$ ) to the overcharge detection voltage ( $V_{CU}$ ), and the current flowing through the batteries becomes equal or lower than a specified value (the VMP pin voltage is equal or lower than overcurrent detection voltage 1), the charging and discharging FETs turn on. In this status, charging and discharging can be carried out freely. This status is called the normal status. In this status, the VMP and VCC pins are shorted by the  $R_{VCM}$  resistor.

### Overcurrent status

This IC is provided with the three overcurrent detection levels ( $V_{IOV1}$ ,  $V_{IOV2}$  and  $V_{IOV3}$ ) and the three overcurrent detection delay time ( $t_{IOV1}$ ,  $t_{IOV2}$  and  $t_{IOV3}$ ) corresponding to each overcurrent detection level.

If the discharging current becomes equal to or higher than a specified value (the VMP pin voltage is equal to or higher than the overcurrent detection voltage) during discharging under normal status and it continues for the overcurrent detection delay time ( $t_{IOV}$ ) or longer, the discharging FET turns off to stop discharging. This status is called an overcurrent status. The VMP and VCC pins are shorted by the  $R_{VCM}$  resistor at this time. The charging FET turns off.

When the discharging FET is off and a load is connected, the VMP pin voltage equals the  $V_{SS}$  potential.

The overcurrent status returns to the normal status when the load is released and the impedance between the EB- and EB+ pins (see **Figure 9** for a connection example) is 100 M $\Omega$  or higher. When the load is released, the VMP pin, which and the VCC pin are shorted with the  $R_{VCM}$  resistor, goes back to the  $V_{CC}$  potential. The IC detects that the VMP pin potential returns to overcurrent detection voltage 1 ( $V_{IOV1}$ ) or lower (or the overcurrent detection voltage 2 ( $V_{IOV2}$ ) or lower if the COVT pin is fixed at the 'L' level and overcurrent detection 1 is inhibited) and returns to the normal status.

### Overcharge status

If one of the battery voltages becomes higher than the overcharge detection voltage ( $V_{CU}$ ) during charging under normal status and it continues for the overcharge detection delay time ( $t_{CU}$ ) or longer, the charging FET turns off to stop charging. This status is called the overcharge status. The 'H' level signal is output to the conditioning pin corresponding to the battery which exceeds the overcharge detection voltage until the battery becomes equal to lower than the overcharge release voltage ( $V_{CD}$ ). The battery can be discharged by connecting an Nch FET externally. The discharging current can be limited by inserting R11, R12 and R13 resistors (see **Figure 9** for a connection example). The VMP and VCC pins are shorted by the  $R_{VCM}$  resistor under the overcharge status.

The overcharge status is released in two cases:

- <1> The battery voltage which exceeded the overcharge detection voltage ( $V_{CU}$ ) falls below the overcharge release voltage ( $V_{CD}$ ), the charging FET turns on and the normal status returns.
- <2> If the battery voltage which exceeded the overcharge detection voltage ( $V_{CU}$ ) is equal or higher than the overcharge release voltage ( $V_{CD}$ ), but the charger is removed, a load is placed, and discharging starts, the charging FET turns on and the normal status returns.

The release mechanism is as follows: the discharge current flows through an internal parasitic diode of the charging FET immediately after a load is installed and discharging starts, and the VMP pin voltage decreases by about 0.6 V from the VCC pin voltage momentarily. The IC detects this voltage (overcurrent detection voltage 1 or higher), releases the overcharge status and returns to the normal status.

### Overdischarge status

If any one of the battery voltages falls below the overdischarge detection voltage ( $V_{DD}$ ) during discharging under normal status and it continues for the overdischarge detection delay time ( $t_{DD}$ ) or longer, the discharging FET turns off and discharging stops. This status is called the overdischarge status. When the discharging FET turns off, the VMP pin voltage becomes equal to the  $V_{SS}$  voltage and the IC's current consumption falls below the power-down current consumption ( $I_{PDN}$ ). This status is called the power-down status. The VMP and VSS pins are shorted by the  $R_{VSM}$  resistor under the overdischarge and power-down statuses.

The power-down status is canceled when the charger is connected and the voltage between VMP and  $V_{SS}$  is 3.0 V or higher (overcurrent detection voltage 3). When all the battery voltages becomes equal to or higher than the overdischarge release voltage ( $V_{DU}$ ) in this status, the overdischarge status changes to the normal status.

### Delay circuits

The overcharge detection delay time ( $t_{CU1}$  to  $t_{CU3}$ ), overdischarge detection delay time ( $t_{DD1}$  to  $t_{DD3}$ ), and overcurrent detection delay time 1 ( $t_{IOV1}$ ) are changed with external capacitors (C4 to C6).

The delay times are calculated by the following equations:

	Min.	Typ.	Max.
$t_{CU}[S] = \text{Delay factor} \times C4 [\mu F]$	1.07	2.13	3.19
$t_{DD}[S] = \text{Delay factor} \times C5 [\mu F]$	0.20	0.40	0.60
$t_{IOV1}[S] = \text{Delay factor} \times C6 [\mu F]$	0.10	0.20	0.30

**Caution** The delay time for overcurrent detection 2 and 3 is fixed by an internal IC circuit. The delay time cannot be changed via an external capacitor.

### CTL pin

[If the CTL logic is "normal"]<S-8233BA, S-8233BC, S-8233BE, S-8233BF>

If the CTL pin is floated under normal status, it is pulled up to the  $V_{CC}$  potential in the IC, and both the charging and discharging FETs turn off to inhibit charging and discharging. Both charging and discharging are also inhibited by applying the VCC pin to the CTL pin externally. At this time, the VMP and VCC pins are shorted by the  $R_{VCM}$  resistor.

When the CTL pin becomes equal to  $V_{SS}$  potential, charging and discharging are enabled and go back to their appropriate statuses for the battery voltages.

[If the CTL logic is "reverse"]<S-8233BB, S-8233BD>

When the CTL pin becomes equal to  $V_{SS}$  potential, both the charging and discharging FETs turn off to inhibit charging and discharging. If the CTL pin is floated under normal status, charging and discharging are enabled and go back to their appropriate statuses for the battery voltages.

**Caution** Please note unexpected behavior might occur when electrical potential difference between the CTL pin ('L' level) and VSS is generated through the external filter ( $R_{VSS}$  and  $C_{VSS}$ ) as a result of input voltage fluctuations.

**Table 5 Output voltage & current consumption by CTL pin voltage**

Statements		Normal & Overcharge state		Power down mode (Without charger)		
		High & Floated	Low	High	Low	Floated
CTL pin voltage		High & Floated	Low	High	Low	Floated
CTL logic "normal" S-8233BA S-8233BC S-8233BE S-8233BF	COP (Charge control)	High	Comply with battery voltage	High	Low	Unknown
	DOP (Discharge control)	High	Comply with battery voltage	High	High	High
	Current consumption	Typ.20 $\mu$ A	Typ.20 $\mu$ A	Typ. 1 nA	Typ. 1 nA	Unknown
	COP	Comply with battery voltage	High	Low	High	Unknown
CTL logic "reverse" S-8233BB S-8233BD	DOP	Comply with battery voltage	High	High	High	High
	Current consumption	Typ.20 $\mu$ A	Typ.20 $\mu$ A	Typ. 1 nA	Typ. 1 nA	Unknown

**0 V battery charging function**

This function is used to recharge the three serially-connected batteries after they self-discharge to 0 V. When the 0 V charging start voltage ( $V_{0CHAR}$ ) or higher is applied to between VMP and VSS by connecting the charger, the charging FET gate is fixed to  $V_{SS}$  potential.

When the voltage between the gate sources of the charging FET becomes equal to or higher than the turn-on voltage by the charger voltage, the charging FET turns on to start charging. At this time, the discharging FET turns off and the charging current flows through the internal parasitic diode in the discharging FET. If all the battery voltages become equal to or higher than the overdischarge release voltage ( $V_{DU}$ ), the normal status returns.

**Caution** In the products without 0 V battery charging function, the resistance between VCC and VMP and between VSS and VMP are lower than the products with 0 V battery charging function. It causes to that overcharge detection voltage increases by the drop voltage of R5 (see Figure 9 for a connection example) with sink current at VMP.

The COP output is undefined below 2.0 V on VCC-VSS voltage in the products without 0 V battery charging function.

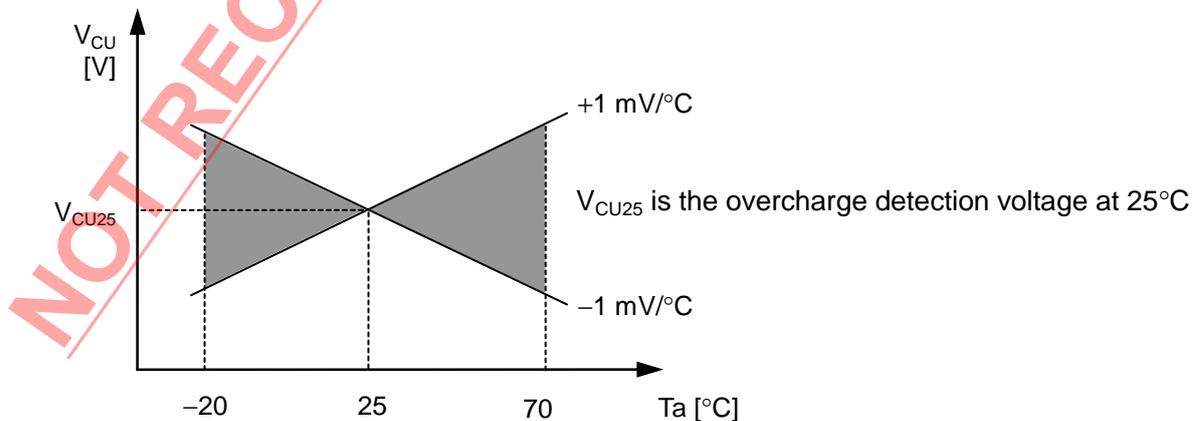
**Voltage temperature factor**

Voltage temperature factor 1 indicates overcharge detection voltage, overcharge release voltage, overdischarge detection voltage, and overdischarge release voltage.

Voltage temperature factor 2 indicates overcurrent detection voltage.

The Voltage temperature factors 1 and 2 are expressed by the oblique line parts in **Figure 5**.

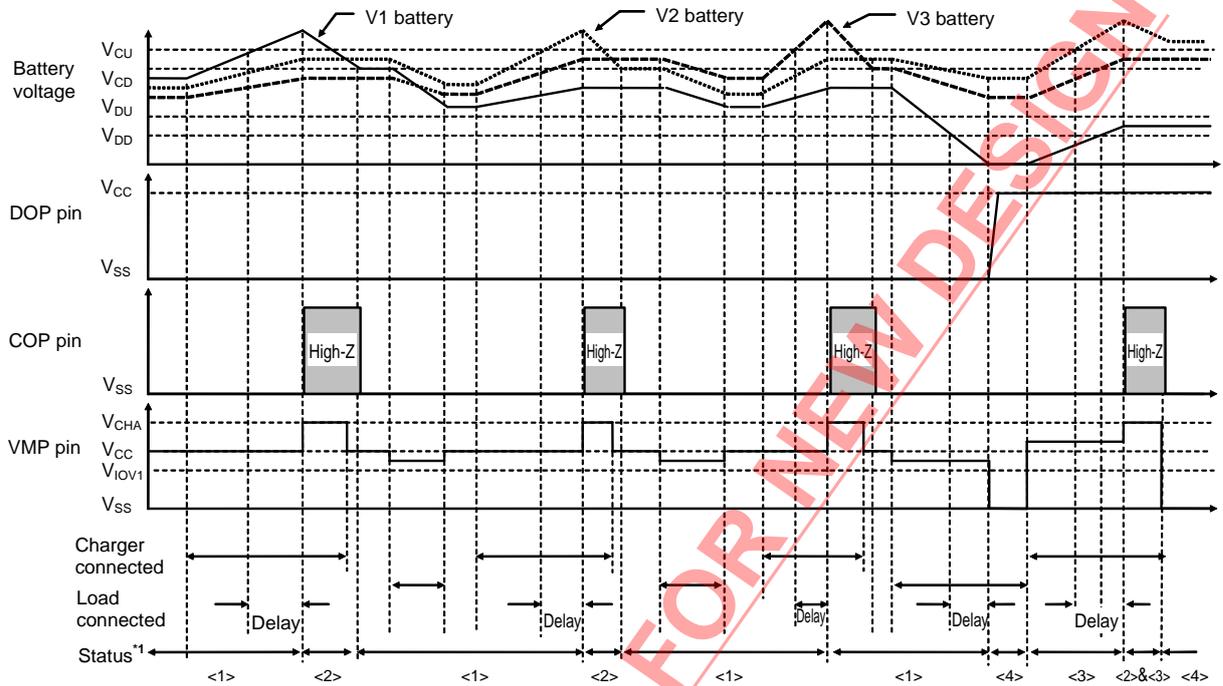
Ex. Voltage temperature factor of overcharge detection voltage Typ.



**Figure 5**

■ Timing Charts

1. Overcharge detection

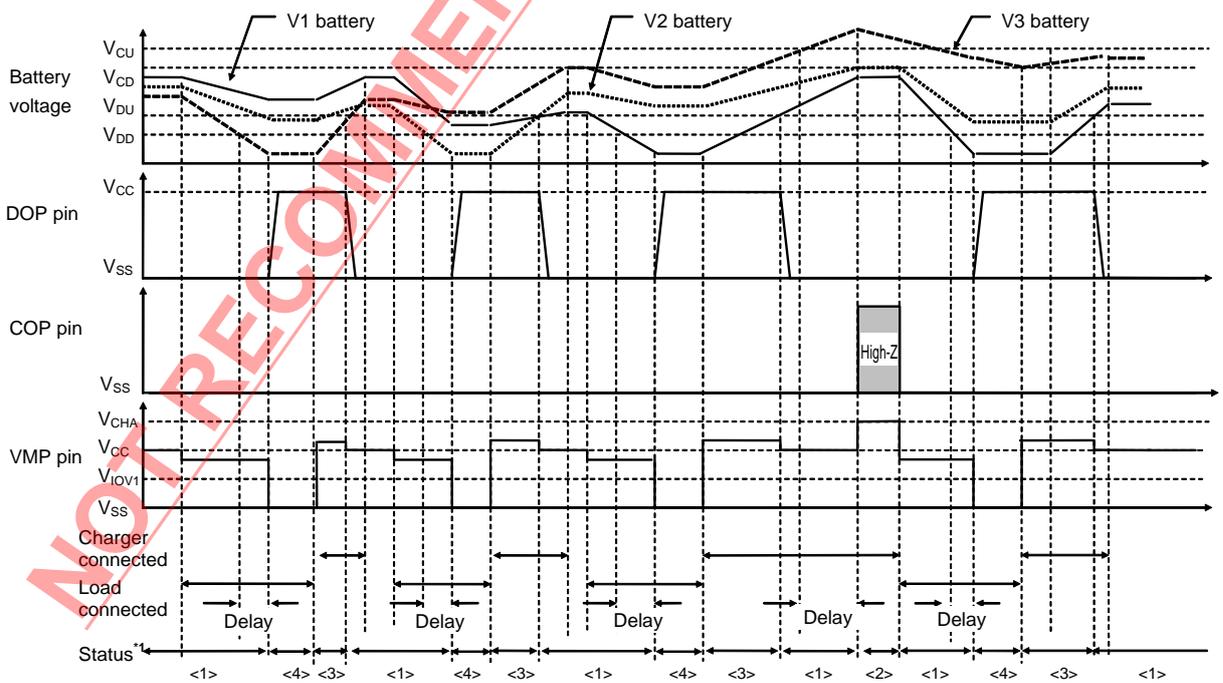


\*1. <1> Normal status, <2> Overcharge status, <3> Overdischarge status, <4> Power-down status

Remark The charger is assumed to charge with a constant current. V<sub>CHA</sub> indicates the open voltage of the charger.

Figure 6

2. Overdischarge detection

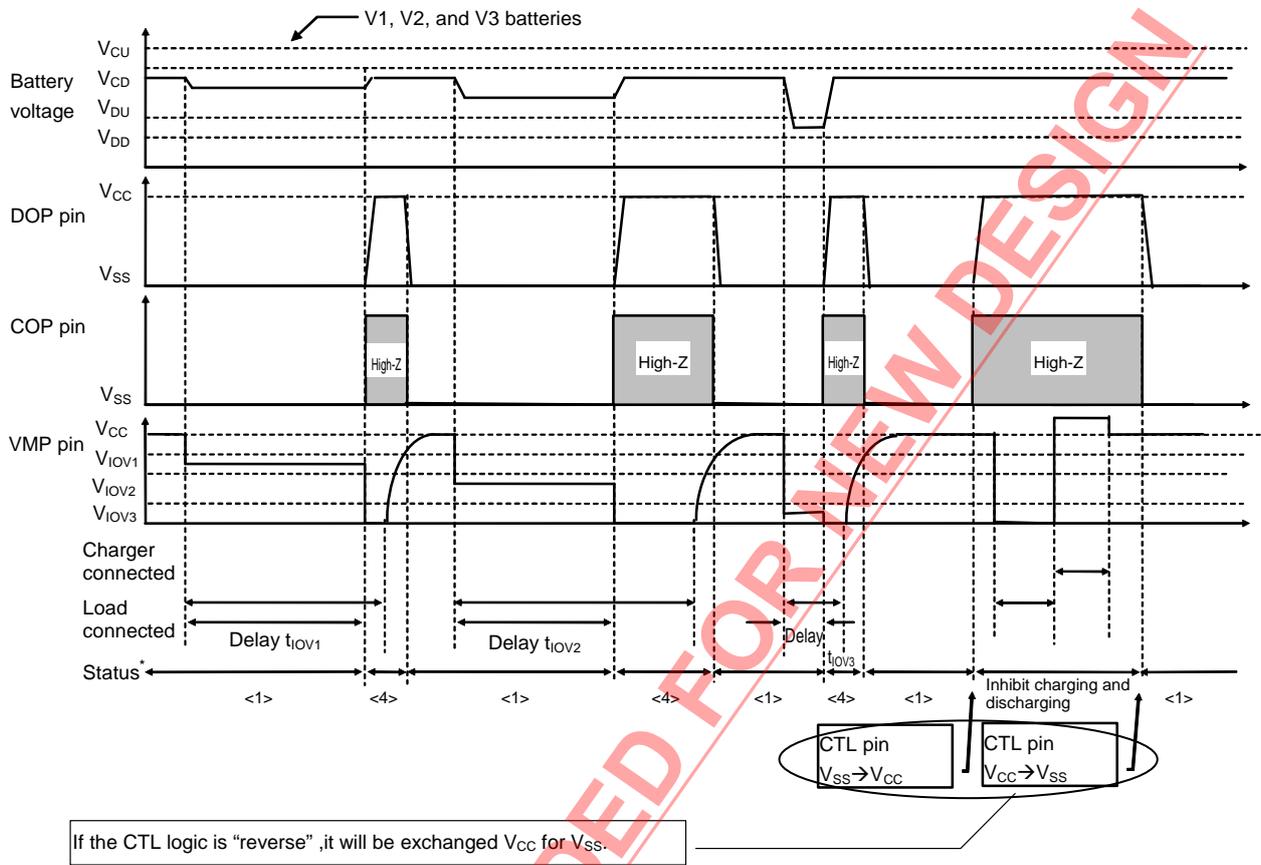


\*1. <1> Normal status, <2> Overcharge status, <3> Overdischarge status, <4> Power-down status

Remark The charger is assumed to charge with a constant current. V<sub>CHA</sub> indicates the open voltage of the charger.

Figure 7

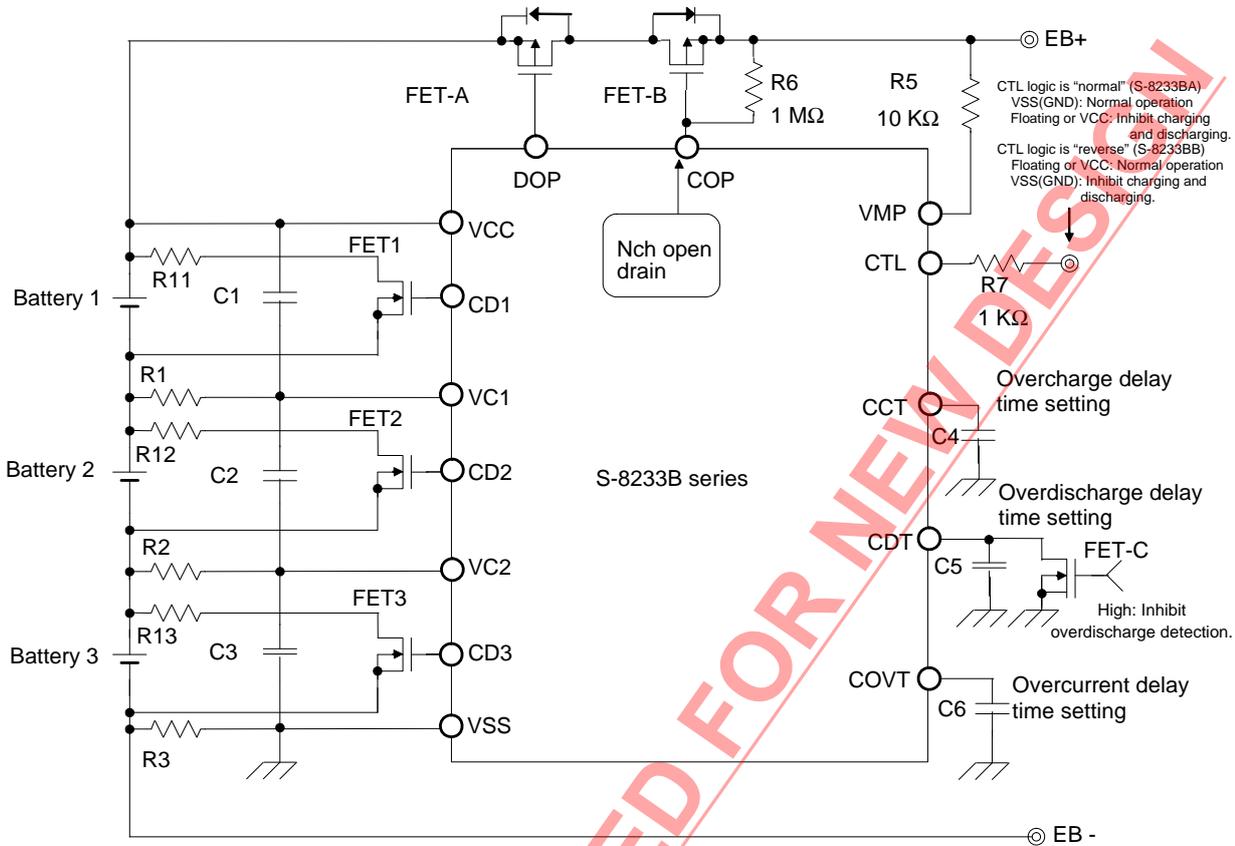
3. Overcurrent detection



\*1. <1>Normal status, <2>Overcharge status, <3>Overdischarge status, <4>Overcurrent status

Figure 8

■ **Battery Protection IC Connection Example**



**Figure 9**

[Description of **Figure 9**]

- R11, R12, and R13 are used to adjust the battery conditioning current. The conditioning current during overcharge detection is given by  $V_{cu}$  (overcharge detection voltage)/R (R: resistance). To disable the conditioning function, open CD1, CD2, and CD3.
- The overcharge detection delay time ( $t_{cu1}$  to  $t_{cu3}$ ), overdischarge detection delay time ( $t_{dd1}$  to  $t_{dd3}$ ), and overcurrent detection delay time ( $t_{ov1}$ ) are changed with external capacitors (C4 to C6). See the electrical characteristics.
- R6 is a pull-up resistor that turns FET-B off when the COP pin is opened. Connect a 100 kΩ to 1 MΩ resistor.
- R5 is used to protect the IC if the charger is connected in reverse. Connect a 10 kΩ to 50 kΩ resistor.
- If capacitor C6 is absent, rush current occurs when a capacitive load is connected and the IC enters the overcurrent mode. C6 must be connected to prevent it.
- If capacitor C5 is not connected, the IC may enter the overdischarge status due to variations of battery voltage when the overcurrent occurs. In this case, a charger must be connected to return to the normal status. To prevent this, connect an at least 0.01 μF capacitor to C5.
- If a leak current flows between the delay capacitor connection pin (CCT, CDT, or COVT) and VSS, the delay time increases and an error occurs. The leak current must be 100 nA or less.
- Overdischarge detection can be disabled by using FET-C. The FET-C off leak must be 0.1 μA or less. If overdischarge is inhibited by using this FET, the current consumption does not fall below 0.1 μA even when the battery voltage drops and the IC enters the overdischarge detection mode.
- R1, R2, and R3 must be 1 kΩ or less.
- R7 is the protection of the CTL when the CTL pin voltage higher than  $V_{CC}$  voltage. Connect a 300 Ω to 5 kΩ resistor. If the CTL pin voltage never greater than the  $V_{CC}$  voltage (ex. R7 connect to  $V_{SS}$ ), without R7 resistance is allowed.

- Caution**
1. The above constants may be changed without notice.
  2. If any electrostatic discharge of 2000 V or higher is not applied to the S-8233B series with a human body model, R1, R2, R3, C1, C2, and C3 are unnecessary.
  3. It has not been confirmed whether the operation is normal or not in circuits other than the above example of connection. In addition, the example of connection shown above and the constant do not guarantee proper operation. Perform through evaluation using the actual application to set the constant.

## ■ Precautions

- If a charger is connected in the overdischarge status and one of the battery voltages becomes equal to or higher than the overcharge release voltage ( $V_{CU}$ ) before the battery voltage which is below the overdischarge detection voltage ( $V_{DD}$ ) becomes equal to or higher than the overdischarge release voltage ( $V_{DU}$ ), the overdischarge and overcharge statuses are entered and the charging and discharging FETs turn off. Both charging and discharging are disabled. If the battery voltage which was higher than the overcharge detection voltage ( $V_{CU}$ ) falls to the overcharge release voltage ( $V_{CD}$ ) due to internal discharging, the charging FET turns on.

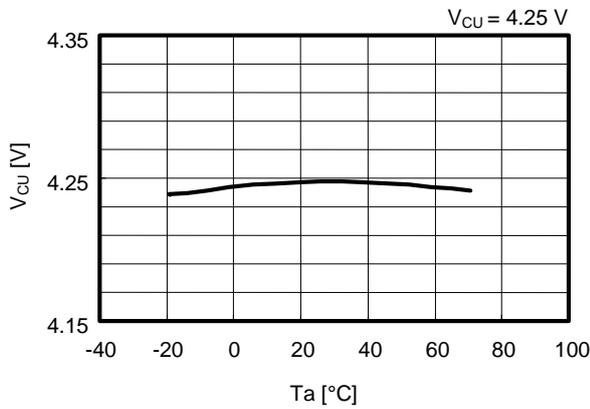
If the charger is detached in the overcharge and overdischarge status, the overcharge status is released, but the overdischarge status remains. If the charger is connected again, the battery status is monitored after that. The charging FET turns off after the overcharge detection delay time, the overcharge and overdischarge statuses are entered.

- If any one of the battery voltages is equal to or lower than the overdischarge release voltage ( $V_{DU}$ ) when they are connected for the first time, the normal status may not be entered. If the VMP pin voltage is made equal to or higher than the  $V_{CC}$  voltage (if a charger is connected), the normal status is entered.
- If the CTL pin floats in power-down mode, it is not pulled up in the IC, charging may not be inhibited. However, the overdischarge status becomes effective. At that time, current consumption would be increase because CTL pin is affected by noise. If the charger is connected, the CTL pin is pulled up, and charging and discharging are inhibited immediately.
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- SII claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

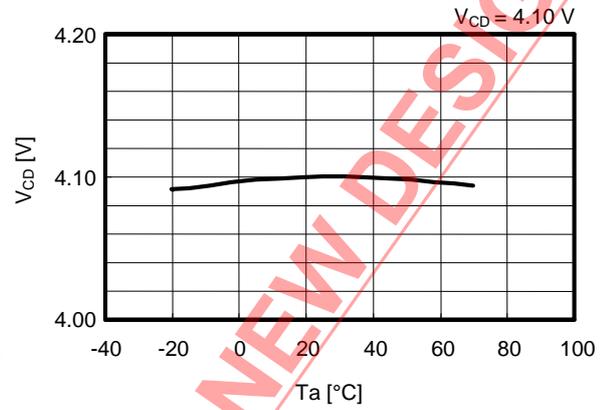
■ **Characteristics (Typical Data)**

**1. Detection voltage temperature characteristics**

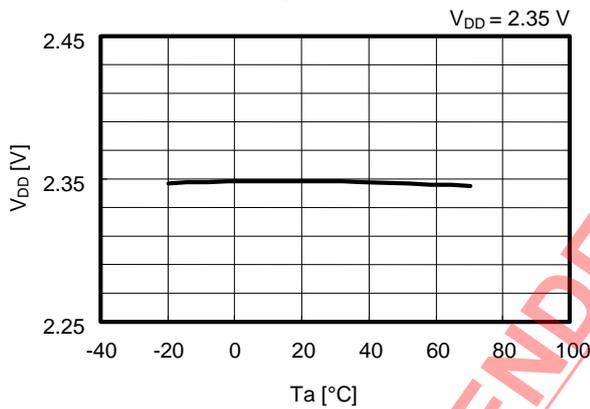
Overcharge detection voltage vs. temperature



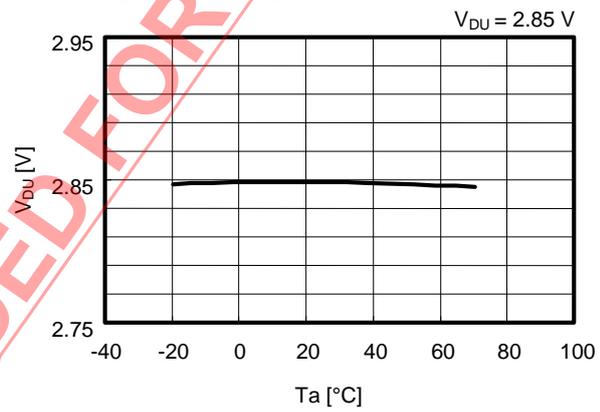
Overcharge release voltage vs. temperature



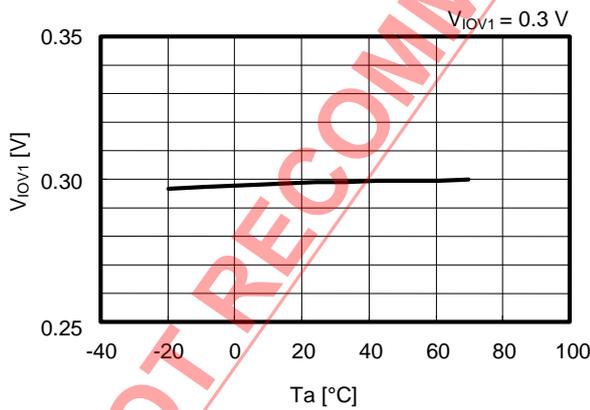
Overdischarge detection voltage vs. temperature



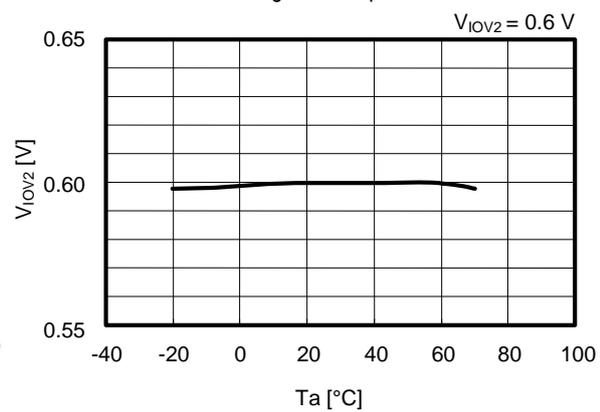
Overdischarge release voltage vs. temperature



Overcurrent1 detection voltage vs. temperature



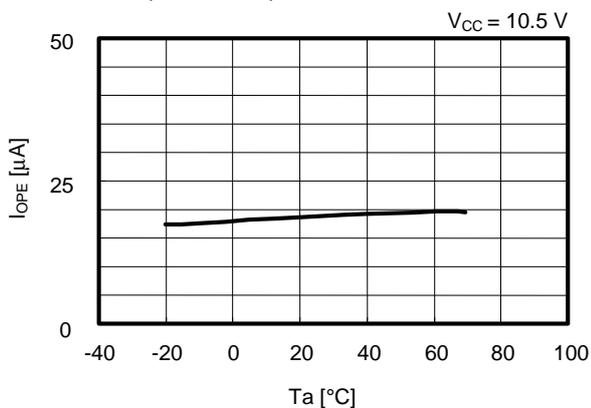
Overcurrent2 detection voltage vs. temperature



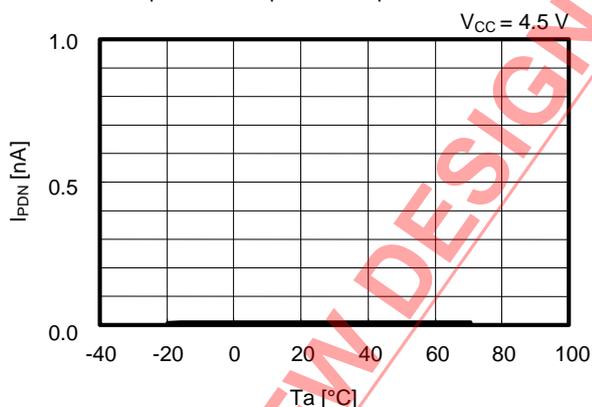
NOT RECOMMENDED FOR NEW DESIGN

**2. Current consumption temperature characteristics**

Current consumption vs. temperature in normal mode

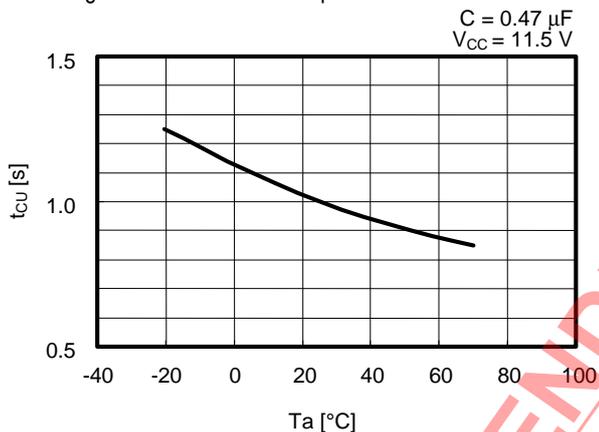


Current consumption vs. temperature in power-down mode

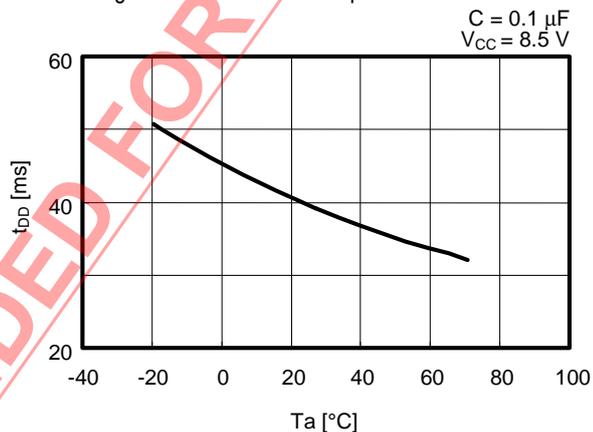


**3. Delay time temperature characteristics**

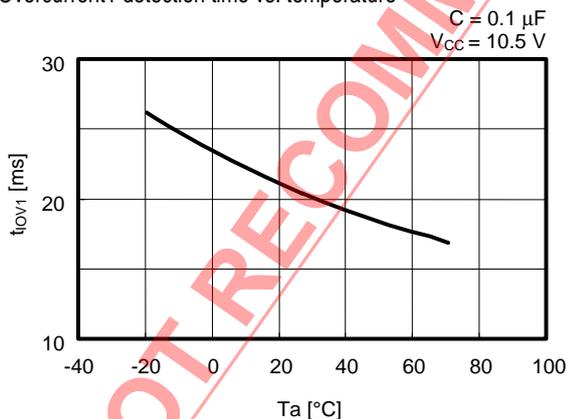
Overcharge detection time vs. temperature



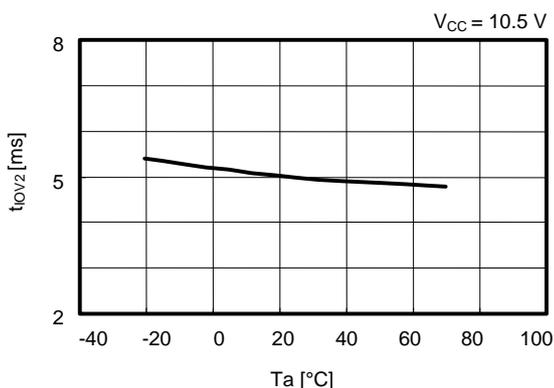
Overdischarge detection time vs. temperature

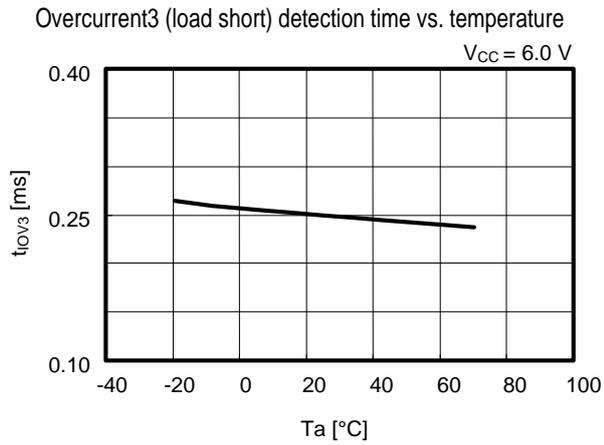


Overcurrent1 detection time vs. temperature

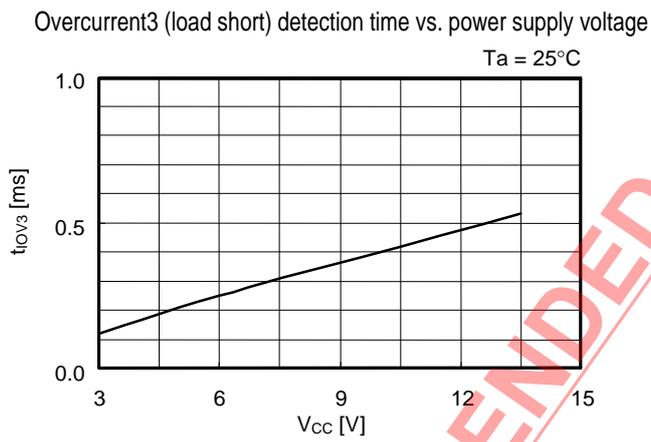


Overcurrent2 detection time vs. temperature



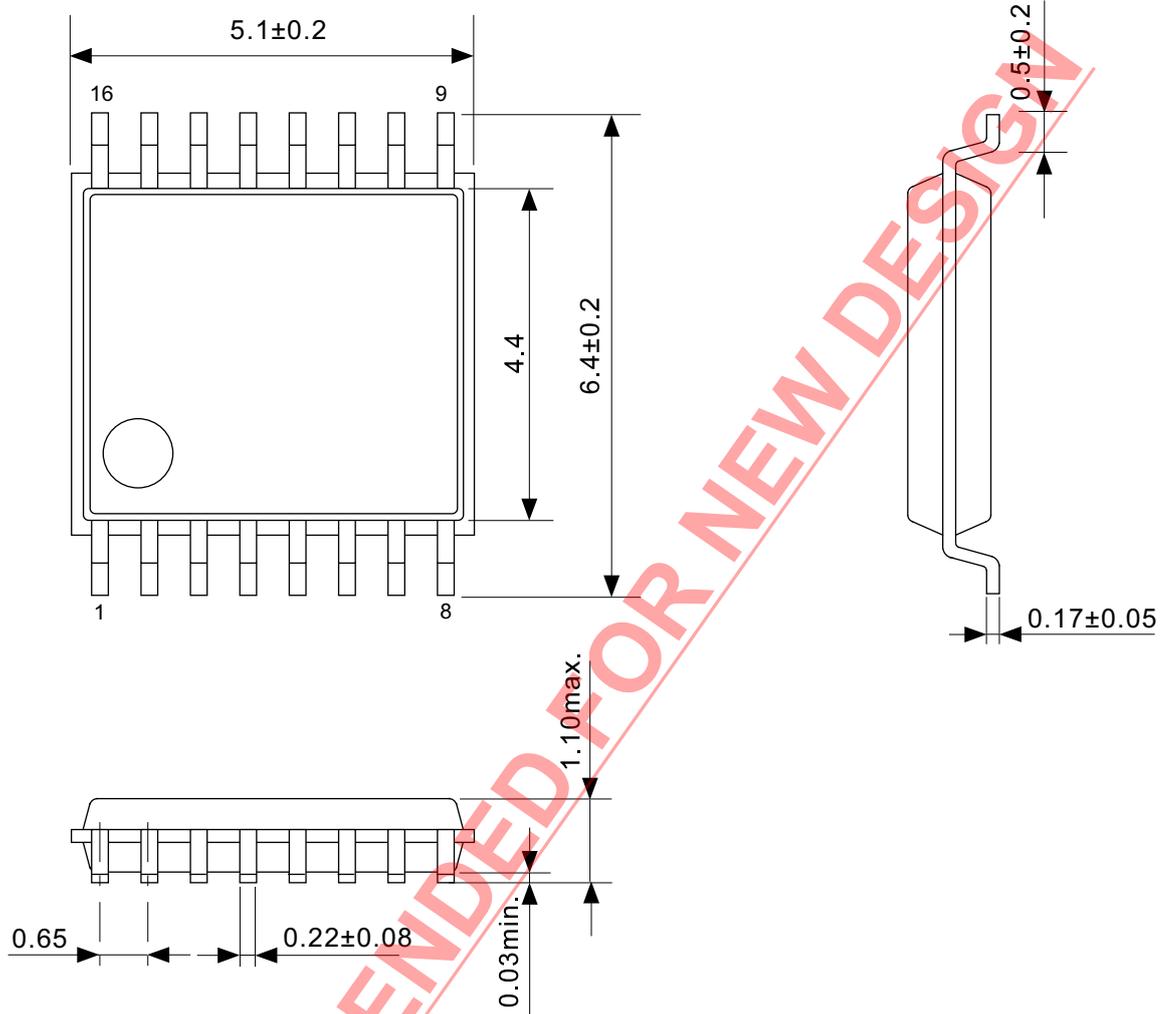


#### 4. Delay time vs. power supply voltage



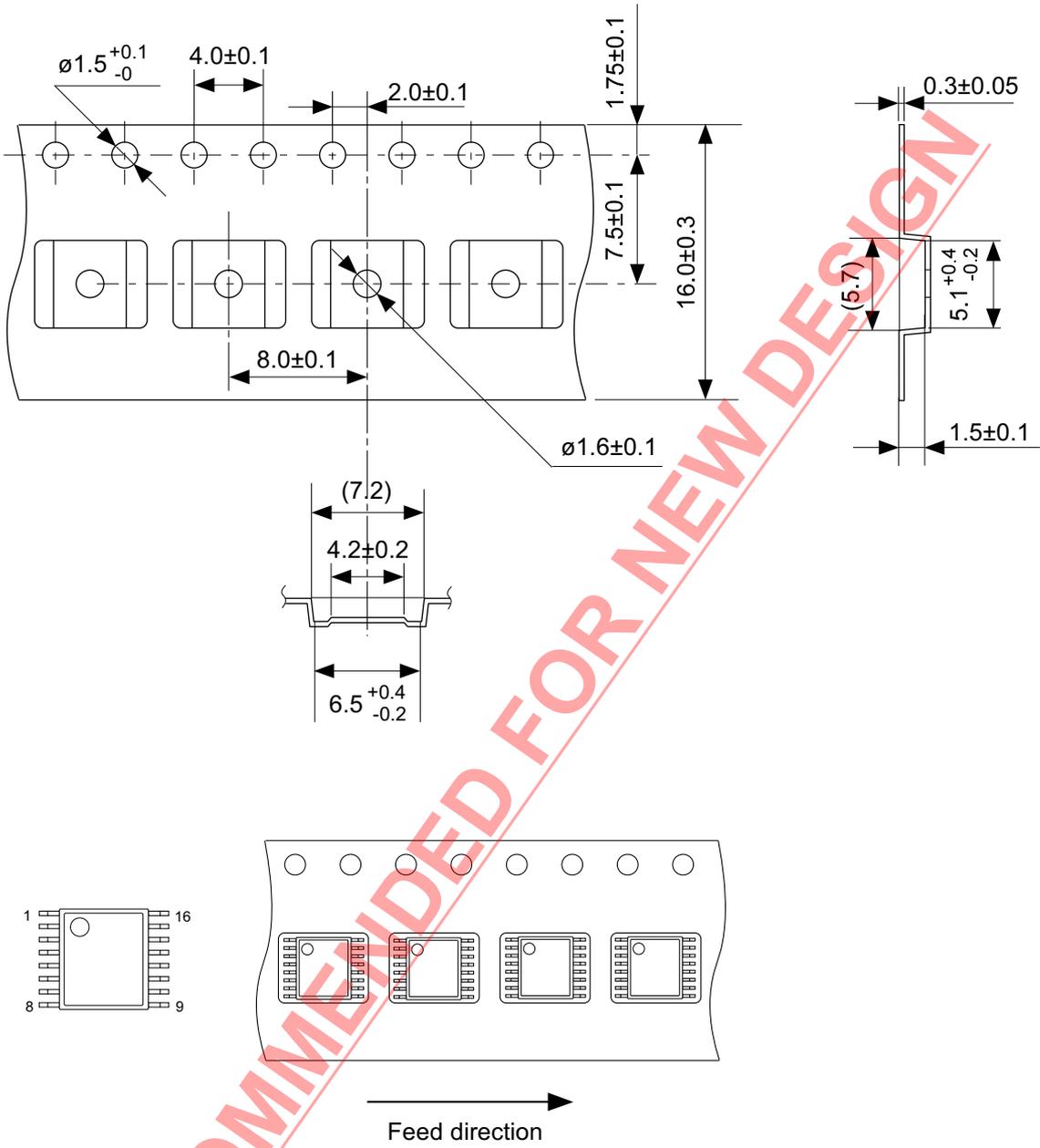
**Caution** Please design all applications of the S-8233B Series with safety in mind.

**NOT RECOMMENDED FOR NEW DESIGN**



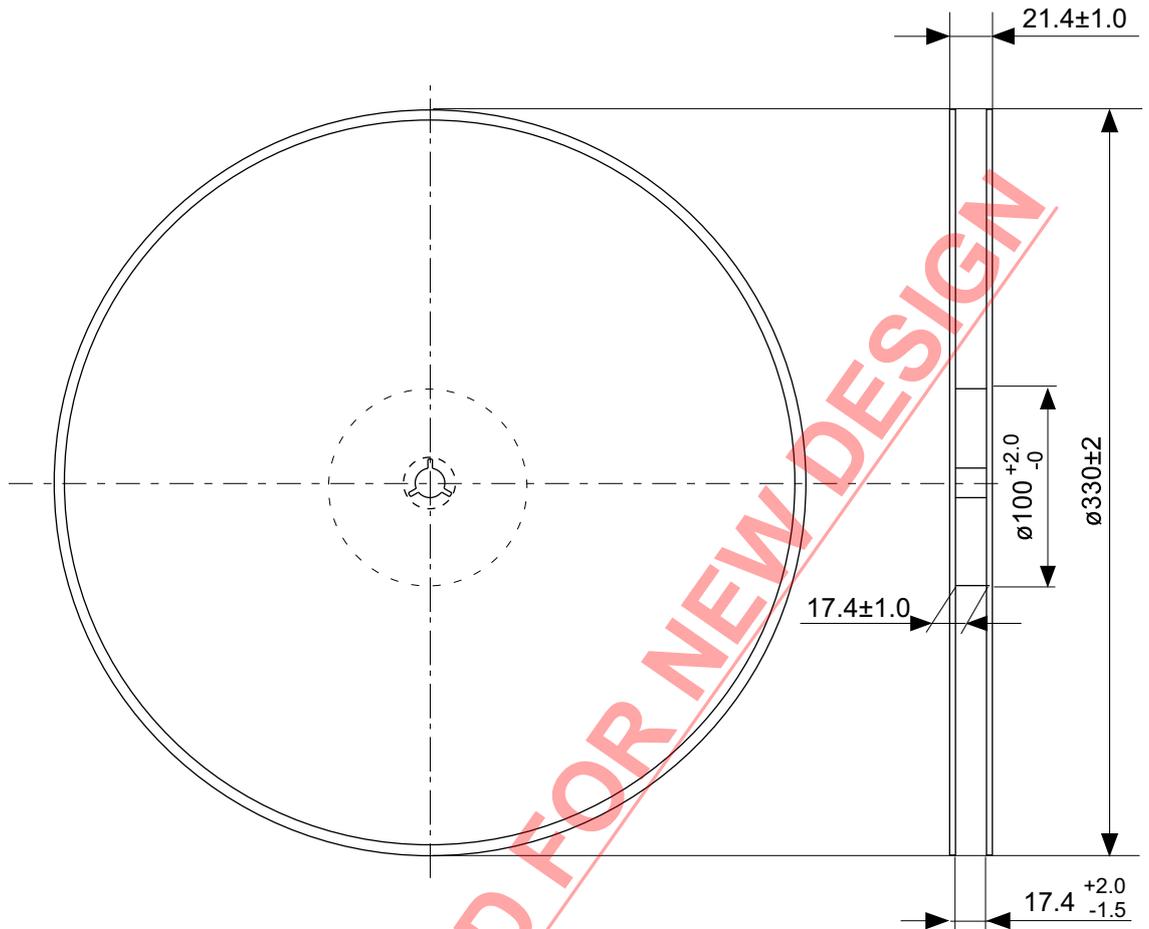
No. FT016-A-P-SD-1.1

TITLE	TSSOP16-A-PKG Dimensions
No.	FT016-A-P-SD-1.1
SCALE	
UNIT	mm
Seiko Instruments Inc.	

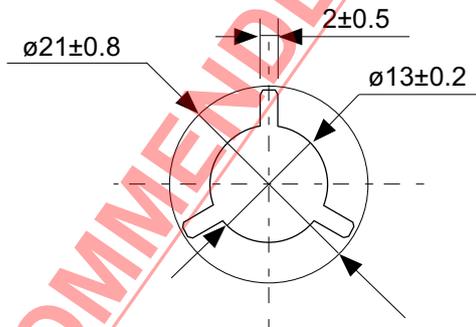


No. FT016-A-C-SD-1.1

TITLE	TSSOP16-A-Carrier Tape
No.	FT016-A-C-SD-1.1
SCALE	
UNIT	mm
Seiko Instruments Inc.	



Enlarged drawing in the central part



No. FT016-A-R-SD-2.0

TITLE	TSSOP16-A- Reel		
No.	FT016-A-R-SD-2.0		
SCALE		QTY.	2,000
UNIT	mm		
Seiko Instruments Inc.			



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