April 2012

FAIRCHILD SEMICONDUCTOR®

FDDS10H04A_F085A
Smart High Side Switch

Features

- Short circuit protection with latch
- Current limitation
- Overlaod protection
- Thermal shutdown with restart.
- Overvoltage protection(including load dump)
- Loss of ground protection
- Loss of supply protection(with external diode for charged inductive load)
- Very low standby current
- Fast demagnetization of inductive loads
- ESD protection
- Optimized static electromagnetic compatibility
- Diagnostic function - Proportional load current sense(with defined fault signal in case of overload operation, overtemperature shutdown and/or short circuit shutdown)
- Qualified to AEC

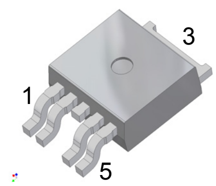
Typical Applications

- Power switch with current sense diagnostic feedback for DC ground loads
- All types of resistive, inductive, and capacitive loads
- Replace electromechanical relays, fuses and discrete circuits

Description

N channel power FET with charge pump, current controlled input and diagnostic feedbcak with load current sense, integrated in smart Trench chip on chip technology. Provides embedded protective functions.

TO252-5L

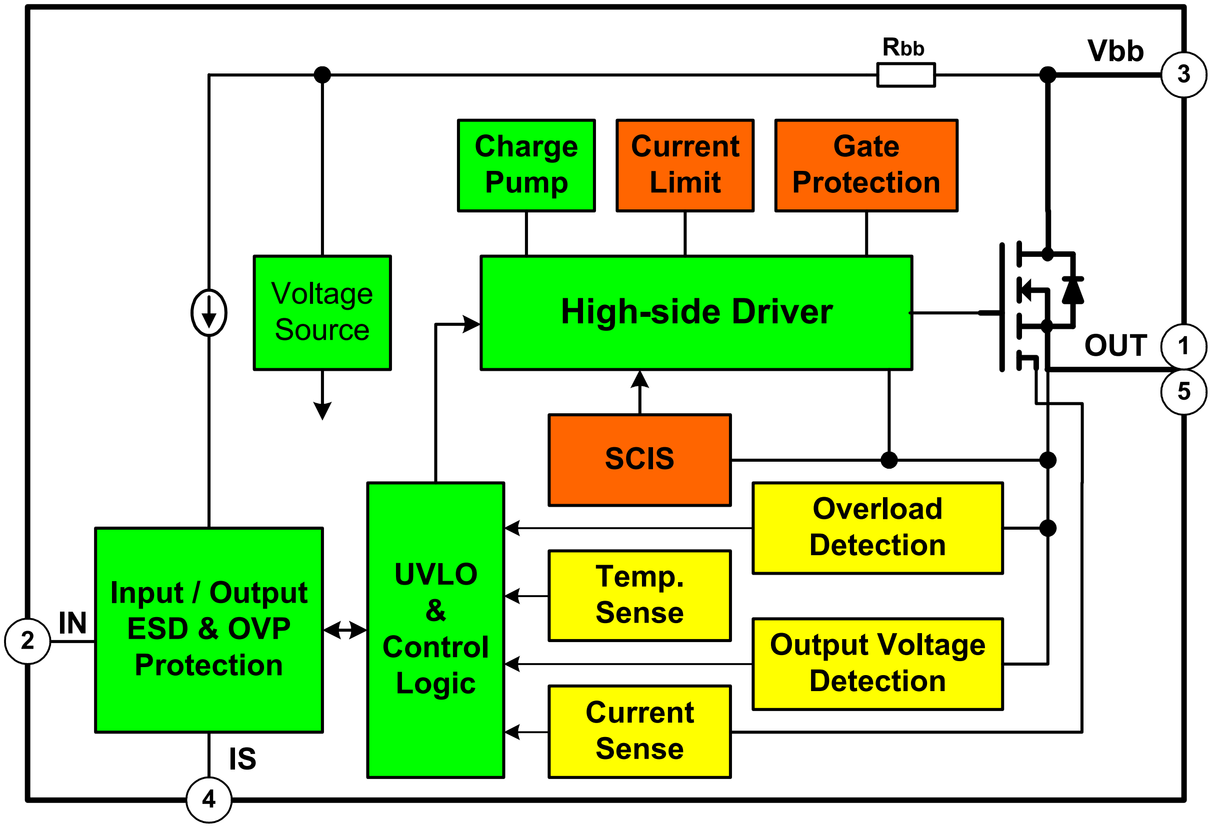


Ordering Information

Part Number	Package	Operating Temperature	Eco Status	Packing Method
FDDS10H04A_F085A	TO252-5L	-40 °C - 150 °C	RoHS	Tape & Reel

For Fairchild's definition of "green" Eco Status, please visit: http://www.fairchildsemi.com/company/green/rohs_green.html.

Block Diagrams



Pin Definitions

Pin Number	Pin Name	I/O	Pin Function Description
1	OUT	A	Output to loads; Pin1and 5 must be externally shorted
2	IN	A	Input: activates the power switch if shorted to ground
3	Vbb	P	Supply voltage; Pin3 and TAB are internally shorted
4	IS	A	Sense output ; Diagnostic feedback; Provides at normal operation a sense current proportion to the load current; in case of overload, over temperature and/or short circuit a defined current is provided
5	OUT	A	Output to loads; Pin1 and 5 must be externally shorted

Absolute Maximum Ratings

At T_j=25°C unless otherwise specified.

Parameter		Symbol	Values	Unit
Supply voltage [4)]		V_{bb}	38	V
Supply voltage for full short circuit protection [1)]		V_{bb}	30	V
Load dump protection $V_{LoadDump}$ = U_A + V_S, U_A=13.5V R_I=2Ω, R_L=1Ω, t_d=400ms, IN=Low o rHigh		$V_{LoadDump}$ [2)]	45	V
Load current (Short-circuit current)		I_L	Self-limited	V
Operating temperature range Storage temperature range		T_j T_{stg}	-40 ~ 150 -55 ~ 150	°C °C
Power Dissipation(DC)		P_{tot}	59	W
Inductive load switch-off energy dissipation [3)] Single pulse, I_L=10.7A, L=5mH, V_{bb}=12V, T_j=150°C		E_{AS}	288	mJ
Electrostatic discharge capability (ESD) (Human Body Model)	IS	V_{ESD}	2.8	KV
	IN	V_{ESD}	3	KV
	VBB, Output	V_{ESD}	5	KV
Current through input pin(DC) Current through current sense pin(DC)		I_{IN} I_{IS}	+15, -120 +15, -120	mA
Input voltage slew rate Vbb <= 16V Input voltage slew rate Vbb > 16V [4)]		dV_{bIN} / dt	self-limited 20	V/us

Note:

1) Short circuit is defined as a combination of remaining resistances and inductances. See schematic on page11.

2) VLoad dump is setup without the DUT connected to the generator

3) See also diagram on page 11.

4) See also on page 7. Slew rate limitation can be achieved by means of using a series resistor RIN in the input path. This resistor is also required for reverse operation. See also page 10.

Electrical Characteristics

At Tj=25°C, Vbb=12V unless otherwise specified.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Theramal Characteristics						
Thermal resistance	RthJC 5) RthJA	(junction to case) (junction to ambient) device on PCB 6), SMD version only	- - -	- 83 45	1.0 - 55	K/W
Load Switching Capability and Characteristics						
On-state resistance(Pin3 to pin 1,5)	RON	VIN=0, Vbb=5.5V, IL=7.5A, Tj=25°C VIN=0, Vbb=5.5V, IL=7.5A, Tj=150°C VIN=0, Vbb=12V, IL=7.5A Tj=25°C VIN=0, Vbb=12V, IL=7.5A Tj=150°C	-	4.5 12 4.5 12	10 16 10 16	mΩ
Output voltage drop limitation at small load currents(tab to pin 1,5)	VON(NL)	Tj=-40 ~ 150°C	-	35	65	mV
Nominal load current(tab to pin1,5)	IL(ISO) IL(NOM)	ISO Proposal6) :VON<=0.5V, TC=85°C, Tj<=150°C SMD 6) 7) : VON<= 0.5V, Ta=85°C, Tj<=150°C	33 10.5	41 12	- -	A
Turn-on time (to 90% VOUT) Turn-off time (to 10% VOUT)	ton toff	RL=2.2Ω, Tj = -40~ 150°C	- -	160 110	400 400	us
Slew rate on (25% to 50% VOUT)	dV / dton	RL=2.2Ω, Tj = -40~ 150°C	-	0.2	0.5	V/us
Slew rate off (50% to 25% VOUT)	-dV / dtoff	RL=2.2Ω, Tj = -40~ 150°C	-	0.3	0.65	V/us
Operating Parameters						
Operating Voltage(VIN=0)	Vbb(ON)	Tj = -40~ 150°C	5.5		38	V
Under voltage shutdown 7) 8)	VbIN(u)		-	1.5	3.5	V
Under voltage restart of charge pump	Vbb(ucp)			3.7	5.5	V
Over voltage protection 9)	VZ,IN	Ibb=15mA, Tj = -40~ 150°C	42.5	47.3	-	V
Standby current	Ibb(off)	IIN=0, Tj = -40~ 120°C IIN=0, Tj = 150°C	- -	0.8 8	5.3 20	uA
Reverse Battery 10)						
Reverse battery voltage	-Vbb		-	-	18	V
On-state resistance(Tab to pin 1,5) 8)	RON(REV)	Vbb=-8V, VIN=0, IL=-7.5A, RIS=1KΩ,Tj=25°C Vbb=-8V,VIN=0,IL=-7.5A,RIS=1KΩ,Tj=150°C Vbb=-12V,VIN=0,IL=-7.5A,RIS=1KΩ,Tj=25°C Vbb=-12V,VIN=0,IL=-7.5A,RIS=1KΩ,Tj=150°C	- - - -	9.5 15 5.5 12	13 22 10 16	mΩ
Integrated resistor in Vbb line	Rbb	Is=1mA, VIN=5V @125°C	65	95	125	Ω
Inverse operation 11)						
Ouptut voltage drop(pin4 to pin 1, 5) 8)	-VON(inv)	IL=-10A,RIS=1KΩ,Tj=25°C IL=-10A,RIS=1KΩ,Tj=150°C	- -	800 600	- -	mV
Turn-on delay after inverse operation;	td(inv)	IL> 0A 8) VIN(inv)=VIN(fwd) = 0V	-	1	-	ms

Note:

5) Thermal resistance RthCH case to heatsink (about 0.5 ... 0.9 K/W with silicone paste) not included!

6) Device on76.2mm * 114mm * 1.57mm glass epoxyPCB. still air condition.

7) Not subject to production test, Parameters are calculated from Ron and Rthjc or Rthja.

8) not subject to production test, specified by design

9) See also VON(CL) in circuit diagram page 8.

10) For operation at voltages higher then |16V| please see required schematic on page 9.

11) Permanent Inverse operation results eventually in a current flow via the intrinsic diode of the power DMOS. In this case the device switches on with a time delay td(inv)) after- the transition from inverse to forward mode.

Electrical Characteristics

At Tj=25°C, Vbb=12V unless otherwise specified

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Protection Functions [12]						
Short circuit current limit (pin4 and tab to pin 1,5 at V_{ON}=6V [13) 14)]	$I_{L6(SC)}$	Tj=-40°C Tj=25°C Tj=150°C	- - 65	100 90 80	130 - -	A
Short circuit current limit (pin4 and tab to pin 1,5 at V_{ON}=12V [13)]	$I_{L12(SC)}$	Tj=-40°C Tj=25°C Tj=150°C	- - 40	80 70 60	120 - -	A
Short circuit current limit (pin4 and tab to pin 1,5 at V_{ON}=18V [13) 14)]	$I_{L18(SC)}$	Tj=-40°C Tj=25°C Tj=150°C	- - 33	63 55 47	81 - -	A
Short circuit current limit (pin4 and tab to pin 1,5 at V_{ON}=24V[13)]	$I_{L24(SC)}$	Tj=-40°C Tj=25°C Tj=150°C	- - 18	43 38 33	65 -	A
Short circuit current limit (pin4 and tab to pin 1,5 at V_{ON}=30V [13) 14)]	$I_{L30(SC)}$	Tj=-40°C Tj=25°C Tj=150°C	- - 7	25 24 23	50 --	A
Short circuit shutddown detection voltage	$V_{ON(SC)}$		2.5	3.5	4.5	V
Short circuit shutdown delay after input current positive slop Min value valid only if “off-signal” time exceeds 30us	$t_{d(SC1)}$	V_{ON} > $V_{ON(SC)}$, Tj=-40 ~ 150°C	250	450	650	us
Output clamp(inductive load switch off) at V_{OUT}= Vbb-$V_{ON(CL)}$(overvoltage) [15)]	$V_{ON(CL)}$	I_L=40mA	38.5	42	-	V
Thermal overload trip temperature	T_{jt}		150	175	-	°C
Thermal hysteresis	ΔT_{jt}		-	10	-	K

notes:

12) Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

13) Short circuit current limit for max. duration of td(SC1) , prior to shutdown, see also figures 3b on page 15.

14) not subject to production test, specified by design

15) See also figure 2b on page 14.

Electrical Characteristics

Aat Tj=25°C, V_{bb}=12V unless otherwise specified.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Diagnostic Characteristics						
Current sense ratio, static on-condition $K_{ILIS} = I_L : I_{IS} < I_{IS,min}$ [16] $V_{IS} < V_{OUT}$-5V, $V_{bIN} > 4.5V$	K_{ILIS}		-	11000	-	-
		I_L=30A, Tj=-40°C	8000	11000	13500	
		I_L=30A, Tj=25°C	8000	10500	13000	
		I_L=30A, Tj=125°C	8000	10500	13000	
		I_L=7.5A, Tj=-40°C	5500	11000	16500	
		I_L=7.5A, Tj=25°C	5500	11500	17000	
		I_L=7.5A, Tj=125°C	5500	11000	16500	
		I_L=2.5A, Tj=-40°C	5000	10500	17000	
		I_L=2.5A, Tj=25°C	5000	11000	17500	
		I_L=2.5A, Tj=125°C	5000	12000	18500	
		I_L=0.5A, Tj=-40°C	4000	9900	18000	
		I_L=0.5A, Tj=25°C	4000	11000	18000	
		I_L=0.5A, Tj=125°C	4000	12000	19000	
I_{IN}=0(e.g. during deenergizing of inductive loads)			-		-	
Sense current under fault conditions[17]	$I_{IS,fault}$	V_{ON} > 1V,typ Tj=-40 ~ 150°C	4	6.2	9	mA
Sense saturation current	$I_{IS,lim}$	V_{ON} < 1V,typ Tj=-40 ~ 150°C	4	7.5	9	mA
Fault-sense signal delay after input current positive slop	$t_{delay(fault)}$	V_{ON} > 1V,typ Tj=-40 ~ 150°C	250	450	650	us
Current sense leakage current	$I_{IS(LL)}$	I_{IN} =0	-	0	0.5	uA
Current sense offset current	$I_{IS(LH)}$	V_{IN} =0, I_L <= 0	-	0	2	uA
Minimum load current for sense functionality	$I_{L(MIN)}$	V_{IN} =0,Tj=-40 ~ 150°C	150	-	-	mA
Current sense settling time to $I_{ISstatic}$ after input current positive slop[18]	$t_{son(IS)}$	I_L =0 --> 20A ,Tj=-40 ~ 150°C	-	300	650	us
Current sense settling timeduring on condition [18]	$t_{slc(IS)}$	I_L =0 --> 20A ,Tj=-40 ~ 150°C	-	50	100	us
Overvoltage protection	$V_{Z,IS}$	I_{bb}=15mA, Tj=-40 ~ 150°C	42.5	47.3	-	V
Input						
Required current capability of input switch	$I_{IN(on)}$	Tj=-40 ~ 150°C	-	1.5	3	mA
Input current for turn-off	$I_{IN(off)}$	Tj=-40 ~ 150°C	-	-	15	uA

notes:

16) See also figures 4.x and 6.x on page 15 and 16.

17) Fault conditions are overload during on (i.e. VON>1V typ.), overtemperature and short circuit; see also truth table on page 7.

18) not subject to production test, specified by design

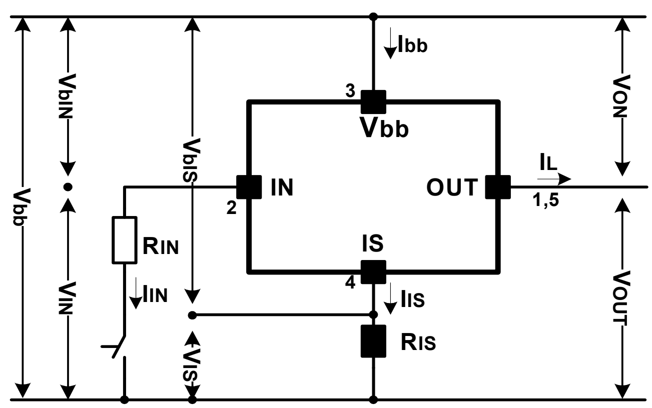
Application Information

1. Truth Table

Sense current under fault conditions	Input Current Level	Output Level	Current Sense
Normal operation	L H	L H	= 0 ($I_{IS(LL)}$) nominal
Overload [19]	L H	L H	= 0 ($I_{IS(LL)}$) $I_{IS,fault}$
Short circuit to GND [20]	L H	L L	= 0 ($I_{IS(LL)}$) $I_{IS,fault}$
Overtemperature	L H	L L	= 0 ($I_{IS(LL)}$) $I_{IS,fault}$
Short circuit to V_{bb}	L H	H H	= 0 ($I_{IS(LL)}$) < nominal [21]
Open load	L H	Z H	= 0 ($I_{IS(LL)}$) = 0 ($I_{IS(LH)}$)

L = " LOW " Level, Z = High impedance, potential depends on external circuit, H = "HIGH" Level

2.Terms



Notes:

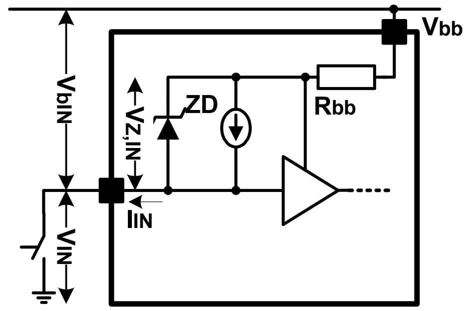
19) Overload is detected at the following condition: 1V (typ.) < V_{ON} < 3.5V (typ.) . See also page 10.

20) Short Circuit is detected at the following condition: V_{ON} > 3.5V (typ.) . See also page 11.

21) Low ohmic short to Vbb may reduce the output current I_L and therefore also the sense current I_{IS}.

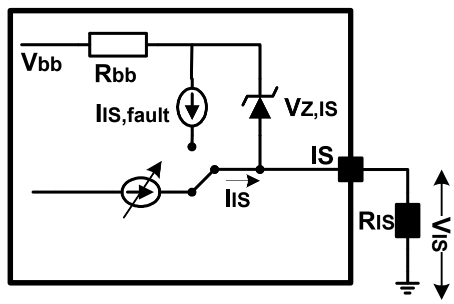
3. Detailed Function Blocks

3.1 Input circuit(ESD protection)



ESD zener diode:47.3V typ., max 15mA

3.2 Current sense output

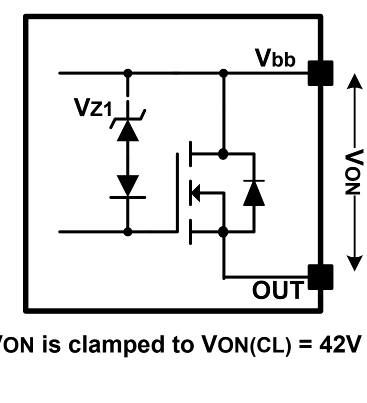


$V_{Z,IS}$ = 47.3 V (typ.), R_{IS} = 1KΩ nominal (or 1KΩ /n, if n devices are connected in parallel). $I_S = I_L/k_{ilis}$ can be only driven by the internal circuit as long as $V_{OUT} - V_{IS}$ > 5V. Therefore RIS should be less than

$$\frac{V_{bb} - 5V}{9mA}$$

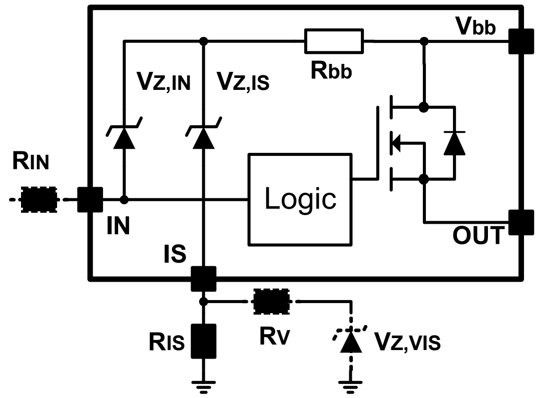
Note: For large values of R_{IS} the voltage VIS can reach almost V_{bb}. See also overvoltage protection. If you don't use the current sense output in your application, you can leave it open.

3.3 Inductive and overvoltage output clamp



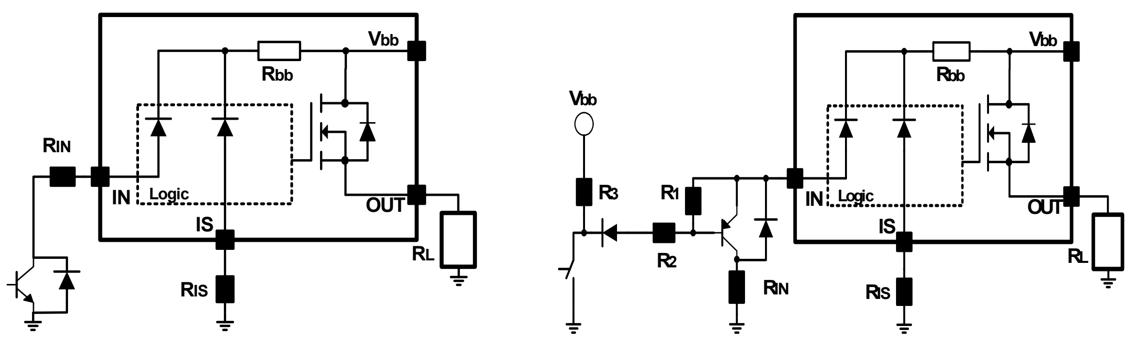
V_{ON} is clamped to $V_{ON(CL)}$ = 42V typ

3.4 Overvoltage protection of logic part



Rbb = 95Ω typ., VZ,IN = VZ,IS = 47.3V typ., RIS = 1KΩ nominal. Note that when overvoltage exceeds 47.3V typ. a voltage above 5V can occure between IS and GND, if RV, VZ,VIS are not used.

3.5 Reverse battery protection

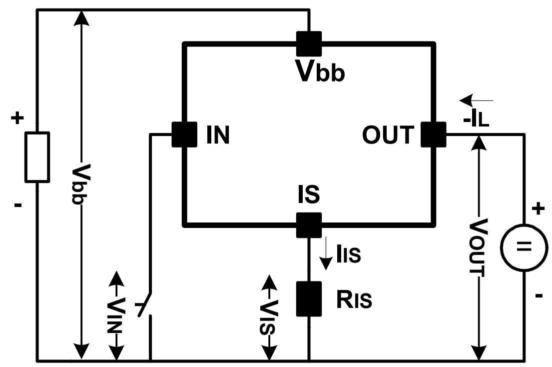


RIS typ. 1KΩ. Add RIN for reverse battery pprotection in application with Vbb above 16V;

$$\frac{1}{R_{IN}} + \frac{1}{R_{is}} = \frac{0.082A}{|V|_{bb} - 9V}$$

To minimise power dissipation at reverse battery operation, the overall current into the IN and IS pin should be about 82mA. The current can be provided by using a small signal diode D in parallel to the input switch, by using a MOSFET input switch or by proper adjusting the current through RIS. Since the current via Rbb generates additional heat in the device, this has to be taken into account in the overall thermal consideration.

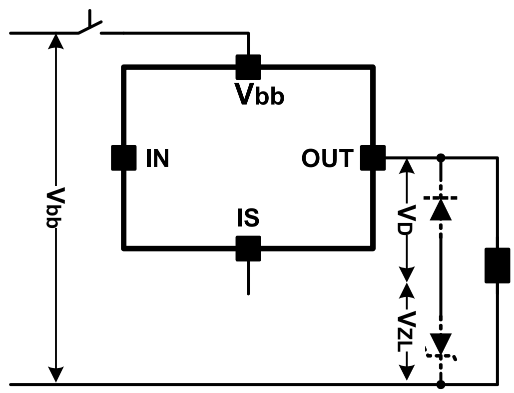
3.6 Inverse load current operation



The device can be operated in inverse load current mode ($V_{OUT} > V_{bb} > 0V$). The current sense feature is not available during this kind of operation ($I_{IS} = 0$). In case of inverse operation the intrinsic drain source diode is eventually conducting resulting in considerably increased power dissipation. The transition from inverse to forward mode can result in a delayed switch on.

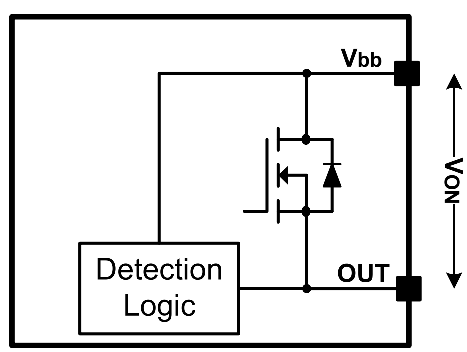
Note: Temperature protection during inverse load current operation is not possible!

3.7 Vbb disconnect with energised inductive load



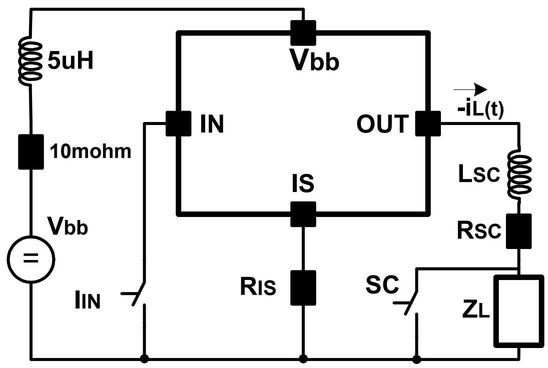
Provide a current path with load current capability by using a diode, a Z-diode, or a varistor. (V_{ZL}+ VD < 38V if R_{IN} = 0). For higher clamp voltages currents at IN and IS have to be limited to 120 mA.

3.8 Overload detection



Fault Condition: V_{ON} > 1V typ.

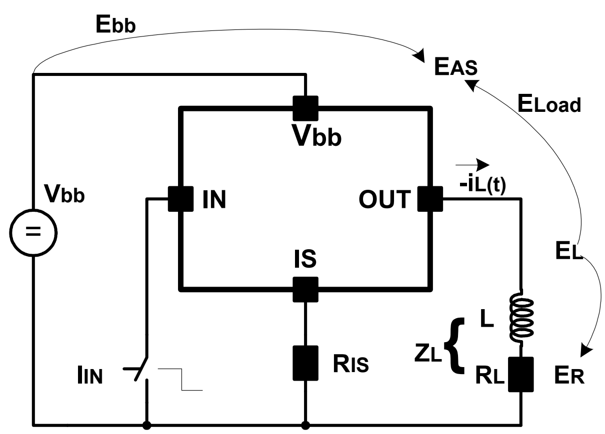
3.9 Short circuit



Fault Condition: $V_{ON} > V_{ON(SC)}$ (3.5V typ.) and $t > t_{d(SC)}$ (typ. 450us)

Short circuit is a combination of primary and secondary impedance's and a resistance's. Allowable combinations of minimum, secondary resistance for full protection at given secondary inductance and supply voltage for single short circuit event:

3.10 Inductive load switch-off energy dissipatoion



Energy stored in load inductance:

$$E_L = 1/2 \cdot L \cdot I_L^2$$

While demagnetizing load inductance, the energy dissipated in MOSFET is

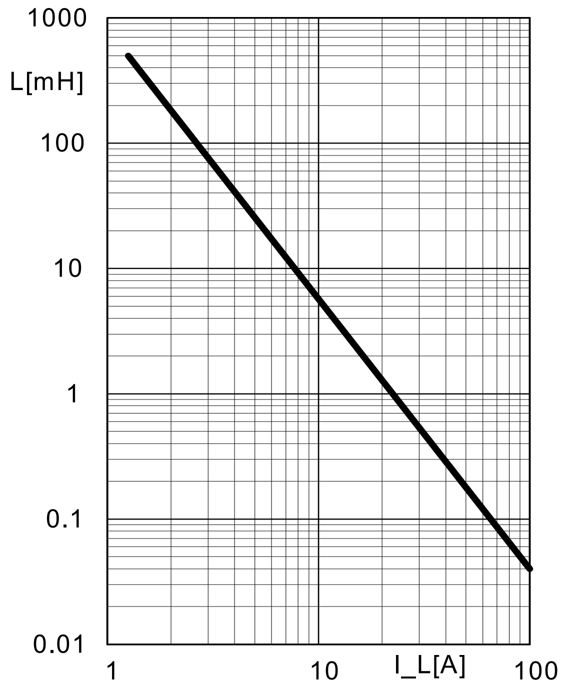
$$E_{AS} = E_{bb} + E_L - E_R = \int V_{ON(CL)} \cdot i_L(t)dt$$

with an approximate solution for $R_L > 0$, $V_{out(CL)} = V_{ON(CL)} - V_{bb}$:

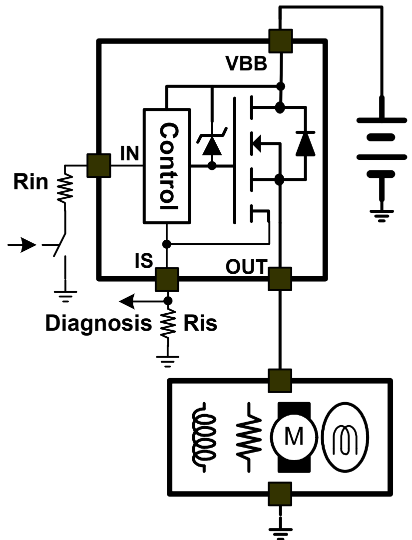
$$E_{AS} = \frac{I_L \cdot L}{2 \cdot R_L}(V_{ON(CL)})IN\left(1 + \frac{I_L \cdot R_L}{|V_{OUT(CL)}|}\right)$$

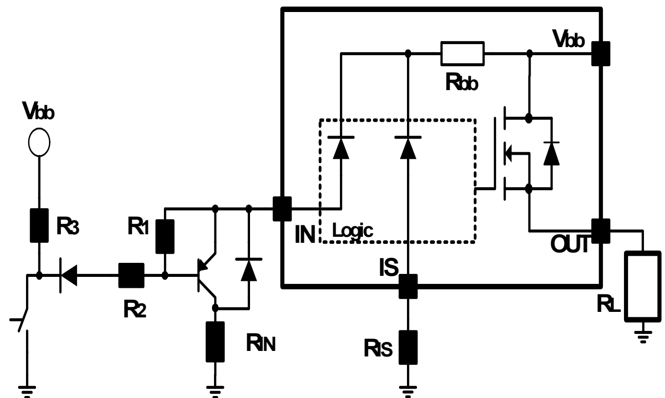
3.11 Maximum allowable load inductance for a single switch off

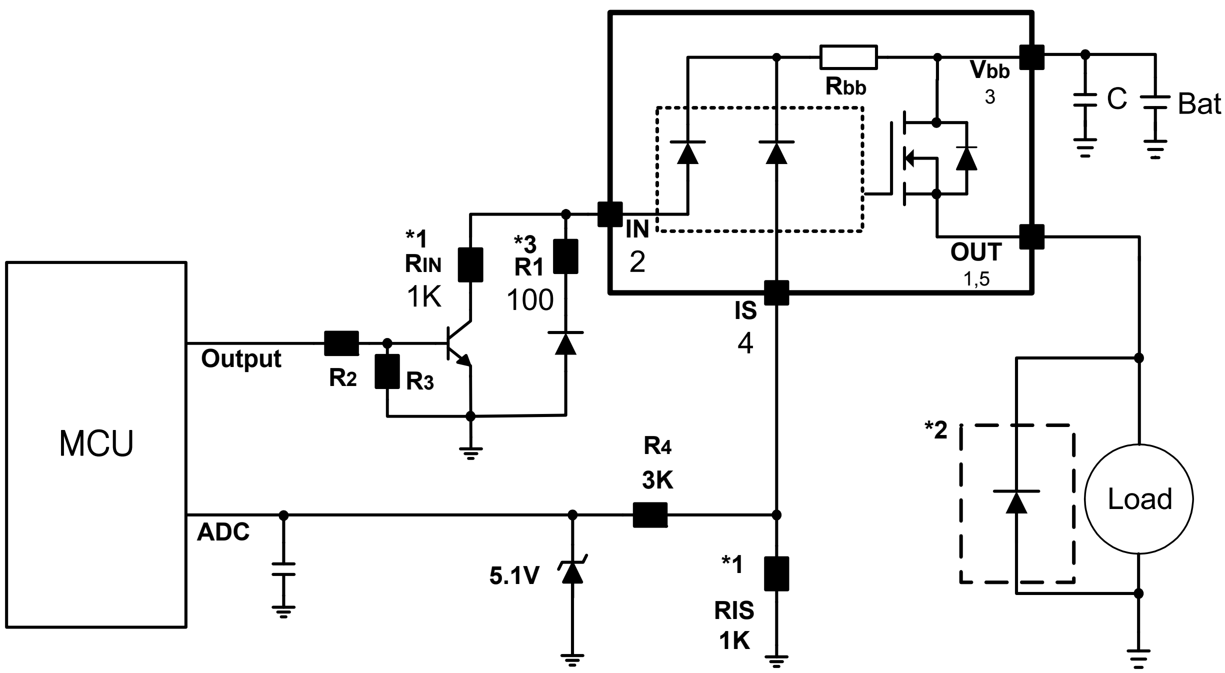
L=f(IL); T_j = 150°C, Vbb=12V, R_L = 0Ω



Typical Application Circuit







1) Ris and Rin is recommended as 1k

2) Put diode or capacitor between load to protect device or to remove noise.

3) For reverse battery protection function, R1 should be used less than 120Ω at -18V.

Timing Diagrams

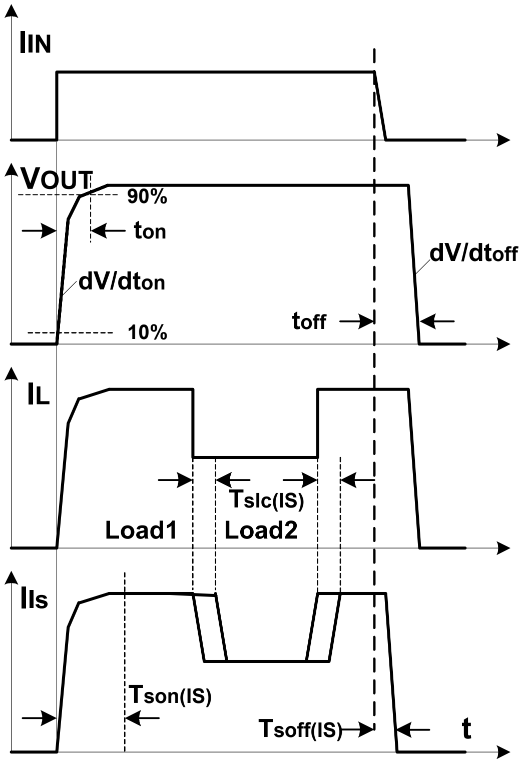


Figure 1a. Switching a resistive load, change of load current in on-condition

The sense signal is not valid during a setling time after turn-of/off and after change of load current

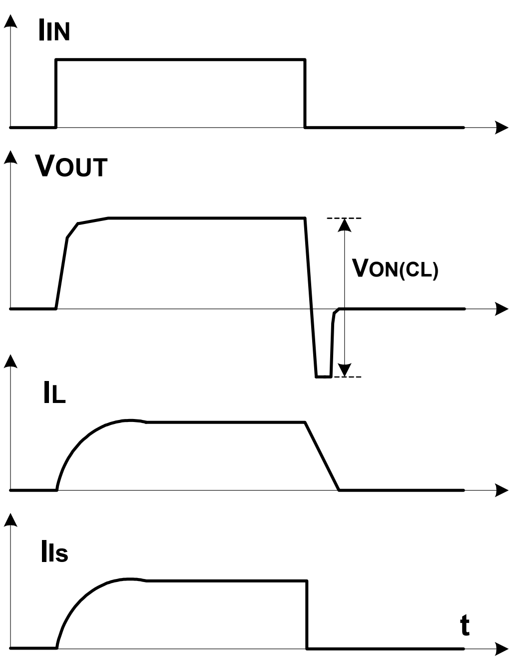


Figure 2b. Switching an inductive load

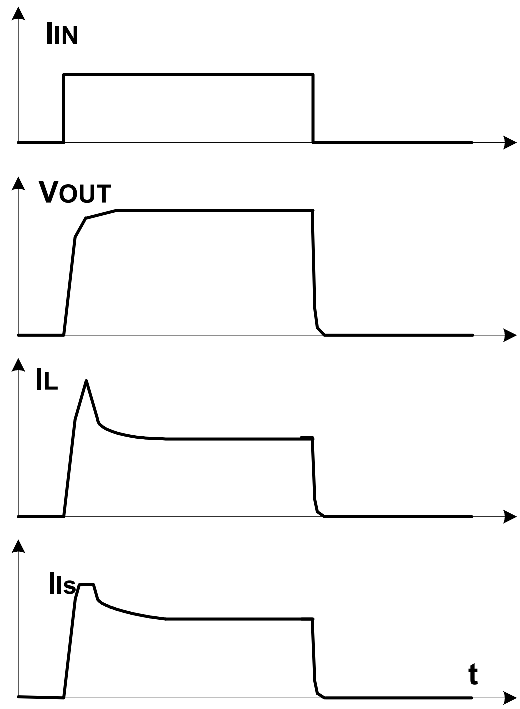


Figure 2a. Switching motors and lamps

As long as $V_{bIS} < V_{Z,IS}$ the sense current will never exceed $I_{IS,fault}$ and/or $I_{IS,lim}$

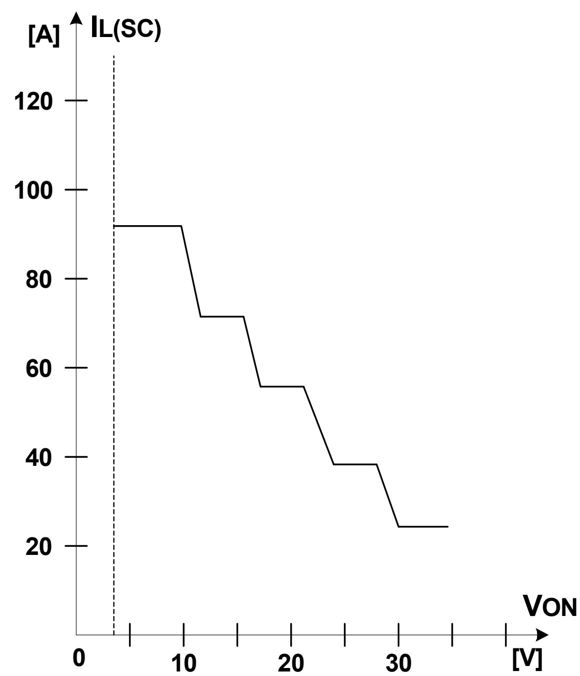


Figure 3a. Typ. current limitation charateristic

In case of $V_{ON} > V_{ON(SC)}$(typ.3.5V) the device will be switched off by internal short circuit detection

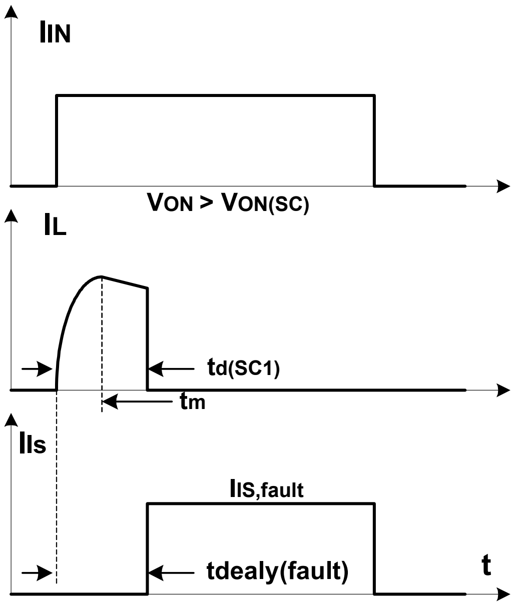


Figure 3b. Short circuit type one:
shut down by short circuit detection, reset by IIN=0

Shut down remains latched until next reset via input

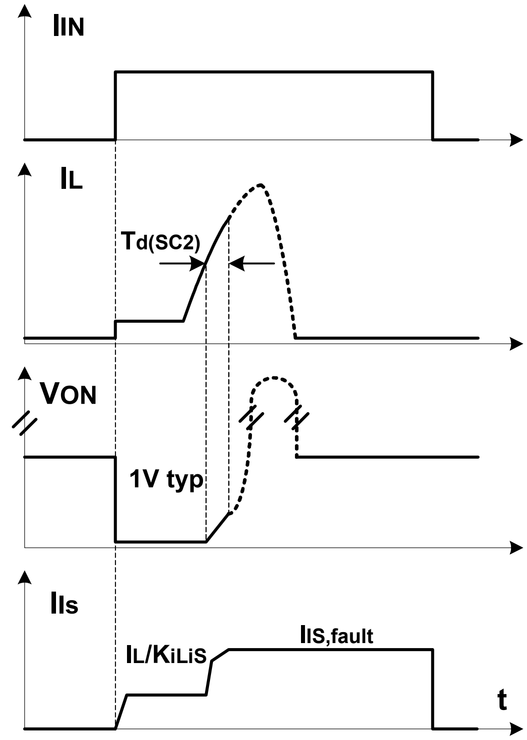


Figure 3c. Short circuit tpye two:
shut down by short circuit detection, reset by IIN=0

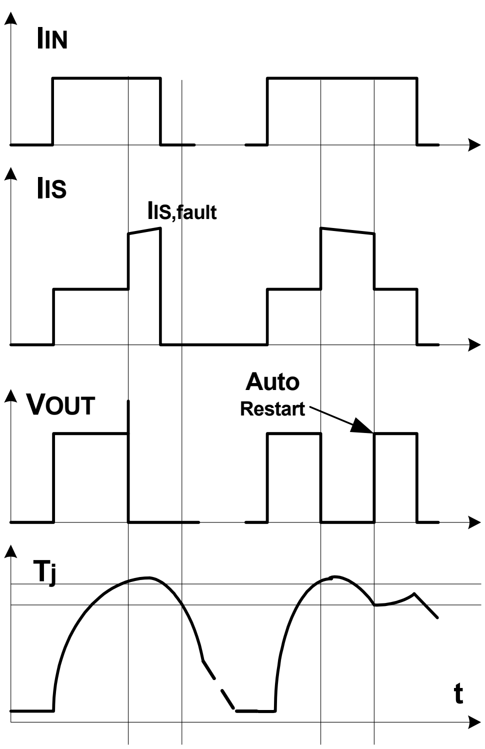


Figure 4a. Overtemperature Reset if Tj < Tjt

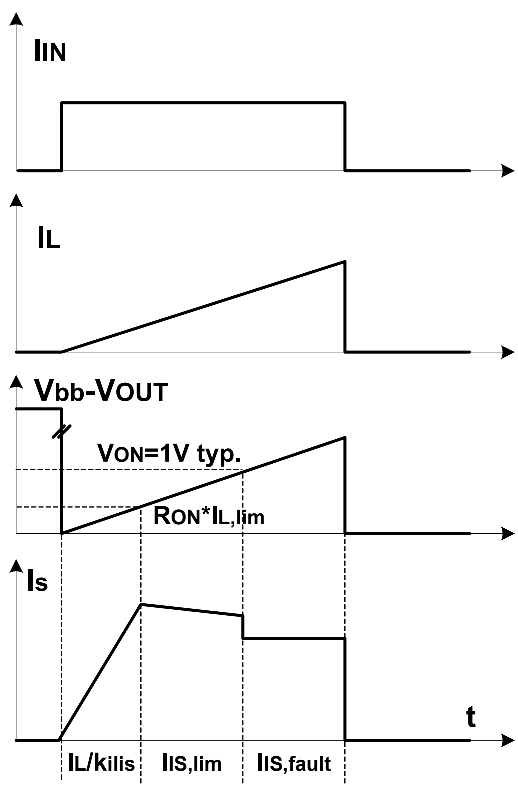


Figure 4b. Overload Reset if Tj < Tjt

3.VB Drop Voltage Diagram

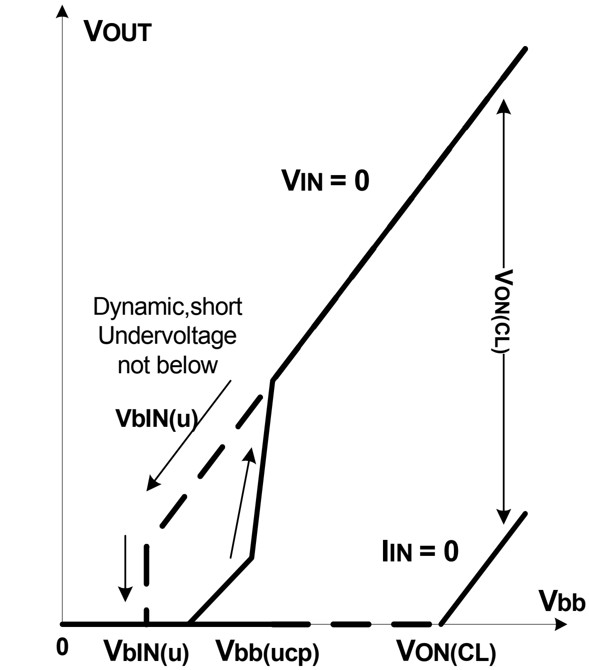


Figure 5. Undervoltage restart of charge pump overvoltage clamp

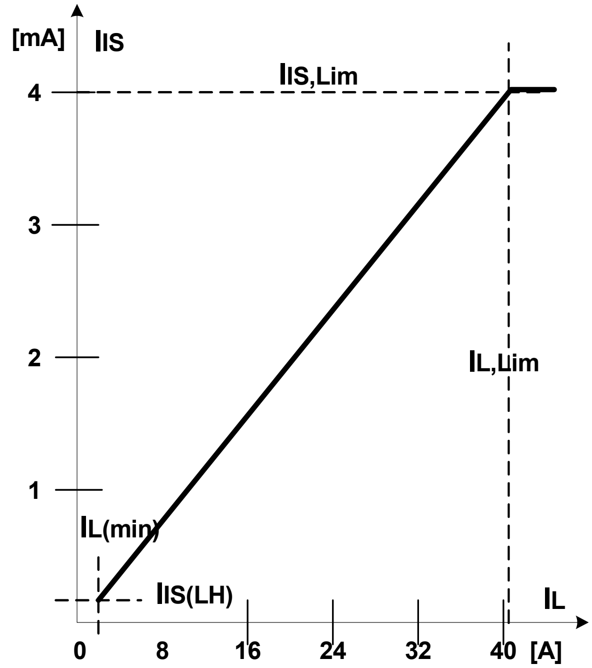


Figure 6a. Current sense versus load current

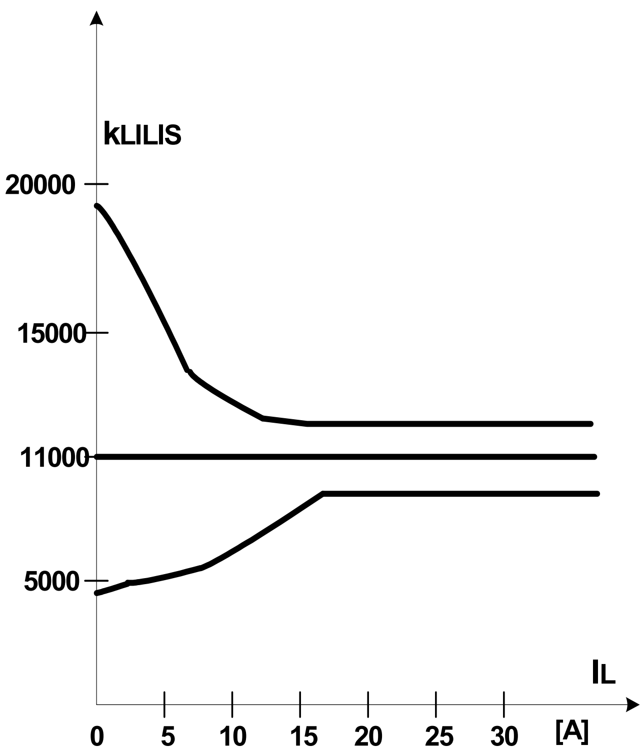


Figure 6b. Current sense ratio

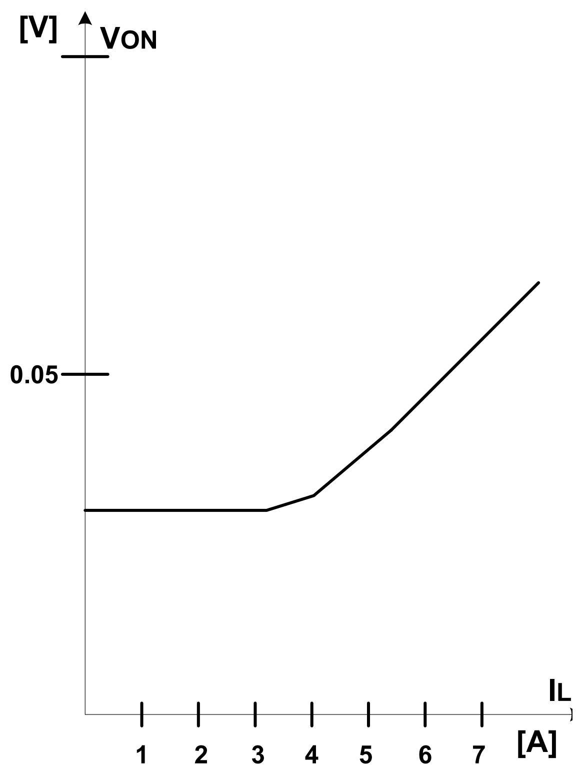
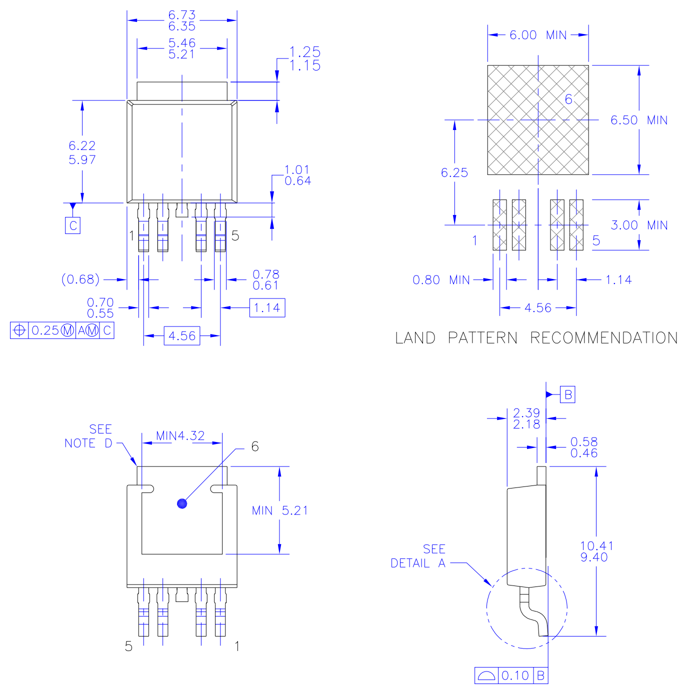


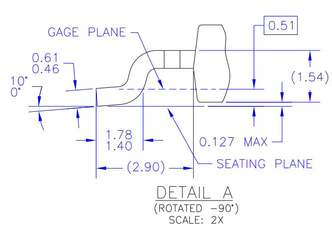
Figure 7. Output voltage drop versus load current

Package Dimensions

REVISIONS

LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
0	RELEASE TO DOCUMENT CONTROL	-	05APR2006	OS.JEON





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- A) THIS PACKAGE CONFORMS TO JEDEC, TO-252 ISSUE E, VARIATION AD, DATED JUNE. 2004.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- D) HEAT SINK TOP EDGE COULD BE IN CHAMFERD CORNERS OR EDGE PROTRUSION.
- E) DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994

APPROVALS	DATE
DRAWN: S. W LIM	05APR2006
CHECKED: S. W LIM	
APPROVED: M.K JONG	
O.S JEON	

FAIRCHILD SEMICONDUCTOR™ BUCHEON KOREA

TO-252 MOLDED, 5LD
JEDEC TO-252, AD

PROJECTION: INCH [MM]
SCALE: 1:1 | SIZE: N/A | DRAWING NUMBER: MKT- | REV: 0
FORMERLY: N/A | SHEET : 1 OF 1

FILE NAME

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