

PLL Clock Generator ICs with Built-In Divider/Multiplier Circuits

GENERAL DESCRIPTION

The XC25BS7 series are high frequency, low power consumption PLL clock generator ICs with divider circuit & multiplier PLL circuit. Laser trimming gives the option of being able to select from input divider ratios (M) of 1 to 256 and output divider ratios (N) of 1 to 256. Output frequency (fQ0) is equal to reference clock oscillation (fCLKin) multiplied by N/M, within a range of 1MHz to 100MHz. Further, frequency within a range of 32kHz to 36MHz can be inputted as a reference clock. The IC stops operation when low level signal is inputted to the CE pin. For this, consumption current can be reduced and output will be one of high-impedance. Because the series is semi-custom, please ask Torex sales contacts for your requested specifications such as input/output frequency, supply voltage. However, the series has the limit of specifications; therefore, your request may not be fully satisfied with your requested frequency range.

APPLICATIONS

- Clock for controlling a Imaging dot Microcomputer and HDD drives
- Cordless phones
- Wireless communication equipment
- PDA's
- Cameras, VCRs
- Various system clocks

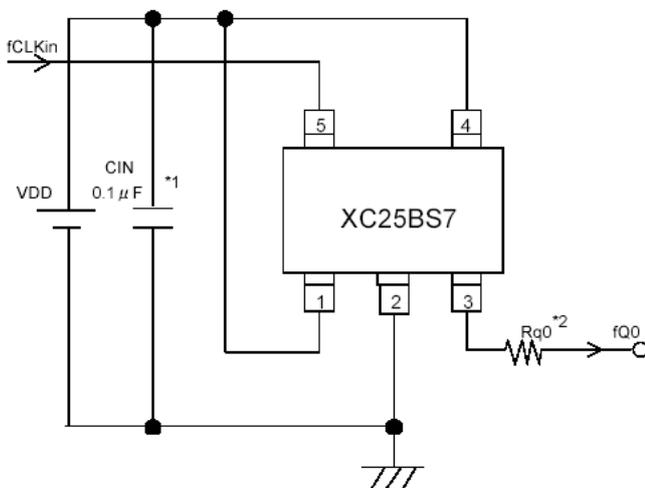
FEATURES

- Input Frequency : 32kHz ~ 36MHz ^{(*)1}
- Output Frequency : 1MHz ~ 100MHz
(fQ0=fCLKin × N/M) ^{(*)1}
- Output Divider (N) : Selectable from divisions from 1 to 256 ^{(*)1}
- Input Divider (M) : Selectable from divisions from 1 to 256 ^{(*)1}
- Operating Voltage Range : 2.50V ~ 5.50V ^{(*)1}
- Low Power Consumption : CMOS with stand-by function ^{(*)2}
(10μA, MAX. when stand-by)
- Packages : SOT-25, USP-6C
- Environmentally Friendly : EU RoHS Compliant, Pb Free

*1: The series are semi-custom products. Specifications for each product are limited within the above range. The input frequency range is set within ±5% of customer's designated typical frequency.

*2: When the IC is in stand-by mode, the output becomes high impedance and the IC stops operation.

TYPICAL APPLICATION CIRCUIT

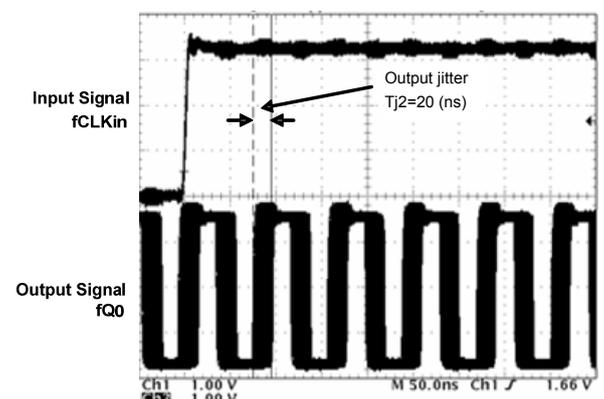


*1: C_{IN} (by-pass capacitor, 0.1 μF) should be connected to the IC as close as possible.

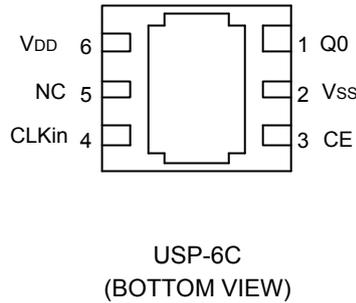
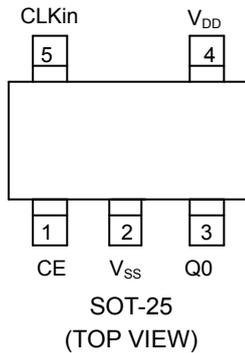
*2: R_{q0} is a resistor for unwanted radiation only to use when needed.

TYPICAL PERFORMANCE CHARACTERISTICS

PLL output signal jitter 2 (equivalent to an input signal)
XC25BS7001xx (256 multiplier, Input 48kHz, TYP.)



PIN CONFIGURATION



* The dissipation pad (TAB) of the bottom view of the USP-6C package should be connected to the V_{SS} (No. 2) pin.

PIN ASSIGNMENT

PIN NUMBER		PIN NAME	FUNCTION
SOT-25	USP-6C		
3	1	Q0	Clock Output
2	2	V_{SS}	Ground
1	3	CE	Stand-by Control
5	4	CLKin	Reference Clock Signal Input
-	5	NC	No Connection
4	6	V_{DD}	Power Input

FUNCTION LIST

CE	'H'	'L' or OPEN
Q0	Signal Output	High Impedance

H: High level input

L: Low level input (stand-by mode)

PRODUCT CLASSIFICATION

Ordering Information

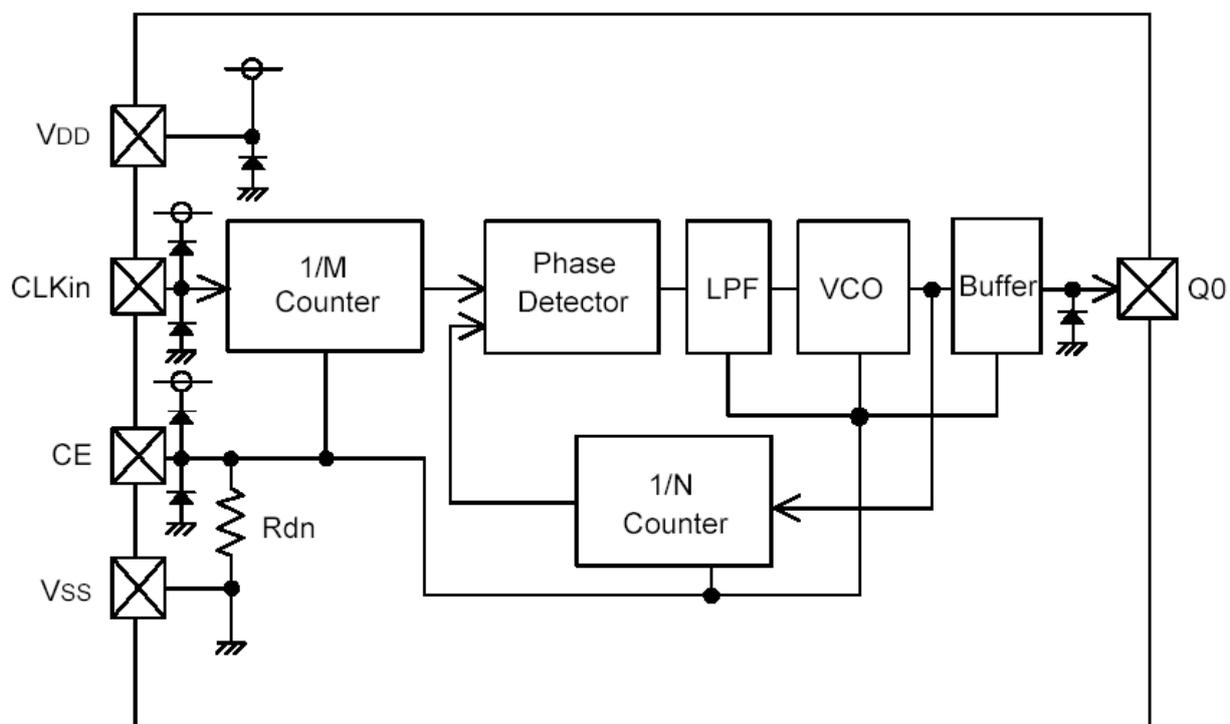
XC25BS7 - (*)

DESIGNATOR	DESCRIPTION	SYMBOL	DESCRIPTION
	Product Number	Integer	Based on internal standards e.g. product number 001 =001
	Packages Taping Type (*)	MR	SOT-25
		MR-G	SOT-25
		ER	USP-6C
		ER-G	USP-6C

(*) The "-G" suffix indicates that the products are Halogen and Antimony free as well as being fully RoHS compliant.

(*) The device orientation is fixed in its embossed tape pocket. For reverse orientation, please contact your local Torex sales office or representative. (Standard orientation: R- , Reverse orientation: L-)

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Ta=25

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V _{DD}	V _{SS} - 0.3 ~ V _{SS} + 7.0	V
CLKIn Pin Input Voltage	V _{CK}	V _{SS} - 0.3 ~ V _{DD} + 0.3	V
CE Pin Input Voltage	V _{CE}	V _{SS} - 0.3 ~ V _{DD} + 0.3	V
Q0 Pin Output Voltage	V _{Q0}	V _{SS} - 0.3 ~ V _{DD} + 0.3	V
Q0 Pin Output Current	I _{Q0}	± 50	mA
Power Dissipation	SOT-25	150	mW
	USP-6C	100	mW
Operating Temperature Range	T _{opr}	-40 ~ +85	°C
Storage Temperature Range	T _{stg}	-55 ~ +125	°C

ELECTRICAL CHARACTERISTICS

Characteristics example by product series

- *1: The chart below introduces the products with typical specification characteristics which is under production or production in the past.
- *2: The series are semi-custom products. Specifications for each product are limited within the range below. The input frequency is set within $\pm 5\%$ of customer's designated typical frequency.
- *3: For other part number with other input-output frequency or multiplication, please ask Torex sales contacts.

XC25BS7001xx (256 multiplication)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input Frequency	fCLKin	-	48.000	-	kHz
Multiplier/Divider Ratio	N/M	-	256	-	Multiplier
PLL Output Frequency	fQ0	-	12.288	-	MHz

XC25BS7007xx (0.333 multiplication)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input Frequency	fCLKin	-	16.9344	-	MHz
Multiplier/Divider Ratio	N/M	-	0.333	-	Multiplier
PLL Output Frequency	fQ0	-	5.6448	-	MHz

XC25BS7008xx (256 multiplication)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input Frequency	fCLKin	-	44.000	-	kHz
Multiplier/Divider Ratio	N/M	-	256	-	Multiplier
PLL Output Frequency	fQ0	-	11.264	-	MHz

XC25BS7012xx (256 multiplication)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input Frequency	fCLKin	-	92.000	-	kHz
Multiplier/Divider Ratio	N/M	-	256	-	Multiplier
PLL Output Frequency	fQ0	-	23.552	-	MHz

XC25BS7013xx (128 multiplication)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input Frequency	fCLKin	-	184.000	-	kHz
Multiplier/Divider Ratio	N/M	-	128	-	Multiplier
PLL Output Frequency	fQ0	-	23.552	-	MHz

ELECTRICAL CHARACTERISTICS (Continued)

Recommended Operating Conditions: XC25BS7001xx (256 multiplication, Input 48kHz (TYP.)) 3.3V (TYP.)

Tested below $T_a=25^{\circ}\text{C}$

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT
Supply Voltage	V_{DD}	3.3V (TYP.) operation	2.97	3.63	V
Input Frequency	f_{CLKin}	(^{*1})	45.000	60.000	kHz
Multiplier/Divider Ratio	N/M	Typical value is shown (^{*1})	256		-
Output Frequency	f_{Q0}	(^{*1})	11.520	15.360	MHz
Capacity Overload (^{*3})	CL		-	15	pF
Output Start Time (^{*2})(^{*3})	t_{START}	$f_{CLKin}=45\text{kHz}$	0.05	20	ms

NOTE:

*1: Connected $C_{IN}=0.1\ \mu\text{F}$ of a ceramic capacitor between the V_{DD} pin the V_{SS} pin while testing.

*2: Time until signal via the Q0 pin flows stably from applying supply voltage to the V_{DD} pin and control voltage to the CE pin while applying the input signal to the CLKin pin.

*3: The value indicated at output start time is designed values which are not guaranteed values.

DC Characteristics: XC25BS7001xx (256 multiplication, Input 48kHz (TYP.)) 3.3V (TYP.)

Test Conditions: $V_{DD}=3.3\text{V}$, $f_{CLKin}=48\text{kHz}$, Multiplier ratio=256, $T_a=25$, No Load

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	CIRCUIT
H Level Input Voltage	V_{IH}		2.70	-	-	V	①
L Level Input Voltage	V_{IL}		-	-	0.60	V	①
H Level Input Current	I_{IH}	$V_{CLKin}=V_{DD}-0.3\text{V}$	-	-	3.0	μA	②
L Level Input Current	I_{IL}	$V_{CLKin}=0.3\text{V}$	-3.0	-	-	μA	②
H Level Output Voltage	V_{OH}	$V_{DD}=2.97\text{V}$, $I_{OH}=-4\text{mA}$	2.50	-	-	V	③
L Level Output Voltage	V_{OL}	$V_{DD}=2.97\text{V}$, $I_{OL}=4\text{mA}$	-	-	0.40	V	③
Supply Current 1	I_{DD1}	$V_{DD}=3.63\text{V}$, $CE=3.63\text{V}$	-	3.0	6.0	mA	④
Supply Current 2	I_{DD2}	$V_{DD}=3.63\text{V}$, $CE=0.0\text{V}$	-	-	10	μA	④
CE H Level Voltage	V_{CEH}		2.70	-	-	V	①
CE L Level Voltage	V_{CEL}		-	-	0.45	V	①
CE Pull-Down Resistance 1	Rdn1	$CE=V_{DD}$	0.2	1.0	1.8	$\text{M}\Omega$	⑤
CE Pull-Down Resistance 2	Rdn2	$CE=0.1 \times V_{DD}$	10	30	60	$\text{k}\Omega$	⑤
Output Off Leak Current	I_{OZ}	$V_{DD}=Q0=3.63\text{V}$, $CE=0.0\text{V}$	-	-	10	μA	⑥

AC Characteristics: XC25BS7001xx (256 multiplication, Input 48kHz (TYP.)) 3.3V (TYP.)

Test Conditions: $V_{DD}=3.3\text{V}$, $f_{CLKin}=48\text{kHz}$, Multiplier ratio=256, $T_a=25$, $CL=15\text{pF}$

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	CIRCUIT
Output Rise Time (^{*1})	t_r	(20% ~ 80%)	-	2.5	5.0	ns	①
Output Fall Time (^{*1})	t_f	(20% ~ 80%)	-	2.5	5.0	ns	①
Output Signal Duty (^{*1})	Duty	$f_{Q0} \leq 60\text{MHz}$	45	50	55	%	①
		$f_{Q0} \geq 60\text{MHz}$	40	50	60	%	
PLL Output Signal Jitter 1 (^{*1})	t_{J1}	1σ (Output Period)	-	20	-	ps	①
PLL Output Signal Jitter 2 (^{*1})	t_{J2}	Peak to Peak (Output Tracking)	-	20	-	ns	①

NOTE:

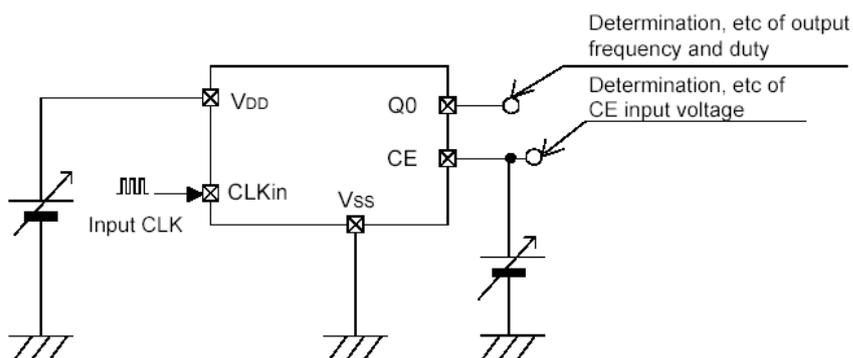
*1: Values indicated at the AC Characteristics are designing values, which are not guaranteed values.

NOTE ON USE

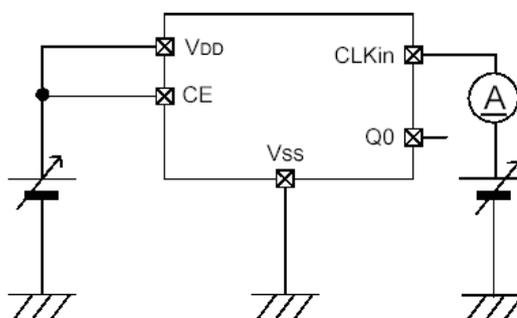
- (1) Please use this IC within the stated absolute maximum ratings. The IC is liable to malfunction should the ratings be exceeded.
- (2) The series is an analog IC. Please use a 0.01 μ F to 0.1 μ F of a by-pass capacitor.
- (3) Rq0 shown in the Typical Application Circuit is a matching resistor. The use is recommended in order to counter unwanted radiations.
- (4) Please place the by-pass capacitor and the matching resistor as close to the IC as possible. The IC may not operate normally if the by-pass capacitor is not close enough to the IC. Further, the unwanted radiation may occur between the resistor and the IC pin if the matching resistor is not close enough to the IC.
- (5) When the CE pin is not controlled by external signals, it is recommended that a time constant circuit of $R1=1k \times C1 = 0.1 \mu F$ be added for stability.
- (6) With this IC, output is achieved by dividing and multiplying the reference oscillation by means of the PLL circuit. In cases where this output is further used as a reference oscillation of another PLL circuit, it may be that the final output signal's jitter increases; therefore, all necessary precautions should be taken to avoid this.
- (7) It is recommended that a low noise power supply, such as a series regulator, be used as the series' supply voltage. Using a power supply such as a switching regulator may enlarge the jitter, which in turn may lead to abnormal operation. Please confirm its operation with the actual device.
- (8) For operating the IC normally, please take procedures below when applying voltage to the series' input pin:
 - 1) Apply power source while the CE pin is "L" level with no clock input (high-Impedance or "L"),
 - 2) Input the clock,
 - 3) At least 100 μ s after applying clock input, change the CE pin into "H" level.The IC has to be started by inputting the clock once the power rises completely. The CE pin, then, should be enabling. If the CE pin becomes enable and the clock is inputted before the power rises completely, an internal reset circuit does not operate normally which may cause to generate extraneous frequency.
- (9) As for this IC, synchronization of input and output signals occurs at the rising edge.

TEST CIRCUIT

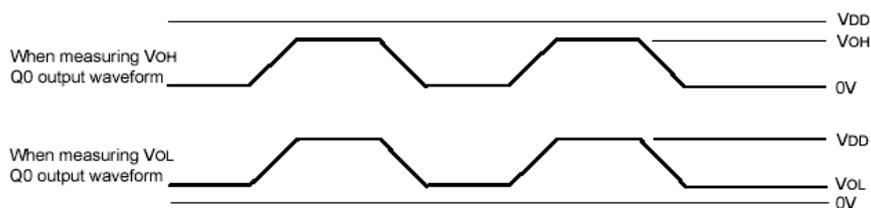
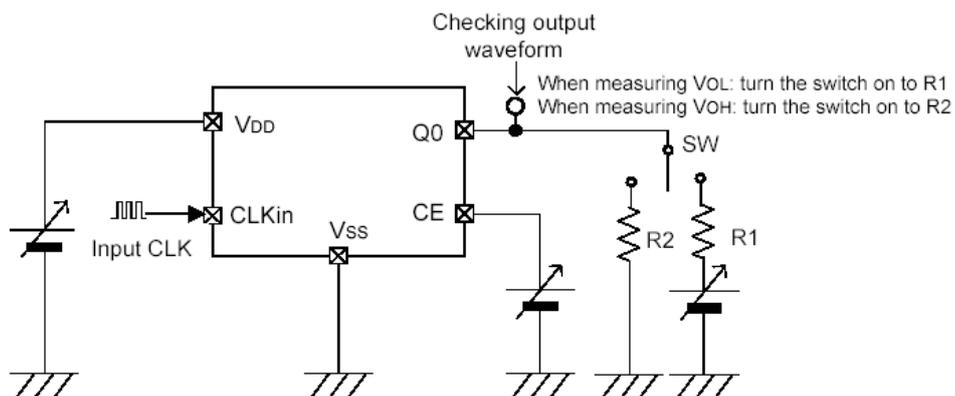
Operating Supply Voltage
 H Level Input Voltage
 L Level Input Voltage
 CE "H" Level Voltage
 CE "L" Level Voltage
 Output Rise Time
 Output Fall Time
 Output Signal Duty
 PLL Output Signal Jitter



H Level Input Current
 L Level Input Current



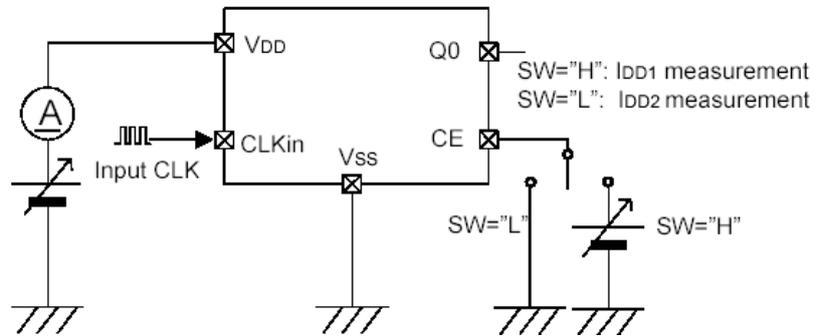
H Level Output Voltage
 L Level Output Voltage



TEST CIRCUIT (Continued)

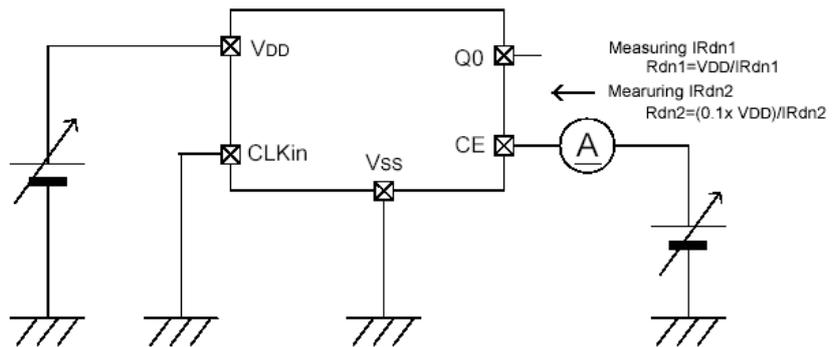
Supply Current 1

Supply Current 2

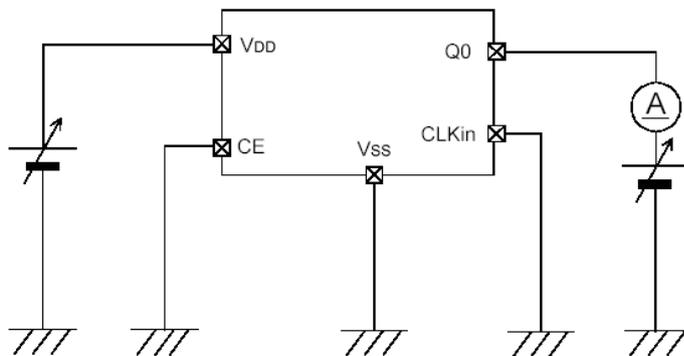


CE Pull-Down Resistance 1

CE Pull-Down Resistance 2

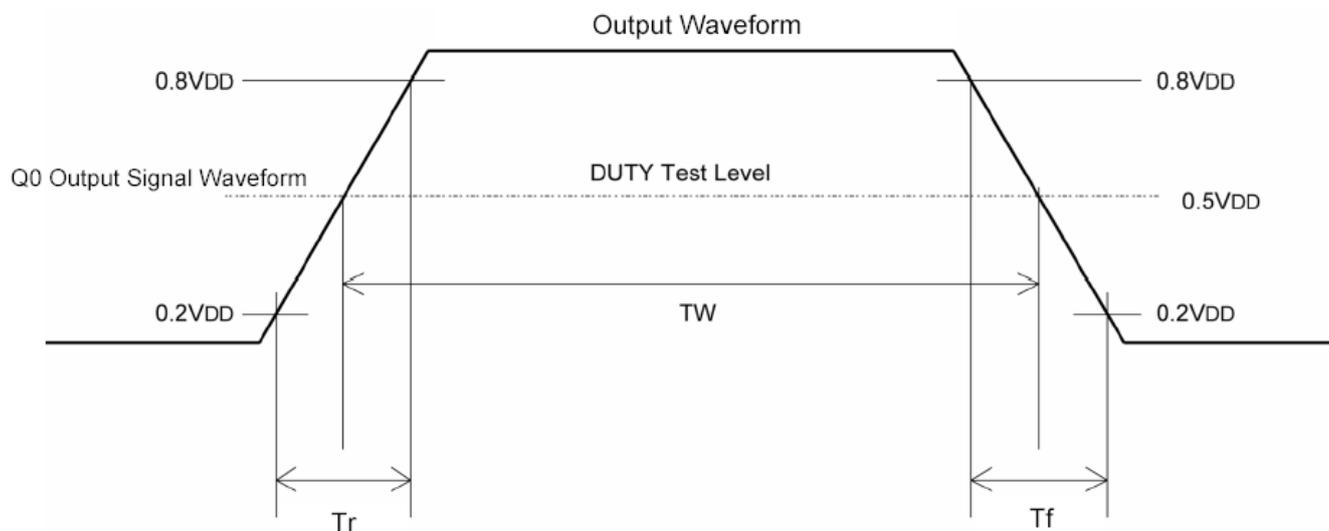


Output Off Leak Current

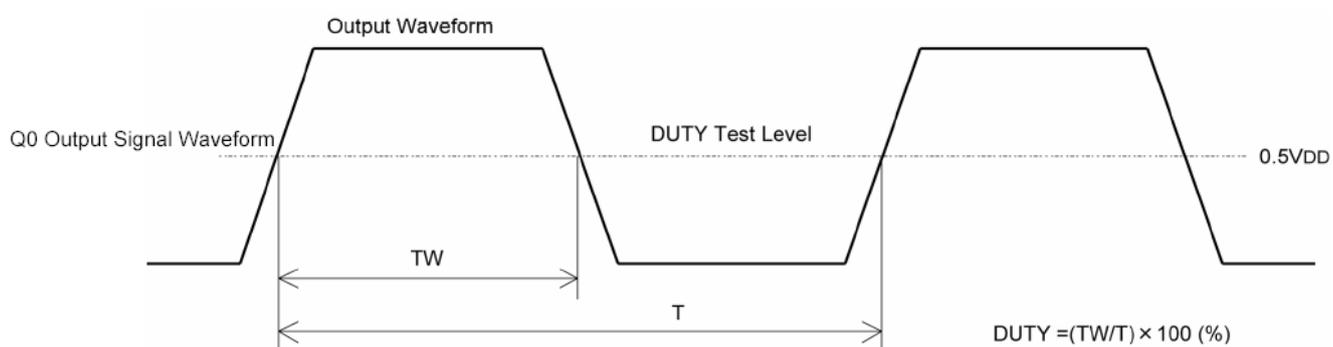


AC CHARACTERISTICS TEST WAVEFORM

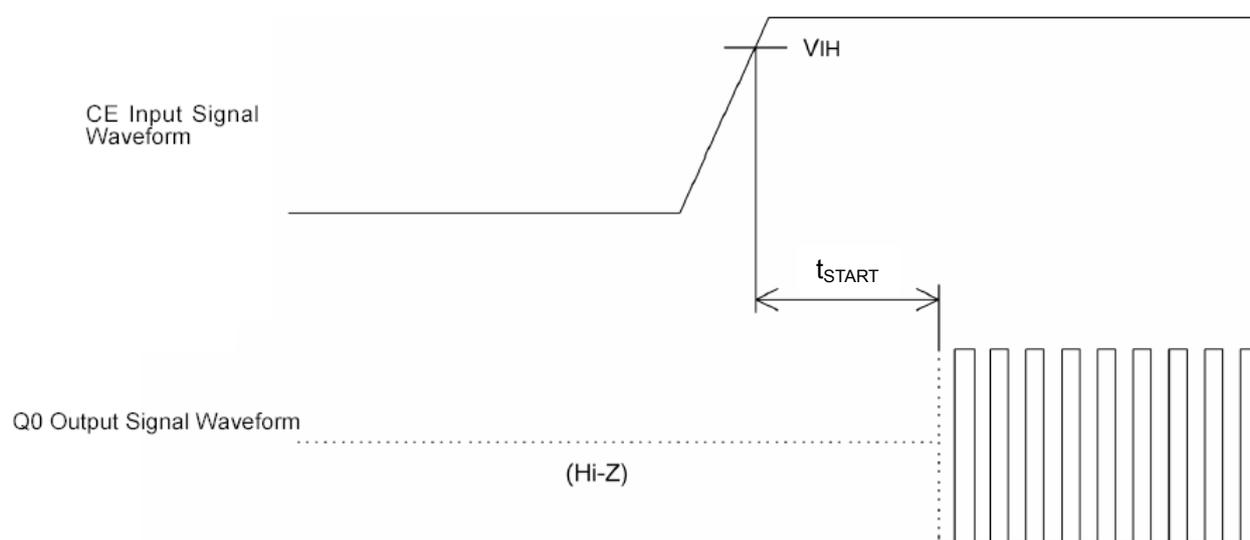
1) Output Rise Time, Output Fall Time



2) Duty Ratio



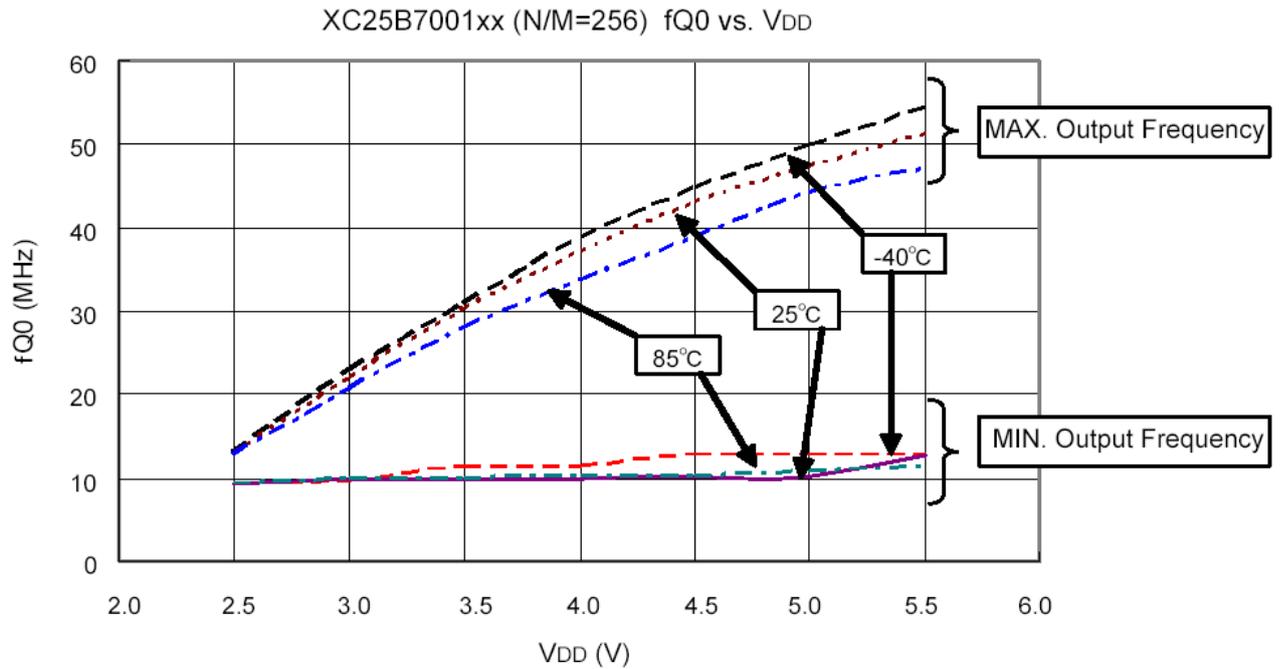
3) Output Start Time



TYPICAL PERFORMANCE CHARACTERISTICS

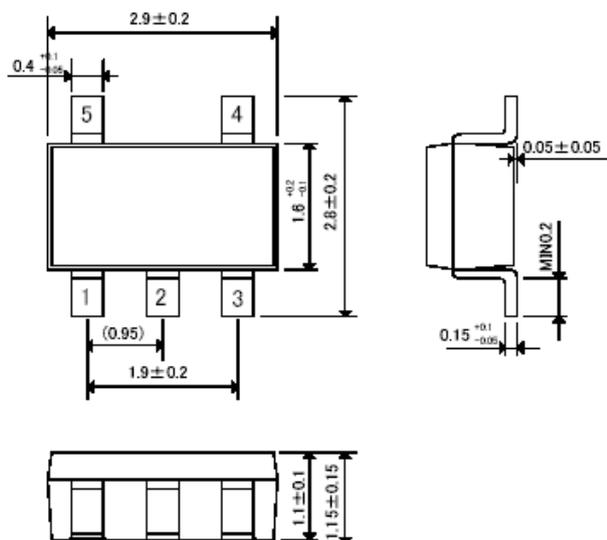
Output Frequency Range (Capable of Synchronous) vs. Supply Voltage

XC25BS7001xx (256 multiplication, Input 48kHz (TYP.))

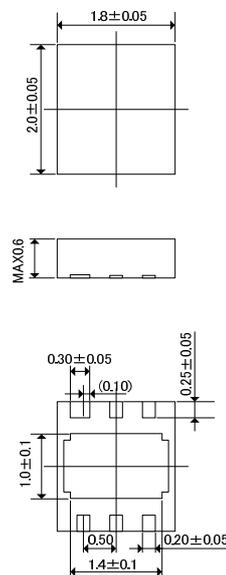


PACKAGE INFORMATION

SOT-25



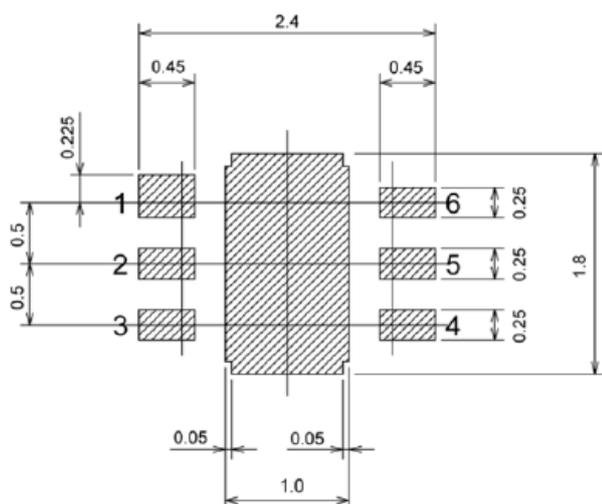
USP-6C



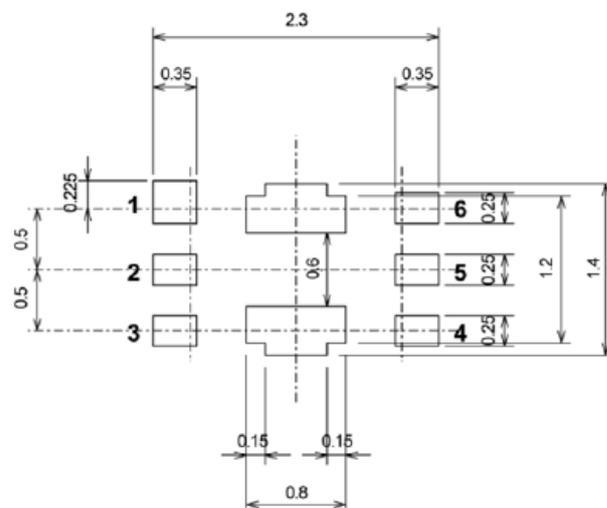
USP-6C Package

* No. 1 pin is larger than the other pins.
Soldering fillet surface is not formed because the sides of the pins are not plated.

USP-6C Reference Mount Pattern

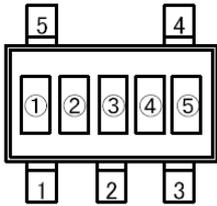


USP-6C Reference Metal Masking



MARKING RULE

SOT-25



SOT-25
(TOP VIEW)

and represent product series.

MARK		PRODUCT SERIES
	②	
B	7	XC25BS70**M*
7	S	XC25BS7S**M*

represents the serial number corresponding to the part number 『b』, 『c』.

* The serial numbers after the 99 are repeated as shown below for and .

MARK	『b』	『c』	PART NUMBER	MARK	『b』	『c』	PART NUMBER
1	0	1	XC25BS7*01M*	K	1	7	XC25BS7*17M*
2	0	2	XC25BS7*02M*	L	1	8	XC25BS7*18M*
3	0	3	XC25BS7*03M*	M	1	9	XC25BS7*19M*
4	0	4	XC25BS7*04M*	N	2	0	XC25BS7*20M*
5	0	5	XC25BS7*05M*	P	2	1	XC25BS7*21M*
6	0	6	XC25BS7*06M*	R	2	2	XC25BS7*22M*
7	0	7	XC25BS7*07M*	S	2	3	XC25BS7*23M*
8	0	8	XC25BS7*08M*	T	2	4	XC25BS7*24M*
9	0	9	XC25BS7*09M*	U	2	5	XC25BS7*25M*
A	1	0	XC25BS7*10M*	V	2	6	XC25BS7*26M*
B	1	1	XC25BS7*11M*	X	2	7	XC25BS7*27M*
C	1	2	XC25BS7*12M*	Y	2	8	XC25BS7*28M*
D	1	3	XC25BS7*13M*	Z	2	9	XC25BS7*29M*
E	1	4	XC25BS7*14M*	<u>1</u>	3	0	XC25BS7*30M*
F	1	5	XC25BS7*15M*	<u>2</u>	3	1	XC25BS7*31M*
H	1	6	XC25BS7*16M*	:	:	:	:

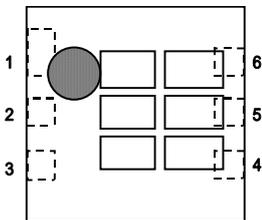
and represents production lot number

01,...09,10,11,...,99, 0A,...,0Z,1A,...,9Z,A0,...,Z9,AA,...,ZZ are used in series.

(G, I, J, O, Q, and W are excluded from the serial numbers.)

* Inverted characters are not used.

USP-6C



USP-6C
(TOP VIEW)

, and represents product series

MARK			PRODUCT SERIES
B	S	7	XC25BS70**E*
S	7	S	XC25BS7S**E*

and represents product serial numbers (= 『b』, = 『c』)

MARK	MARK	PART NUMBER
『b』	『c』	
0	1	XC25BS7001E*
0	2	XC25BS7S02E*
:	:	:

represents production lot number

0 ~ 9, A ~ Z repeated (G, I, J, O, Q, and W are excluded from the serial numbers)

* Inverted characters are not used.

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