

### **General Description**

The MAX5965A/MAX5965B are guad, monolithic, -48V power controllers designed for use in IEEE® 802.3af-compliant/IEEE 802.3at-compatible power-sourcing equipment (PSE). These devices provide powered device (PD) discovery, classification, current limit, DC and AC load disconnect detections in compliance with the IEEE 802.3af standard. The MAX5965A/MAX5965B are pin compatible with the MAX5952/MAX5945/LTC4258/LTC4259A PSE controllers and provide additional features.

The MAX5965A/MAX5965B feature a high-power mode that provides up to 45W per port. The MAX5965A/ MAX5965B provide new Class 5 and 2-event classification (Class 6) for detection and classification of highpower PDs. The MAX5965A/MAX5965B provide instantaneous readout of each port current through the I<sup>2</sup>C interface. The MAX5965A/MAX5965B also provide high-capacitance detection for legacy PDs.

These devices feature an I<sup>2</sup>C-compatible, 3-wire serial interface, and are fully software configurable and programmable. The class-overcurrent detection function enables system power management to detect if a PD draws more than the allowable current. The MAX5965A/MAX5965B's extensive programmability enhances system flexibility, enables field diagnosis, and allows for uses in other applications.

The MAX5965A/MAX5965B provide four operating modes to suit different system requirements. Auto mode allows the devices to operate automatically without any software supervision. Semi-automatic mode automatically detects and classifies a device connected to a port after initial software activation, but does not power up that port until instructed to by software. Manual mode allows total software control of the device and is useful for system diagnostics. Shutdown mode terminates all activities and securely turns off power to the ports.

The MAX5965A/MAX5965B provide input undervoltage lockout (UVLO), input undervoltage detection, a loadstability safety check during detection, input overvoltage lockout, overtemperature detection, output voltage slew-rate limit during startup, power-good status, and fault status. The MAX5965A/MAX5965B's programmability includes startup timeout, overcurrent timeout, and load-disconnect detection timeout.

The MAX5965A/MAX5965B are available in a 36-pin SSOP package and are rated for both extended (-40°C to +85°C) and upper commercial (0°C to +85°C) temperature ranges.

### **Applications**

Power-Sourcing Equipment (PSE) Switches/Routers

Midspan Power Injectors

MIXIM

**Features** 

- ♦ IEEE 802.3af Compliant/IEEE 802.3at Compatible
- ♦ Instantaneous Readout of Port Current Through I<sup>2</sup>C Interface
- ♦ High-Power Mode Enables Up to 45W Per Port
- **♦** High-Capacitance Detection for Legacy Devices
- ♦ Pin Compatible with MAX5952/MAX5945/ LTC4258/LTC4259A
- **♦** Four Independent Power-Switch Controllers
- ◆ PD Detection and Classification (Including 2-**Event Classification**)
- ♦ Selectable Load-Stability Safety Check During Detection
- ♦ Supports Both DC and AC Load Removal **Detections**
- ♦ I<sup>2</sup>C-Compatible, 3-Wire Serial Interface
- ♦ Current Foldback and Duty-Cycle-Controlled **Current Limit**
- ♦ Open-Drain INT Signal
- **♦ Direct Fast Shutdown Control Capability**
- ♦ Special Class 5 Classification

### **Ordering Information**

| PART          | TEMP RANGE     | PIN-PACKAGE |
|---------------|----------------|-------------|
| MAX5965AEAX+  | -40°C to +85°C | 36 SSOP     |
| MAX5965AUAX+* | 0°C to +85°C   | 36 SSOP     |
| MAX5965BEAX+  | -40°C to +85°C | 36 SSOP     |
| MAX5965BUAX+* | 0°C to +85°C   | 36 SSOP     |

<sup>+</sup>Denotes a lead(Pb)-free/RoHS-compliant package.

### **Selector Guide**

| PART         | PIN-PACKAGE | AC DISCONNECT<br>FEATURE |
|--------------|-------------|--------------------------|
| MAX5965AEAX+ | 36 SSOP     | No                       |
| MAX5965AUAX+ | 36 SSOP     | No                       |
| MAX5965BEAX+ | 36 SSOP     | Yes                      |
| MAX5965BUAX+ | 36 SSOP     | Yes                      |

Pin Configuration appears at end of data sheet.

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<sup>\*</sup>Future product—contact factory for availability.

#### ABSOLUTE MAXIMUM RATINGS

| (Voltages referenced to $V_{EE,}$ unless other AGND, DGND, DET_, $V_{DD}$ , $\overline{RESET}$ , A3-A |                      |
|---|----------------------|
| SCL, SDAIN, AUTO  | 0.3V to +80V         |
| OUT   | 12V to (AGND + 0.3V) |
| GATE_ (internally clamped) (Note 1)   | 0.3V to +11.4V       |
| SENSE   |                      |
| V <sub>DD</sub> , RESET, MIDSPAN, A3-A0, SHD_, O  |                      |
| SDAIN and AUTO to DGND  | 0.3V to +7V          |
| INT and SDAOUT to DGND  | 0.3V to +12V         |
| Maximum Current into INT, SDAOUT, DE  | Γ80mA                |
|   |                      |

| Maximum Power Dissipation (TA       | $t = +70^{\circ}C$      |
|-------------------------------------|-------------------------|
| 36-Pin SSOP (derate 17.4mW/         | °C above +70°C)1388.9mW |
| <b>Operating Temperature Ranges</b> |                         |
| MAX5965A/MAX5965B_EAX               | 40°C to +85°C           |
| MAX5965A/MAX5965B_UAX               | 0°C to +85°C            |
| Storage Temperature Range           | 65°C to +150°C          |
| Junction Temperature                | +150°C                  |
| Lead Temperature (soldering, 1      | 0s)+300°C               |
| Soldering Temperature (reflow).     | +260°C                  |
|                                     |                         |

Note 1: GATE\_ is internally clamped to 11.4V above VEE. Driving GATE\_ higher than 11.4V above VEE may damage the device.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### **ELECTRICAL CHARACTERISTICS**

 $(V_{AGND} = 32V \text{ to } 60V, V_{EE} = 0V, V_{DD} \text{ to } V_{DGND} = +3.3V, \text{ all voltages are referenced to } V_{EE}, \text{ unless otherwise noted.}$  Typical values are at  $V_{AGND} = +48V, V_{DGND} = +48V, V_{DGND} = (V_{DGND} + 3.3V), T_{A} = +25^{\circ}C.$  Currents are positive when entering the pin and negative otherwise.) (Note 2)

| PARAMETER                   | SYMBOL            | CONDITIONS  | MIN | TYP | MAX  | UNITS |
|-----------------------------|-------------------|---|-----|-----|------|-------|
| POWER SUPPLIES              |                   |   |     |     |      |       |
|                             | Vagnd             | VAGND - VEE   | 32  |     | 60   |       |
| Operating Valtage Dange     | V <sub>DGND</sub> |   | 0   |     | 60   | V     |
| Operating Voltage Range     | \/pp              | V <sub>DD</sub> to V <sub>DGND</sub> , V <sub>DGND</sub> = V <sub>AGND</sub>  | 2.4 |     | 3.6  | V     |
|                             | V <sub>DD</sub>   | V <sub>DD</sub> to V <sub>DGND</sub> , V <sub>DGND</sub> = V <sub>EE</sub>  | 3.0 |     | 3.6  |       |
| Supply Currents             | lee               | VOUT_ = VEE, VSENSE_ = VEE, DET_ = AGND, all logic inputs open, SCL = SDAIN = VDD.  INT and SDAOUT unconnected. Measured at AGND in power mode after GATE_ pullup |     | 4.8 | 6.8  | mA    |
|                             | I <sub>DIG</sub>  | All logic inputs high, measured at V <sub>DD</sub>  |     | 0.2 | 0.4  |       |
| GATE DRIVER AND CLAMPING    | G                 |   |     |     |      |       |
| GATE_ Pullup Current        | I <sub>PU</sub>   | Power mode, gate drive on, VGATE_ = VEE (Note 3)  | -40 | -50 | -65  | μΑ    |
| Weak GATE_ Pulldown Current | I <sub>PDW</sub>  | SHD_ = DGND, V <sub>GATE</sub> _ = V <sub>EE</sub> + 10V  |     | 42  |      | μΑ    |
| Maximum Pulldown Current    | IPDS              | VSENSE_ = 600mV, VGATE_ = VEE + 2V  |     | 100 |      | mA    |
| External Gate Drive         | V <sub>G</sub> S  | VGATE VEE, power mode, gate drive on, IPU = 1µA   | 9   | 10  | 11.5 | V     |

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### **ELECTRICAL CHARACTERISTICS (continued)**

 $(V_{AGND} = 32V \text{ to } 60V, V_{EE} = 0V, V_{DD} \text{ to } V_{DGND} = +3.3V, \text{ all voltages are referenced to } V_{EE}, \text{ unless otherwise noted.}$  Typical values are at  $V_{AGND} = +48V, V_{DGND} = +48V, V_{DD} = (V_{DGND} + 3.3V), T_{A} = +25^{\circ}C.$  Currents are positive when entering the pin and negative otherwise.) (Note 2)

| PARAMETER                                   | SYMBOL               | CONDITIONS   |  | MIN | TYP | MAX | UNITS |
|---|----------------------|--|--|-----|-----|-----|-------|
| CURRENT LIMIT                               |                      |  |  |     |     |     |       |
|   |                      |  | IVEE = 00                                | 202 | 212 | 220 |       |
|   |                      | Maximum V <sub>SENSE</sub> allowed   | IVEE = 01                                | 192 | 202 | 212 |       |
| Current-Limit Clamp Voltage                 | V <sub>SU_LIM</sub>  | during current limit, V <sub>OUT</sub> = 0V (ICUT = 000) (Note 4)  | IVEE = 10                                | 186 | 190 | 200 | mV    |
|   |                      |  | IVEE = 11                                | 170 | 180 | 190 |       |
| Overcurrent Threshold After Startup         |                      |  | ICUT = 000<br>(Class 0/3)                | 177 | 186 | 196 |       |
|   |                      |  | ICUT = 110<br>(Class 1)                  | 47  | 55  | 64  | mV    |
|   | VFLT_LIM             | Overcurrent V <sub>SENSE_</sub> threshold allowed for t ≤ t <sub>FAULT</sub> after startup; V <sub>OUT_</sub> = 0V (IVEE = 00)   | ICUT = 111<br>(Class 2)                  | 86  | 94  | 101 |       |
|   |                      |  | ICUT = 001                               | 265 | 280 | 295 |       |
|   |                      |  | ICUT = 010                               | 310 | 327 | 345 |       |
|   |                      |  | ICUT = 011                               | 355 | 374 | 395 |       |
|   |                      |  | ICUT = 100                               | 398 | 419 | 440 |       |
|   |                      |  | ICUT = 101                               | 443 | 466 | 488 |       |
| Foldback Initial OUT_ Voltage               | V <sub>FLBK_ST</sub> | VOUT VEE, above which the current-limit trip voltage starts  | ICUT = 000,<br>ICUT = 110,<br>ICUT = 111 |     | 32  |     | V     |
|   |                      | folding back, IVEE = 00  | ICUT = 001101                            |     | 13  |     |       |
| Foldback Final OUT_ Voltage                 | VFLBK_END            | IVEE = 00, ICUT = 000, V <sub>OUT</sub> - V <sub>EE</sub> above which the current-limit trip voltage reaches V <sub>TH</sub> _FB |  |     | 50  |     | V     |
| Minimum Foldback<br>Current-Limit Threshold | V <sub>TH_FB</sub>   | V <sub>OUT</sub> _ = AGND = 60V, IVEE = 00, ICUT = 000   |  |     | 64  |     | mV    |
| SENSE_ Input Bias Current                   |                      | VSENSE_ = VEE  |  | -5  |     | +5  | μΑ    |

### **ELECTRICAL CHARACTERISTICS (continued)**

 $(V_{AGND} = 32V \text{ to } 60V, V_{EE} = 0V, V_{DD} \text{ to } V_{DGND} = +3.3V, \text{ all voltages are referenced to } V_{EE}, \text{ unless otherwise noted.}$  Typical values are at  $V_{AGND} = +48V, V_{DGND} = +48V, V_{DD} = (V_{DGND} + 3.3V), T_{A} = +25^{\circ}C.$  Currents are positive when entering the pin and negative otherwise.) (Note 2)

| PARAMETER  | SYMBOL              | CONDITIONS   | MIN  | TYP  | MAX | UNITS |
|--|---------------------|--|------|------|-----|-------|
| SUPPLY MONITORS                                    | •                   | ·  | •    |      |     | •     |
| VEE Undervoltage Lockout                           | VEEUVLO             | VAGND - VEE, VAGND - VEE increasing  |      | 28.5 |     | V     |
| V <sub>EE</sub> Undervoltage Lockout<br>Hysteresis | VEEUVLOH            | Ports shut down if V <sub>AGND</sub> - V <sub>EE</sub> < V <sub>UVLO</sub> - V <sub>EE</sub> UVLOH                           |      | 3    |     | V     |
| VEE Overvoltage Lockout                            | V <sub>EE</sub> _OV | VEE_OV event bit sets and ports shut down if VAGND - VEE > VEE_OV, VAGND increasing  |      | 62.5 |     | V     |
| V <sub>EE</sub> Overvoltage Lockout<br>Hysteresis  | Vovh                |  |      | 1    |     | V     |
| V <sub>EE</sub> Undervoltage                       | V <sub>EE_UV</sub>  | VEE_UV event bit is set if VAGND - VEE < VEE_UV, VEE increasing  |      | 40   |     | V     |
| V <sub>DD</sub> Overvoltage                        | V <sub>DD_OV</sub>  | V <sub>DD_OV</sub> event bit is set if V <sub>DD</sub> - V <sub>DGND</sub> > V <sub>DD_OV</sub> ; V <sub>DD</sub> increasing |      | 3.82 |     | V     |
| V <sub>DD</sub> Undervoltage                       | V <sub>DD_UV</sub>  | V <sub>DD_UV</sub> is set if V <sub>DD</sub> - V <sub>DGND</sub> < V <sub>DD_UV</sub> ,<br>V <sub>DD</sub> decreasing        |      | 2.7  |     | V     |
| V <sub>DD</sub> Undervoltage Lockout               | V <sub>DDUVLO</sub> | Device operates when V <sub>DD</sub> - V <sub>DGND</sub> > V <sub>DDUVLO</sub> , V <sub>DD</sub> increasing                  | 2    |      | V   |       |
| V <sub>DD</sub> Undervoltage Lockout<br>Hysteresis | V <sub>DDHYS</sub>  |  |      | 120  |     | mV    |
| Thermal Shutdown Threshold                         | T <sub>SHD</sub>    | Ports shut down and device resets if its junction temperature exceeds this limit, temperature increasing (Note 5)            | +150 |      | °C  |       |
| Thermal Shutdown Hysteresis                        | T <sub>SHDH</sub>   | Thermal hysteresis, temperature decreasing (Note 5)  |      | 20   |     | °C    |
| OUTPUT MONITOR                                     |                     |  |      |      |     |       |
| OUT_ Input Current                                 | IBOUT               | V <sub>OUT</sub> = V <sub>AGND</sub> , all modes   |      |      | 2   | μΑ    |
| Idle Pullup Current at OUT_                        | I <sub>DIS</sub>    | OUT_ discharge current, detection and classification off, port shutdown, V <sub>OUT</sub> _ = AGND - 2.8V                    | 200  |      | 265 | μА    |
| PGOOD High Threshold                               | PGTH                | V <sub>OUT</sub> - V <sub>EE</sub> , V <sub>OUT</sub> decreasing   | 1.5  | 2.0  | 2.5 | V     |
| PGOOD Hysteresis                                   | PGHYS               |  |      | 220  |     | mV    |
| PGOOD Low-to-High Glitch Filter                    | tpgood              | Minimum time PGOOD has to be high to set bit in register 10h   |      | 3    |     | ms    |

### **ELECTRICAL CHARACTERISTICS (continued)**

 $(V_{AGND} = 32V \text{ to } 60V, V_{EE} = 0V, V_{DD} \text{ to } V_{DGND} = +3.3V, \text{ all voltages are referenced to } V_{EE}, \text{ unless otherwise noted.}$  Typical values are at  $V_{AGND} = +48V, V_{DGND} = +48V, V_{DD} = (V_{DGND} + 3.3V), T_{A} = +25^{\circ}C.$  Currents are positive when entering the pin and negative otherwise.) (Note 2)

| PARAMETER                                 | SYMBOL            | CONDITIONS  | MIN  | TYP  | MAX  | UNITS |
|---|-------------------|---|------|------|------|-------|
| LOAD DISCONNECT                           | •                 |   |      |      |      | •     |
| DC Load Disconnect<br>Threshold           | VDCTH             | Minimum V <sub>SENSE</sub> _ allowed before disconnect (DC disconnect active), V <sub>OUT</sub> _ = 0V                        | 2.5  | 3.75 | 5.0  | mV    |
| AC Load Disconnect<br>Threshold           | lacth             | Current into DET_, for I < I <sub>ACTH</sub> the port powers off, ACD_EN_ bit = H; V <sub>OSC</sub> = 2.2V, MAX5965B (Note 6) | 285  | 320  | 360  | μΑ    |
| Oscillator Buffer Gain                    | Aosc              | V <sub>DET_</sub> /V <sub>OSC</sub> , ACD_EN_ bit = H, MAX5965B   | 2.9  | 3.0  | 3.1  | V/V   |
| OSC Fail Threshold                        | Vosc_fail         | Port does not power on if Vosc < Vosc_Fail and ACD_EN_ bit is high, MAX5965B (Note 7)   | 1.8  |      | 2.2  | V     |
| OSC Input Impedance                       | Z <sub>OSC</sub>  | OSC input impedance when all the ACD_EN_ are active, MAX5965B   | 100  |      |      | kΩ    |
| Load Disconnect Timer                     | tDISC             | Time from V <sub>SENSE</sub> < V <sub>DCTH</sub> to gate shutdown (Note 8)  | 300  |      | 400  | ms    |
| DETECTION                                 | •                 |   |      |      |      | •     |
| Detection Probe Voltage<br>(First Phase)  | V <sub>DPH1</sub> | Vagnd - VDet_ during the first detection phase  | 3.8  | 4    | 4.2  | V     |
| Detection Probe Voltage<br>(Second Phase) | V <sub>DPH2</sub> | Vagnd - VDET_ during the second detection phase   | 9.0  | 9.3  | 9.6  | V     |
| Current-Limit Protection                  | IDLIM             | V <sub>DET</sub> = V <sub>AGND</sub> , during detection, measure current through DET_   | 1.5  | 1.8  | 2.2  | mA    |
| Short-Circuit Threshold                   | V <sub>DCP</sub>  | If VAGND - VOUT_ < VDCP after the first detection phase a short circuit to AGND is detected                                   |      | 1    |      | V     |
| Open-Circuit Threshold                    | ID_OPEN           | First point measurement current threshold for open condition  |      | 12.5 |      | μΑ    |
| Resistor Detection Window                 | R <sub>DOK</sub>  | (Note 9)  | 19.0 |      | 26.5 | kΩ    |
| Resistor Rejection Window                 | R <sub>DBAD</sub> | Detection rejects lower values  |      |      | 15.2 | kΩ    |
| Tiodictor Flojoction Window               | IIDDAD            | Detection rejects higher values   | 32   |      |      | 1/22  |

### **ELECTRICAL CHARACTERISTICS (continued)**

 $(V_{AGND} = 32V \text{ to } 60V, V_{EE} = 0V, V_{DD} \text{ to } V_{DGND} = +3.3V, \text{ all voltages are referenced to } V_{EE}, \text{ unless otherwise noted.}$  Typical values are at  $V_{AGND} = +48V, V_{DGND} = +48V, V_{DD} = (V_{DGND} + 3.3V), T_{A} = +25^{\circ}C.$  Currents are positive when entering the pin and negative otherwise.) (Note 2)

| PARAMETER                                  | SYMBOL             | CONDITIO   | NS                           | MIN | TYP                        | MAX | UNITS |
|--|--------------------|--|------------------------------|-----|----------------------------|-----|-------|
| DIGITAL INPUTS/OUTPUTS (R                  | eferred to Do      | GND)   |                              |     |                            |     |       |
| Digital Input Low                          | VIL                |  |                              |     |                            | 0.9 | V     |
| Digital Input High                         | VIH                |  |                              | 2.4 |                            |     | V     |
| Internal Input Pullup/Pulldown<br>Resistor | R <sub>DIN</sub>   | Pullup (pulldown) resistor to set default level  | V <sub>DD</sub> (DGND) to    | 25  | 50                         | 75  | kΩ    |
| Open-Drain Output Low Voltage              | V <sub>OL</sub>    | I <sub>SINK</sub> = 15mA   |                              |     |                            | 0.4 | V     |
| Digital Input Leakage                      | I <sub>DL</sub>    | Input connected to the pull  | voltage                      |     |                            | 2   | μΑ    |
| Open-Drain Leakage                         | loL                | Open-drain high impedanc   | e, V <sub>OUT</sub> _ = 3.3V |     |                            | 2   | μΑ    |
| TIMING                                     |                    | _  |                              |     |                            |     |       |
| Startup Time                               | <sup>t</sup> START | Time during which a curren V <sub>SU_LIM</sub> is allowed, starts w turned on (Note 9) | •                            | 50  | 60                         | 70  | ms    |
| Fault Time                                 | t <sub>FAULT</sub> | Maximum allowed time for a condition set by V <sub>FLT_LIM</sub> a (Note 9)            |                              | 50  | 60                         | 70  | ms    |
| Port Turn-Off Time                         | toff               | Minimum delay between an does not apply in case of a                                   |                              |     | 0.5                        |     | ms    |
| Detection Reset Time                       |                    | Time allowed for the port volbefore detection starts                                   | oltage to reset              |     | 80                         | 90  | ms    |
| Detection Time                             | tDET               | Maximum time allowed before completed  | ore detection is             |     |                            | 330 | ms    |
| Midspan Mode Detection Delay               | tDMID              |  |                              | 2.0 |                            | 2.4 | S     |
| Classification Time                        | tCLASS             | Time allowed for classificati  | ion                          |     | 19                         | 23  | ms    |
| VEEUVLO Turn-On Delay                      | tDLY               | Time V <sub>AGND</sub> must be above thresholds before the device                      |                              | 2   |                            | 4   | ms    |
|  |                    | Time a port has to wait  | RSTR bits = 00               |     | 16 x<br>t <sub>FAULT</sub> |     |       |
| Restart Timer                              | trestart           | before turning on after an overcurrent fault during                                    | RSTR bits = 01               |     | 32 x<br>t <sub>FAULT</sub> | ms  |       |
|  |                    | normal operation,<br>RSTR_EN bits = high   | RSTR bits = 10               |     | 64 x<br>t <sub>FAULT</sub> |     |       |
|  |                    | RSTR bits = 11   |                              |     | 0                          |     |       |
| Watchdog Clock Period                      | twD                | Rate of decrement of the wa  | atchdog timer                |     | 164                        |     | ms    |
| ADC PERFORMANCE                            |                    |  |                              |     |                            |     |       |
| Resolution                                 |                    |  |                              |     | 9                          |     | Bits  |
| Range                                      |                    |  |                              |     | 0.51                       |     | V     |
| LSB Step Size                              |                    |  |                              |     | 1                          |     | mV    |
| Integral Nonlinearity (Relative)           | INL                |  |                              |     | 0.2                        | 1.5 | LSB   |

### **ELECTRICAL CHARACTERISTICS (continued)**

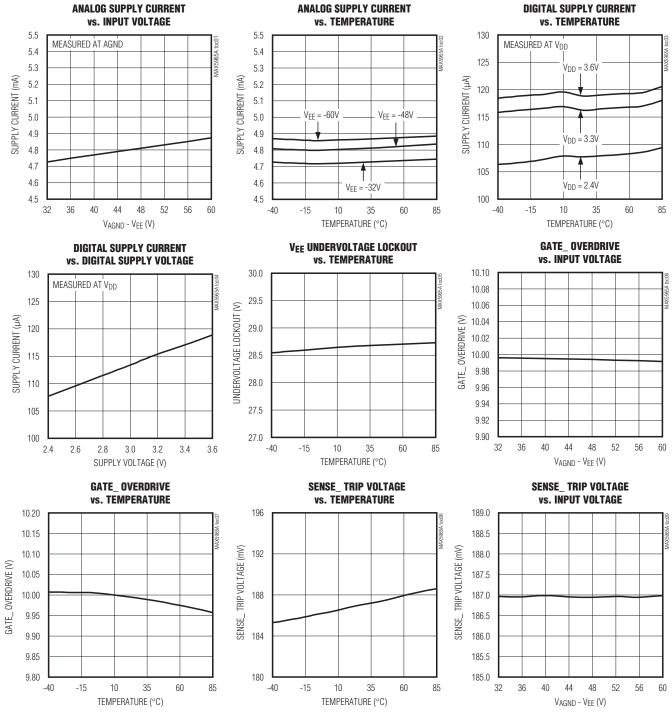
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| PARAMETER  | SYMBOL  | CONDITIONS                  | MIN                       | TYP | MAX | UNITS |  |
|--|---|-----------------------------|---------------------------|-----|-----|-------|--|
| Differential Nonlinearity                        | DNL   |                             |                           | 0.2 | 1.5 | LSB   |  |
| Gain Error                                       |   |                             |                           |     | 3   | %     |  |
| ADC Absolute Accuracy                            |   | V <sub>SENSE_</sub> = 300mV | 295                       | 300 | 305 | LSB   |  |
| TIMING CHARACTERISTICS (F                        | TIMING CHARACTERISTICS (For 2-Wire Fast Mode) |                             |                           |     |     |       |  |
| Serial-Clock Frequency                           | fscl  |                             |                           |     | 400 | kHz   |  |
| Bus Free Time Between a STOP and START Condition | tBUF  |                             | 1.2                       |     |     | μs    |  |
| Hold Time for a START<br>Condition               | tHD, STA                                      |                             | 0.6                       |     |     | μs    |  |
| Low Period of the SCL Clock                      | t <sub>LOW</sub>                              |                             | 1.2                       |     |     | μs    |  |
| High Period of the SCL Clock                     | tHIGH   |                             | 0.6                       |     |     | μs    |  |
| Setup Time for a Repeated START Condition        | tsu, sta                                      |                             | 0.6                       |     |     | μs    |  |
| Data Hold Time                                   | thd, dat                                      |                             | 100                       |     | 300 | ns    |  |
| Data in Setup Time                               | tsu, dat                                      |                             | 100                       |     |     | ns    |  |
| Rise Time of Both SDA and SCL Signals, Receiving | t <sub>R</sub>                                |                             | 20 +<br>0.1C <sub>B</sub> |     | 300 | ns    |  |
| Fall Time of SDA Transmitting                    | t <sub>F</sub>                                |                             | 20 +<br>0.1C <sub>B</sub> |     | 300 | ns    |  |
| Setup Time for STOP Condition                    | tsu, sto                                      |                             | 0.6                       |     |     | μs    |  |
| Capacitive Load for Each Bus Line                | Св  |                             |                           |     | 400 | рF    |  |
| Pulse Width of Spike<br>Suppressed               | tsp   |                             |                           |     | 50  | ns    |  |

- **Note 2:** Limits to  $T_A = -40^{\circ}C$  are guaranteed by design.
- **Note 3:** Default values. The charge/discharge currents are programmable through the serial interface (see the *Register Map and Description* section).
- **Note 4:** Default values. The current-limit thresholds are programmed through the I<sup>2</sup>C-compatible serial interface (see the *Register Map and Description* section).
- Note 5: Functional test is performed over thermal shutdown entering test mode.
- Note 6: This is the default value. Threshold can be programmed through serial interface R23h[2:0].
- Note 7: AC disconnect works only if (V<sub>DD</sub> V<sub>DGND</sub>) ≥ 3V and DGND is connected to AGND.
- Note 8: tDISC can also be programmed through the serial interface (R16h) (see the Register Map and Description section).
- Note 9: R<sub>D</sub> = (V<sub>OUT2</sub> V<sub>OUT1</sub>)/(I<sub>DET2</sub> I<sub>DET1</sub>). V<sub>OUT1</sub>, V<sub>OUT2</sub>, I<sub>DET2</sub>, and I<sub>DET1</sub> represent the voltage at OUT\_ and the current at DET\_ during phase 1 and 2 of the detection.
- **Note 10:** Default values. The startup and fault times can also be programmed through the I<sup>2</sup>C serial interface (see the *Register Map and Description* section).

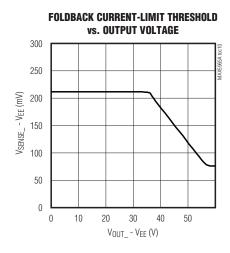
### **Typical Operating Characteristics**

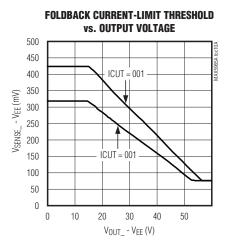
 $(V_{EE} = -48V, V_{DD} = +3.3V, V_{AUTO} = V_{AGND} = V_{DGND} = 0V, \overline{RESET} = \overline{SHD}_{=} = unconnected, R_{SENSE}_{=} = 0.5\Omega$ , IVEE = 00, ICUT = 000, T<sub>A</sub> = +25°C, all registers = default setting, unless otherwise noted.)

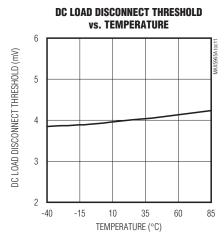


### Typical Operating Characteristics (continued)

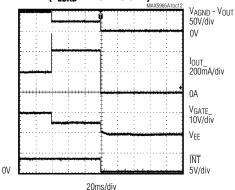
 $(V_{EE} = -48V, V_{DD} = +3.3V, V_{AUTO} = V_{AGND} = V_{DGND} = 0V, \overline{RESET} = \overline{SHD}_{=} = unconnected, R_{SENSE}_{=} = 0.5\Omega$ , IVEE = 00, ICUT = 000, T<sub>A</sub> = +25°C, all registers = default setting, unless otherwise noted.)



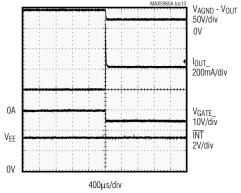




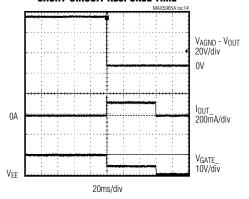
### OVERCURRENT TIMEOUT (RLOAD = 240 $\Omega$ TO 57 $\Omega$ )



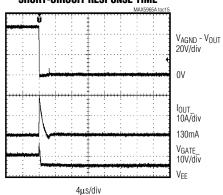
### OVERCURRENT RESPONSE WAVEFORM (MAX5965AUAX) ( $R_{LOAD}$ = 240 $\Omega$ TO 57 $\Omega$ )



#### SHORT-CIRCUIT RESPONSE TIME



### **SHORT-CIRCUIT RESPONSE TIME**



### **Typical Operating Characteristics (continued)**

**ZERO-CURRENT DETECTION WAVEFORM** 

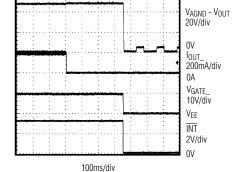
 $(V_{EE} = -48V, V_{DD} = +3.3V, V_{AUTO} = V_{AGND} = V_{DGND} = 0V, \overline{RESET} = \overline{SHD}_{-} = unconnected, R_{SENSE} = 0.5\Omega, IVEE = 00, ICUT = 000, I$  $T_A = +25$ °C, all registers = default setting, unless otherwise noted.)

### **RESET TO OUT TURN-OFF DELAY** RESET 2V/div 0V 200mA/div

 $V_{GATE}$ 

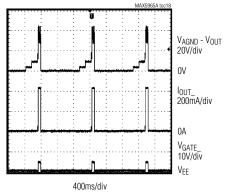
5V/div

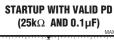
 $V_{EE}$ 

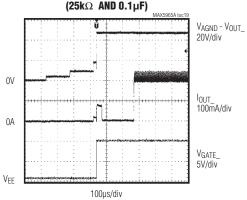




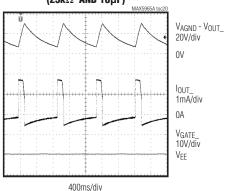
100µs/div



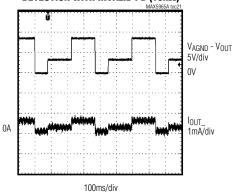




#### **DETECTION WITH INVALID PD** (25k $\Omega$ AND 10 $\mu$ F)

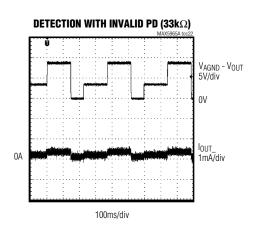


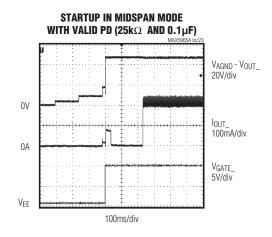
### DETECTION WITH INVALID PD (15 $k\Omega$ )

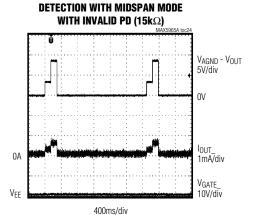


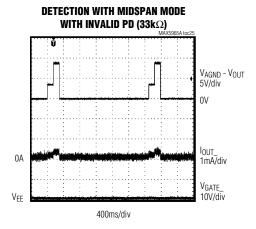
### Typical Operating Characteristics (continued)

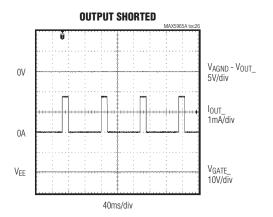
 $(V_{EE} = -48V, V_{DD} = +3.3V, V_{AUTO} = V_{AGND} = V_{DGND} = 0V, \overline{RESET} = \overline{SHD}_{-} = unconnected, R_{SENSE}_{-} = 0.5Ω, IVEE = 00, ICUT = 000, T_{A} = +25°C, all registers = default setting, unless otherwise noted.)$ 

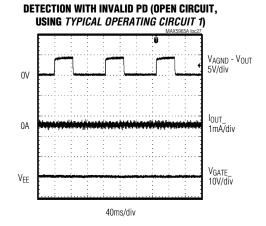






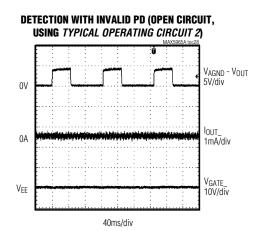


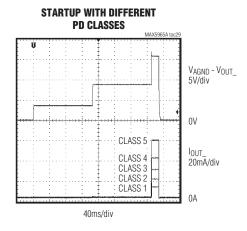


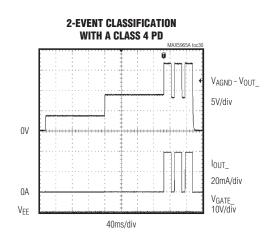


### Typical Operating Characteristics (continued)

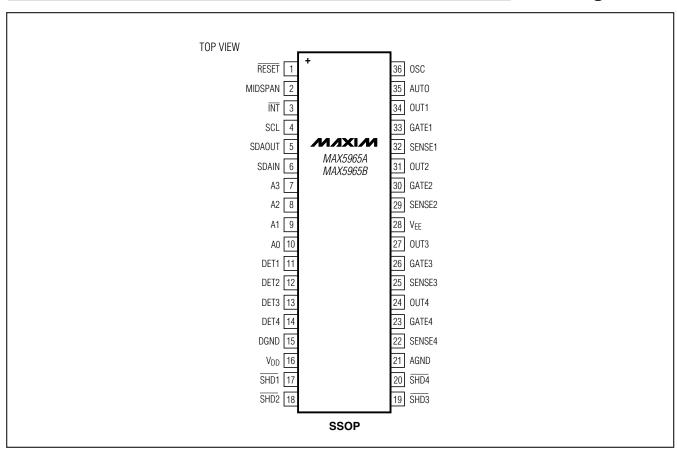
 $(V_{EE} = -48V, V_{DD} = +3.3V, V_{AUTO} = V_{AGND} = V_{DGND} = 0V, \overline{RESET} = \overline{SHD}_{=} = unconnected, R_{SENSE}_{=} = 0.5\Omega$ , IVEE = 00, ICUT = 000, T<sub>A</sub> = +25°C, all registers = default setting, unless otherwise noted.)







### Pin Configuration



### Pin Description

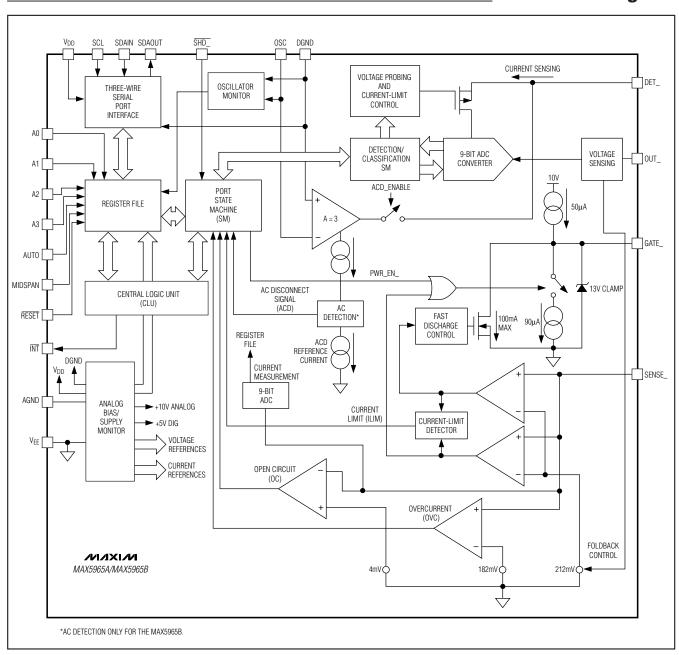
| PIN | NAME    | FUNCTION   |
|-----|---------|--|
| 1   | RESET   | Hardware Reset. Pull $\overline{\text{RESET}}$ low for at least 300µs to reset the device. All internal registers reset to their default value. The address (A0–A3), and AUTO and MIDSPAN input-logic levels latch on during low-to-high transition of $\overline{\text{RESET}}$ . $\overline{\text{RESET}}$ is internally pulled up to $V_{DD}$ with a 50k $\Omega$ resistor. |
| 2   | MIDSPAN | Midspan Mode Input. An internal $50k\Omega$ pulldown resistor to DGND sets the default mode to endpoint PSE operation (power-over-signal pairs). Pull MIDSPAN to $V_{DIG}$ to set midspan operation. The MIDSPAN value latches after the device is powered up or reset (see the <i>PD Detection</i> section).  |
| 3   | ĪNT     | Open-Drain Interrupt Output. INT goes low whenever a fault condition exists. Reset the fault condition using software or by pulling RESET low (see the <i>Interrupt</i> section for more information about interrupt management).  |
| 4   | SCL     | Serial Interface Clock Line Input  |
| 5   | SDAOUT  | Serial Output Data Line. Connect the data line optocoupler input to SDAOUT (see the <i>Typical Operating Circuits</i> ). Connect SDAOUT to SDAIN if using a 2-wire, I <sup>2</sup> C-compatible system.  |

### \_\_\_\_\_Pin Description (continued)

| PIN               | NAME                                    | FUNCTION   |
|-------------------|---|--|
| 6                 | SDAIN                                   | Serial Interface Input Data Line. Connect the data line optocoupler output to SDAIN (see the <i>Typical Operating Circuits</i> ). Connect SDAIN to SDAOUT if using a 2-wire, I <sup>2</sup> C-compatible system.   |
| 7–10              | A3-A0                                   | Address Bits. A3–A0 form the lower part of the device's address. Address inputs default high with an internal $50k\Omega$ pullup resistor to $V_{DD}$ . The address values latch when $V_{DD}$ or $V_{EE}$ ramps up and exceeds its UVLO threshold or after a reset. The 3 MSBs of the address are set to 010.   |
| 11–14             | DET1-DET4                               | Detection/Classification Voltage Outputs. Use DET1 to set the detection and classification probe voltages on port 1. Use DET1 for the AC voltage sensing of port 1 when using the AC disconnect scheme (see the <i>Typical Operating Circuits</i> ).   |
| 15                | DGND                                    | Digital Ground. Connect to digital ground.   |
| 16                | V <sub>DD</sub>                         | Positive Digital Supply. Connect to a digital power supply (reference to DGND).  |
| 17– 20            | SHD1-SHD4                               | Port Shutdown Inputs. Pull $\overline{SHD}$ low to turn off the external FET on port Internally pulled up to $V_{DD}$ with a $50k\Omega$ resistor.   |
| 21                | AGND                                    | Analog Ground. Connect to the high-side analog supply.   |
| 22, 25,<br>29, 32 | SENSE4,<br>SENSE3,<br>SENSE2,<br>SENSE1 | MOSFET Source Current-Sense Negative Inputs. Connect to the source of the power MOSFET and connect a current-sense resistor between SENSE_ and VEE (see the <i>Typical Operating Circuits</i> ).   |
| 23, 26,<br>30, 33 | GATE4,<br>GATE3,<br>GATE2,<br>GATE1     | Port_ MOSFET Gate Drivers. Connect GATE_ to the gate of the external MOSFET (see the <i>Typical Operating Circuits</i> ).  |
| 24, 27,<br>31, 34 | OUT4, OUT3,<br>OUT2, OUT1               | MOSFET Drain-Output Voltage Senses. Connect OUT_ to the power MOSFET drain through a resistor (100 $\Omega$ to 100k $\Omega$ ). The low leakage at OUT_ limits the drop across the resistor to less than 100mV (see the Typical Operating Circuits).   |
| 28                | VEE                                     | Low-Side Analog Supply Input. Connect the low-side analog supply to $V_{\text{EE}}$ (-48V). Bypass with a 1 $\mu$ F capacitor between AGND and $V_{\text{EE}}$ .   |
| 35                | AUTO                                    | Auto or Shutdown Mode Input. Force AUTO high to enter auto mode after a reset or power-up. Drive low to put the MAX5965A/MAX5965B into shutdown mode. In shutdown mode, software controls the operational modes of the MAX5965A/MAX5965B. A 50k $\Omega$ internal pulldown resistor defaults to AUTO low. AUTO latches when VDD or VEE ramps up and exceeds its UVLO threshold or when the device resets. Software commands can take the MAX5965A/MAX5965B out of AUTO while AUTO is high. |
| 36                | OSC                                     | Oscillator Input. AC-disconnect detection function uses OSC. Connect a 100Hz ±10%, 2V <sub>P-P</sub> ±5%, +1.3V offset sine wave to OSC. If the oscillator positive peak falls below the OSC_FAIL threshold of 2V, the ports that have the AC function enabled shut down and are not allowed to power-up. When not using the AC-disconnect detection function, leave OSC unconnected.  |

14 \_\_\_\_\_\_\_**/I/XI/VI** 

### **Functional Diagram**



### **Detailed Description**

The MAX5965A/MAX5965B are quad -48V power controllers designed for use in IEEE 802.3af-compliant/IEEE 802.3at-compatible PSE. The devices provide PD discovery, classification, current limit, DC and AC load disconnect detections in compliance with the IEEE 802.3af standard. The MAX5965A/MAX5965B are pin compatible with the MAX5952/MAX5945/LTC4258/LTC4259A PSE controllers and provides additional features.

The MAX5965A/MAX5965B feature a high-power mode, which provides up to 45W per port. The devices allow the user to program the current-limit and overcurrent thresholds up to 2.5 times the default thresholds. The MAX5965A/MAX5965B can also be programmed to decrease the current-limit and overcurrent threshold by 15% for high operating voltage conditions to keep the output power constant.

The MAX5965A/MAX5965B provide new Class 5 and 2-event classification (Class 6) for detection and classification of high-power PDs. The MAX5965A/MAX5965B provide instantaneous readout of each port current through the I<sup>2</sup>C interface. The MAX5965A/MAX5965B also provide high-capacitance detection for legacy PDs.

The MAX5965A/MAX5965B are fully software configurable and programmable through an I<sup>2</sup>C-compatible, 3-wire serial interface with 49 registers. The class-over-current detection function enables system power management to detect if a PD draws more than the allowable current. The MAX5965A/MAX5965B's extensive programmability enhances system flexibility, enables field diagnosis, and allows for uses in other applications.

The MAX5965A/MAX5965B provide four operating modes to suit different system requirements. Auto mode allows the device to operate automatically without any software supervision. Semi-auto mode automatically detects and classifies a device connected to a port after initial software activation but does not power up that port until instructed to by software. Manual mode allows total software control of the device and is useful for system diagnostics. Shutdown mode terminates all activities and securely turns off power to the ports.

The MAX5965A/MAX5965B provide input undervoltage lockout, input undervoltage detection, a load-stability safety check during detection, input overvoltage lockout, overtemperature detection, output voltage slew-rate limit during startup, power-good, and fault status. The MAX5965A/MAX5965B's programmability includes startup timeout, overcurrent timeout, and load-disconnect detection timeout.

The MAX5965A/MAX5965B communicate with the system microcontroller through an I $^2\text{C}$ -compatible interface. The MAX5965A/MAX5965B feature separate input and output data lines (SDAIN and SDAOUT) for use with optocoupler isolation. As slave devices, the MAX5965A/MAX5965B include four address inputs allowing 16 unique addresses. A separate  $\overline{\text{INT}}$  output and four independent shutdown inputs ( $\overline{\text{SHD}}$ ) provide fast response from a fault to port shutdown between the MAX5965A/MAX5965B and the microcontroller. A  $\overline{\text{RESET}}$  input allows hardware reset of the device.

#### Reset

Reset is a condition the MAX5965A/MAX5965B enter after any of the following conditions:

- After power-up (VEE and VDD rise above their UVLO thresholds).
- 2) Hardware reset. The RESET input is driven low and back high again any time after power-up.
- 3) Software reset. Writing a 1 into R1Ah[4] any time after power-up.
- 4) Thermal shutdown.

During a reset, the MAX5965A/MAX5965B reset their register map to the reset state as shown in Table 37 and latch in the state of AUTO (pin 35) and MIDSPAN (pin 2). During normal operation, change at the AUTO and MIDSPAN input is ignored. While the condition that caused the reset persists (i.e. high temperature, RESET input low, or UVLO conditions) the MAX5965A/MAX5965B do not acknowledge any addressing from the serial interface.

#### Port Reset (R1Ah[3:0])

Set high anytime during normal operation to turn off power and clear the events and status registers of the corresponding port. Port reset only resets the events and status registers.

#### Midspan Mode

In midspan mode, the device adopts cadence timing during the detection phase. When cadence timing is enabled and a failed detection occurs, the port waits between 2s and 2.4s before attempting to detect again. Midspan mode is activated by setting R11h[1] high. The status of the MIDSPAN pin is written to R11h[1] during power-up or after a reset. MIDSPAN is internally pulled low by a  $50 k\Omega$  resistor.

#### **Operation Modes**

The MAX5965A/MAX5965B contain four independent, but identical state machines to provide reliable and real-time control of the four network ports. Each state machine has four operating modes: auto mode, semi-auto mode, manual, and shutdown. Auto mode allows the device to operate automatically without any software supervision. Semi-auto mode, upon request, continuously detects and classifies a device connected to a port but does not power up that port until instructed by software. Manual mode allows total software control of the device and is useful in system diagnostics. Shutdown mode terminates all activities and securely turns off power to the ports.

Switching between auto, semi, or manual mode does not interfere with the operation of the port. When the port is set into shutdown mode, all the port operations are immediately stopped and the port remains idle until shutdown is exited.

#### Automatic (Auto) Mode

Enter automatic (auto) mode by forcing the AUTO input high prior to a reset, or by setting R12h[P\_M1,P\_M0] to [1,1] during normal operation (see Tables 16a and 16b). In auto mode, the MAX5965A/MAX5965B performs detection, classification, and power up the port automatically once a valid PD is detected at the port. If a valid PD is not connected at the port, the MAX5965A/MAX5965B repeat the detection routine continuously until a valid PD is connected.

Going into auto mode, the DET\_EN\_ and CLASS\_EN\_ bits are set to high and stay high unless changed by software. Using software to set DET\_EN\_ and/or CLASS\_EN\_ low causes the MAX5965A/MAX5965B to skip detection and/or classification. As a protection, disabling the detection routine in auto mode does not allow the corresponding port to power up, unless the DET\_BY (R23h[4]) is set to 1.

The AUTO status is latched into the register only during a reset. Any changes to the AUTO input after reset are ignored.

#### Semi-Automatic (Semi-Auto) Mode

Enter semi-auto mode by setting R12h[P\_M1,P\_M0] to [1,0] during normal operation (see Tables 16a and 16b). In semi-auto mode, the MAX5965A/MAX5965B, upon request, perform detection and/or classification repeatedly but do not power up the port(s), regardless of the status of the port connection.

Setting R19h[PWR\_ON\_] (Table 22) high immediately terminates detection/classification routines and turns on power to the port(s).

R14h[DET\_EN\_, CLASS\_EN\_] default to low in semi-auto mode. Use software to set R14h[DET\_EN\_, CLASS\_EN\_] to high to start the detection and/or classification routines. R14h[DET\_EN\_, CLASS\_EN\_] are reset every time the software commands a power off of the port (either through reset or PWR\_OFF\_). In any other case, the status of the bits is left unchanged (including when the state machine turns off the power because a load disconnect or a fault condition is encountered).

#### Manual Mode

Enter manual mode by setting R12h[P\_M1,P\_M0] to [0,1] during normal operation (see Tables 16a and 16b). Manual mode allows the software to dictate any sequence of operation. Write a 1 to both R14h[DET\_EN\_] and R14h[CLASS\_EN\_] to start detection and classification operations, respectively, and in that priority order. After execution, the command is cleared from the register(s). PWR\_ON\_ has highest priority. Setting PWR\_ON\_ high at any time causes the device to immediately enter the powered mode. Setting DET\_EN\_ and CLASS\_EN\_ high at the same time causes detection to be performed first. Once in the powered state, the device ignores DET\_EN\_ or CLASS\_EN\_ commands.

When switching to manual mode from another mode, DET\_EN\_, CLASS\_EN\_ default to low. These bits become pushbutton rather than configuration bits (i.e., writing ones to these bits while in manual mode commands the device to execute one cycle of detection and/or classification. The bits are reset back to zero at the end of the execution).

#### Shutdown Mode

Enter shutdown mode by forcing the AUTO input low prior to a reset, or by setting R12h[P\_M1,P\_M0] to [0,0] during normal operation (see Tables 16a and 16b). Putting the MAX5965A/MAX5965B into shutdown mode immediately turns off power and halts all operations to the corresponding port. The event and status bits of the affected port(s) are also cleared. In shutdown mode, the DET\_EN\_, CLASS\_EN\_, and PWR\_ON\_ commands are ignored.

In shutdown mode, the serial interface operates normally.

#### **PD Detection**

When PD detection is activated, the MAX5965A/MAX5965B probe the output for a valid PD. After each detection cycle, the device sets the DET\_END\_ bit R04h/05h[3:0] high and reports the detection results in the status registers R0Ch[2:0], R0Dh[2:0], R0Eh[2:0], and R0Fh[2:0]. The DET\_END\_ bit is reset to low when read through R05h or after a port reset.

A valid PD has a  $25 \mathrm{k}\Omega$  discovery signature characteristic as specified in the IEEE 802.3af/at standard. Table 1 shows the IEEE 802.3af/at specification for a PSE detecting a valid PD signature. See the *Typical Operating Circuits* and Figure 1a (Detection, Classification, and Power-Up Port Sequence). The MAX5965A/MAX5965B can probe and categorize different types of devices connected to the port such as: a valid PD, an open circuit, a low resistive load, a high resistive load, a high capacitive load, a positive DC supply, or a negative DC supply.

During detection, the MAX5965A/MAX5965B keep the external MOSFET off and force two probe voltages through the DET\_ input. The current through the DET\_ input is measured as well as the voltage at OUT\_. A two-point slope measurement is used as specified by the IEEE 802.3af standard to verify the device connected to the port. The MAX5965A/MAX5965B implement appropriate settling times and a 100ms digital integration to reject 50Hz/60Hz power-line noise coupling.

An external diode, in series with the DET\_ input, restricts PD detection to the first quadrant as specified by the IEEE 802.3af/at standard. To prevent damage to non-PD devices, and to protect themselves from an output short circuit, the MAX5965A/MAX5965B limit the current into DET\_ to less than 2mA maximum during PD detection.

In midspan mode, the MAX5965A/MAX5965B wait 2.2s before attempting another detection cycle after every failed detection. The first detection, however, happens immediately after issuing the detection command.

#### **High-Capacitance Detection**

The CLC\_EN bit in register R23h[5] enables the large capacitor detection feature for legacy PD devices. When CLC\_EN = 1, the high-capacitance detection limit is extended up to  $150\mu\text{F}$ . CLC\_EN = 0 is the default condition for the normal capacitor size detection. See Table 1 and the *Register Map and Description* section.

Table 1. PSE PI Detection Modes Electrical Requirement (Table 33-2 of the IEEE 802.3af Standard)

| PARAMETER                                 | SYMBOL            | MIN  | MAX  | UNITS | ADDITIONAL INFORMATION                                |
|---|-------------------|------|------|-------|---|
| Open-Circuit Voltage                      | Voc               | _    | 30   | V     | In detection mode only                                |
| Short-Circuit Current                     | I <sub>SC</sub>   | _    | 5    | mA    | In detection mode only                                |
| Valid Test Voltage                        | Vvalid            | 2.8  | 10   | V     |   |
| Voltage Difference<br>Between Test Points | ΔVTEST            | 1    | _    | V     |   |
| Time Between Any Two<br>Test Points       | t <sub>BP</sub>   | 2    | _    | ms    | This timing implies a 500Hz maximum probing frequency |
| Slew Rate                                 | V <sub>SLEW</sub> |      | 0.1  | V/µs  |   |
| Accept Signature<br>Resistance            | RGOOD             | 19   | 26.5 | kΩ    |   |
| Reject Signature<br>Resistance            | R <sub>BAD</sub>  | < 15 | > 33 | kΩ    |   |
| Open-Circuit Resistance                   | ROPEN             | 500  | _    | kΩ    |   |
| Accept Signature<br>Capacitance           | C <sub>GOOD</sub> | _    | 150  | nF    |   |
| Reject Signature<br>Capacitance           | C <sub>BAD</sub>  | 10   | _    | μF    |   |
| Signature Offset Voltage<br>Tolerance     | Vos               | 0    | 2.0  | V     |   |
| Signature Offset Current<br>Tolerance     | IOS               | 0    | 12   | μΑ    |   |

### Powered Device Classification (PD Classification)

During the PD classification mode, the MAX5965A/MAX5965B force a probe voltage (-18V) at DET\_ and measure the current into DET\_. The measured current determines the class of the PD.

After each classification cycle, the device sets the CL\_END\_ bit (R04h/05h[7:4]) high and reports the classification results in the status registers R0Ch[6:4], R0Dh[6:4], R0Eh[6:4], and R0Fh[6:4]. The CL\_END\_ bit is reset to low when read through register R05h or after a port reset. Both events registers, R04h, and R05h are cleared after the port powers down. Table 2 shows the IEEE 802.3af requirement for a PSE classifying a PD at the power interface (PI).

The MAX5965A/MAX5965B support high power beyond the IEEE 802.3af standard by providing additional classifications (Class 5 and 2-event classification).

#### Class 5 PD Classification

During classification, if the MAX5965A/MAX5965B detect currents in excess of I<sub>CLASS</sub> > 48mA, then the PD will be classified as a Class 5 powered device. Status registers R0Ch[6:4] or R0Dh[6:4] or R0Eh[6:4] or R0Fh[6:4] will report the Class 5 classification result.

#### 2-Event (Class 6) PD Classification

When 2-event classification is activated, the classification cycle is repeated three times with 8ms wait time between each cycle (see Figure 1b). Between each classification cycle, the MAX5965A/MAX5965B do not reset the port voltage completely but keeps the output

voltage at -9V. The EN\_CL6 bits in R1Ch[7:4] enable 2-event classification on a per port basis.

#### **Powered State**

When the MAX5965A/MAX5965B enter a powered state, the tSTART and tDISC timers are reset. Before turning on the port power, the MAX5965A/MAX5965B check if any other port is not turning on and if the tFAULT timer is zero. Another check is performed if the ACD\_EN\_ bit is set, in this case the OSC\_FAIL bit must be low (oscillator is okay) for the port to be powered.

If these conditions are met, the MAX5965A/MAX5965B enter startup where it turns on power to the port. An internal signal, POK\_, asserts high when V<sub>OUT</sub>\_ is within 2V from V<sub>EE</sub>. PGOOD\_ status bits are set high if POK\_ stays high longer than t<sub>PGOOD</sub>. PGOOD\_ immediately resets when POK\_ goes low (see Figure 2).

The PG\_CHG\_ bit sets when a port powers up or down. PWR\_EN\_ sets when a port powers up and resets when a port shuts down. The port shutdown timer lasts 0.5ms and prevents other ports from turning off during that period, except in the case of emergency shutdowns (RESET = L, RESET\_IC = H, VEEUVLO, VDDUVLO, and TSHD).

The MAX5965A/MAX5965B always check the status of all ports before turning off. A priority logic system determines the order to prevent the simultaneous turn-on or turn-off of the ports. The port with the lesser ordinal number gets priority over the others (i.e., port 1 turns on first, port 2 second, port 3 third, and port 4 fourth). Setting PWR\_OFF\_ high turns off power to the corresponding port.

Table 2. PSE Classification of a PD (Refer to Table 33-4 of the IEEE 802.3af)

| MEASURED I <sub>CLASS</sub> (mA) | CLASSIFICATION       |  |  |
|----------------------------------|----------------------|--|--|
| 0 to 5                           | Class 0              |  |  |
| > 5 and < 8                      | May be Class 0 and 1 |  |  |
| 8 to 13                          | Class 1              |  |  |
| > 13 and < 16                    | May be Class 1 or 2  |  |  |
| 16 to 21                         | Class 2              |  |  |
| > 21 and < 25                    | May be Class 2 or 3  |  |  |
| 25 to 31                         | Class 3              |  |  |
| > 31 and < 35                    | May be Class 3 or 4  |  |  |
| 35 to 45                         | Class 4              |  |  |
| > 45 and < 51                    | May be Class 4 or 5  |  |  |
| 51 to 68                         | Class 5              |  |  |

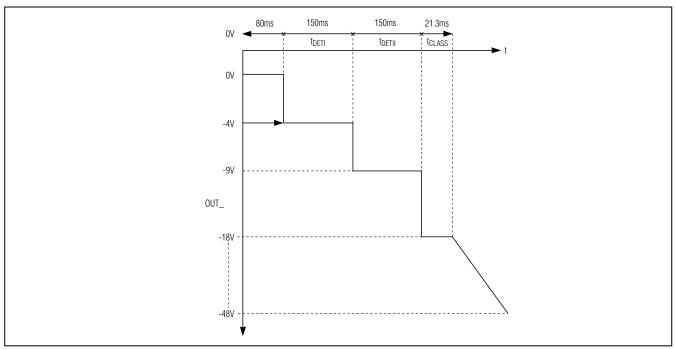


Figure 1a. Detection, Classification, and Power-Up Port Sequence

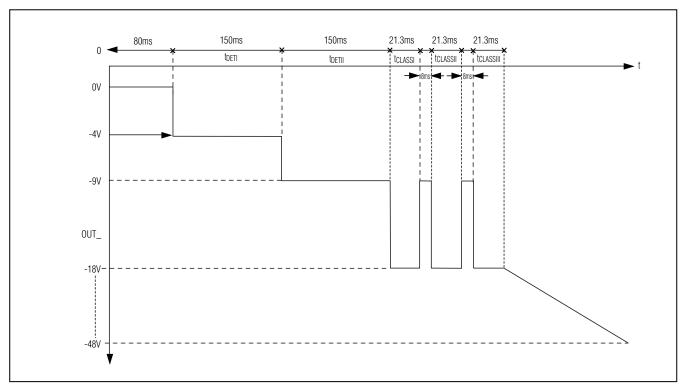


Figure 1b. Detection, 2-Event Classification, and Power-Up Port Sequence

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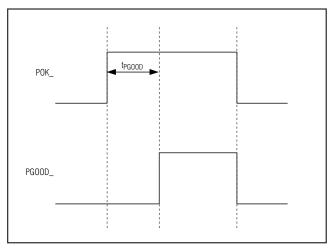


Figure 2. PGOOD\_ Timing

#### **Overcurrent Protection**

A sense resistor Rs connected between SENSE\_ and VEE monitors the load current. Under normal operating conditions, the voltage across Rs (VRS) never exceeds the threshold Vsu Lim. If VRS exceeds Vsu Lim, an internal current-limiting circuit regulates the GATE\_ voltage, limiting the current to ILIM = VSU LIM/Rs. During transient conditions, if VRS exceeds VSU LIM by more than 1V, a fast pulldown circuit activates to quickly recover from the current overshoot. During startup, if the current-limit condition persists, when the startup timer, tstart, times out, the port shuts off, and the STRT\_FLT\_ bit is set. In the normal powered state, the MAX5965A/MAX5965B check for overcurrent conditions as determined by VFLT\_LIM = ~88% of VSU\_LIM. The trault counter sets the maximum allowed continuous overcurrent period. The tFAULT counter increases when VRS exceeds VFLT LIM and decreases at a slower pace when V<sub>RS</sub> drops below V<sub>FLT LIM</sub>. A slower decrement for the tFAULT counter allows for detecting repeated short-duration overcurrents. When the counter reaches the tFAULT limit, the MAX5965A/MAX5965B power off the port and assert the IMAX\_FLT\_ bit. For a continuous overstress, a fault latches exactly after a period of tFAULT. VSU LIM is programmable through the ICUT registers R2Ah[6:4], R2Ah[2:0], R2Bh[6:4], R2Bh[2:0], and the IVEE bits in register R29h[1:0]. See the High-Power Mode section for more information on the ICUT register.

After power-off due to an overcurrent fault, and if the RSTR\_EN bit is set, the tFAULT timer is not immediately reset but starts decrementing at the same slower pace. The MAX5965A/MAX5965B allow the port to be powered on only when the tFAULT counter is at zero. This feature sets an automatic duty-cycle protection to the external MOSFET avoiding overheating.

The MAX5965A/MAX5965B continuously flag when the current exceeds the maximum current allowed for the class as indicated in the CLASS status register. When class overcurrent occurs, the MAX5965A/MAX5965B set the IVC\_ bit in register R09h.

### ICUT Register and High-Power Mode

ICUT Register

The ICUT register determines the maximum current limits allowed for each port of the MAX5965A/MAX5965B. The 3 ICUT bits (R2Ah[6:4], R2Ah[2:0], R2Bh[6:4], and R2Bh[2:0]) allow programming of the current-limit and overcurrent thresholds in excess of the IEEE standard limit (see Tables 34a, 34b, and 34c). The ICUT registers can be written to directly through the I<sup>2</sup>C interface when CL\_DISC (R17h[2]) is set to 0 (see Table 3). In this case, the current limit of the port is configured regardless of the status of the classification.

By setting the CL\_DISC bit to 1, the MAX5965A/MAX5965B automatically set the ICUT register based upon the classification result of the port. See Table 3 and the *Register Map and Description* section.

### High-Power Mode

When CL\_DISC (R17h[2]) is set to 0, high-power mode is configured by setting the ICUT bits to any combination other than 000, 110, or 111 (note that 000 is the default value for the IEEE standard limit). See Table 3 and the *Register Map and Description* section.

#### **Foldback Current**

During startup and normal operation, an internal circuit senses the voltage at OUT\_ and reduces the current-limit value when  $(V_{OUT_-} - V_{EE}) > 28V$ . The foldback function helps to reduce the power dissipation on the FET. The current limit eventually reduces down to 1/3 of ILIM when  $(V_{OUT_-} - V_{EE}) > 48V$  (see Figure 3a). For high-power mode, the foldback starts when  $(V_{OUT_-} - V_{EE}) > 10V$  (see Figure 3b). In high-power mode, the current limit  $(I_{LIM})$  is reduced down to minimum foldback current  $(V_{TH}) = V_{TE}$  (VOUT\_- - V\_{EE}) > 48V.

**Table 3. Automatic ICUT Programming** 

| CL_DISC | PORT<br>CLASSIFICATION<br>RESULT | ENx_CL6 | EN_HP_ALL | EN_HP_CL6 | EN_HP_CL5 | EN_HP_CL4 | RESULTING ICUT<br>REGISTER BITS |
|---------|----------------------------------|---------|-----------|-----------|-----------|-----------|---------------------------------|
| 0       | Any                              | Х       | X         | X         | X         | X         | User programmed                 |
| 1       | 1                                | Х       | X         | X         | X         | X         | ICUT = 110                      |
| 1       | 2                                | Х       | X         | X         | X         | X         | ICUT = 111                      |
| 1       | 0, 3                             | Х       | X         | X         | Х         | X         | ICUT = 000                      |
| 1       | 4, 5                             | Х       | 0         | X         | X         | X         | ICUT = 000                      |
| 1       | 5                                | Х       | 1         | X         | 1         | X         | ICUT = R24h[6:4]                |
| 1       | 5                                | Х       | 1         | Х         | 0         | Х         | ICUT = 000                      |
| 1       | 4                                | Х       | 1         | Х         | Х         | 1         | ICUT = R24h[6:4]                |
| 1       | 4                                | Х       | 1         | X         | Х         | 0         | ICUT = 000                      |
| 1       | 6 or Illegal                     | 0       | X         | X         | Х         | X         | _                               |
| 1       | 6 or Illegal                     | 1       | 1         | 1         | Х         | Х         | (See Table 35a)                 |
| 1       | 6 or Illegal                     | 1       | 1         | 0         | Х         | Х         | ICUT = 000                      |
| 1       | 6 or Illegal                     | 1       | 0         | Х         | Х         | Х         | ICUT = 000                      |

#### **MOSFET Gate Driver**

Connect the gate of the external n-channel MOSFET to GATE\_. An internal 50µA current source pulls GATE\_ to (VEE + 10V) to turn on the MOSFET. An internal 40µA current source pulls down GATE\_ to VEE to turn off the MOSFET.

The pullup and pulldown current controls the maximum slew rate at the output during turn-on or turn-off. Use the following equation to set the maximum slew rate:

$$\frac{\Delta V_{OUT}}{\Delta t} = \frac{I_{GATE}}{C_{GD}}$$

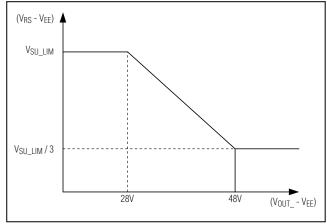


Figure 3a. Foldback Current Characteristics

where CGD is the total capacitance between GATE and DRAIN of the external MOSFET. Current limit and the capacitive load at the drain control the slew rate during startup. During current-limit regulation, the MAX5965A/MAX5965B manipulate the GATE\_ voltage to control the voltage at SENSE\_ (VRS). A fast pulldown activates if VRS overshoots the limit threshold (VSU\_LIM). The fast pulldown current increases with the amount of overshoot. The maximum fast pulldown current is 100mA.

During turn-off, when the GATE\_ voltage reaches a value lower than 1.2V, a strong pulldown switch is activated to keep the MOSFET securely off.

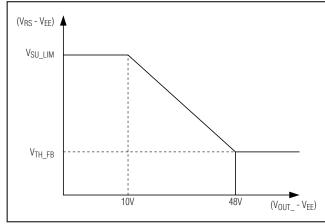


Figure 3b. Foldback Current Characteristics for High-Power Mode

#### **Digital Logic**

Vpp supplies power for the internal logic circuitry. Vpp ranges from +3.0V to +5.5V and determines the logic thresholds for the CMOS connections (SDAIN, SDAOUT, SCL, AUTO, SHD\_, A\_). This voltage range enables the MAX5965A/MAX5965B to interface with a nonisolated low-voltage microcontroller. The MAX5965A/MAX5965B check the digital supply for compatibility with the internal logic. The MAX5965A/MAX5965B also feature a VDD undervoltage lockout (VDDUVLO) of +2.0V. A VDDUVLO condition keeps the MAX5965A/MAX5965B in reset and the ports shut off. Bit 0 in the supply event register shows the status of VDDUVLO (Table 12) after VDD has recovered. All logic inputs and outputs reference to DGND. For AC-disconnected detection, DGND and AGND must be connected together externally. Connect DGND to AGND at a single point in the system as close as possible to the MAX5965A/MAX5965B.

#### **Hardware Shutdown**

SHD\_ shuts down the respective ports without using the serial interface. Hardware shutdown offers an emergency turn-off feature that allows a fast disconnect of the power supply from the port. Pull SHD\_ low to remove power. SHD\_ also resets the corresponding events and status register bits.

#### Interrupt

The MAX5965A/MAX5965B contain an open-drain logic output (INT) that goes low when an interrupt condition exists. R00h and R01h (Tables 6 and 7) contain the definitions of the interrupt registers. The mask register R01h determines events that trigger an interrupt. As a response to an interrupt, the controller reads the status of the event register to determine the cause of the interrupt and takes subsequent actions. Each interrupt event register also contains a Clear on Read (CoR) register. Reading through the CoR register address clears the interrupt. INT remains low when reading the interrupt through the read-only addresses. For example, to clear a startup fault on the port 4 read address 09h (see Table 11). Use the global pushbutton bit in register 1Ah (bit 7, Table 23) to clear interrupts, or use a software or hardware reset.

### Undervoltage and Overvoltage Protection

The MAX5965A/MAX5965B contain several undervoltage and overvoltage protection features. Table 12 in the Register Map and Description section shows a detailed list of the undervoltage and overvoltage protection features. An internal VEE undervoltage lockout (VEEUVLO) circuit keeps the MOSFET off and the MAX5965A/MAX5965B in reset until VAGND - VEE exceeds 29V for more than 3ms. An internal VEE overvoltage (VEE\_OV) circuit shuts down the ports when (VAGND - VEE) exceeds

60V. The digital supply also contains an undervoltage lockout (VDDUVLO). The MAX5965A/MAX5965B also feature three other undervoltage and overvoltage interrupts: VEE undervoltage interrupt (VEE\_UV), VDD undervoltage interrupt (VDD\_UV), and VDD overvoltage interrupt (VDD\_OV). A fault latches into the supply events register (Table 12), but the MAX5965A/MAX5965B does not shut down the ports with VEE\_UV, VDD\_UV, or VDD\_OV.

### **DC** Disconnect Monitoring

Setting R13h[DCD\_EN\_] bits high enables DC load monitoring during a normal powered state. If  $V_{RS}$  (the voltage across Rs) falls below the DC load disconnect threshold,  $V_{DCTH}$ , for more than  $t_{DISC}$ , the device turns off power and asserts the LD\_DISC\_ bit of the corresponding port.

### AC Disconnect Monitoring Features (MAX5965B)

The MAX5965B features AC load disconnect monitoring. Connect an external sine wave to OSC. The oscillator requirements are:

- 1)  $V_{P-P} \times Frequency = 200V_{P-P} \times Hz \pm 15\%$
- 2) Positive peak voltage > +2.2V
- 3) Frequency > 60Hz

A 100Hz  $\pm$ 10%, 2Vp-p  $\pm$ 5%, with +1.3V offset (VpEAK = +2.3V typical) is recommended.

The MAX5965B buffers and amplifiers three times the external oscillator signal and sends the signal to DET\_, where the sine wave is AC-coupled to the output. The MAX5965B senses the presence of the load by monitoring the amplitude of the AC current returned to DET\_ (see the *Functional Diagram*).

Setting R13h[ACD\_EN\_] bits high enable AC load disconnect monitoring during a normal powered state. If the AC current peak at the DET\_ input falls below IACTH for more than tDISC, the device turns off power and asserts the LD\_DISC\_ bit of the corresponding port. IACTH is programmable using R23h[2:0].

An internal comparator checks for a proper amplitude of the oscillator input. If the positive peak of the input sinusoid falls below a safety value of 2V (typ), OSC\_FAIL sets and the port shuts down. Power cannot be applied to the ports when ACD\_EN\_ is set high and OSC\_FAIL is set high. Leave OSC unconnected or connect it to DGND when not using AC-disconnect detection.

#### **Thermal Shutdown**

If the MAX5965A/MAX5965B die temperature reaches +150°C, an overtemperature fault generates and the MAX5965A/MAX5965B shut down. The MOSFETs turn off. The die temperature of the MAX5965A/MAX5965B must cool down below +130°C to remove the overtemperature fault condition. After a thermal shutdown, the part is reset.

#### Watchdog

The R1Eh and R1Fh registers control the watchdog operation. The watchdog function, when enabled, allows the MAX5965A/MAX5965B to gracefully take over control or securely shuts down the power to the ports in case of software/firmware crashes. Contact the factory for more details.

#### **Address Inputs**

A3, A2, A1, and A0 represent the 4 LSBs of the chip address. The complete chip address is 7 bits (see Table 4).

The 4 LSBs latch on the low-to-high transition of  $\overline{RESET}$  or after a power-supply start (either on VDD or VEE). Address inputs default high through an internal  $50k\Omega$  pullup resistor to VDD. The MAX5965A/MAX5965B also respond to the call through a global address 30h (see the <code>Global Addressing and Alert Response Protocol</code> section).

#### Table 4. MAX5965A/MAX5965B Address

| 0 | 1 | 0 | АЗ | A2 | A1 | A0 | R/W |
|---|---|---|----|----|----|----|-----|

### I<sup>2</sup>C-Compatible Serial Interface

The MAX5965A/MAX5965B operate as a slave that sends and receives data through an I<sup>2</sup>C-compatible, 2-wire or 3-wire interface. The interface uses a serial-data input line (SDAIN), a serial-data output line (SDAOUT), and a serial-clock line (SCL) to achieve bidirectional communication between master(s) and slave(s). A master (typically a microcontroller) initiates all data transfers to and from the MAX5965A/MAX5965B, and generates the SCL clock that synchronizes the data transfer. In most applications, connect the SDAIN and the SDAOUT lines together to form the serial-data line (SDA).

Using the separate input and output data lines allows optocoupling with the controller bus when an isolated supply powers the microcontroller.

The MAX5965A/MAX5965B SDAIN line operates as an input. The MAX5965A/MAX5965B SDAOUT operates as an open-drain output. A pullup resistor, typically 4.7k $\Omega$ , is required on SDAOUT. The MAX5965A/MAX5965B SCL line operates only as an input. A pullup resistor, typically 4.7k $\Omega$ , is required on SCL if there are multiple masters, or if the master in a single-master system has an open-drain SCL output.

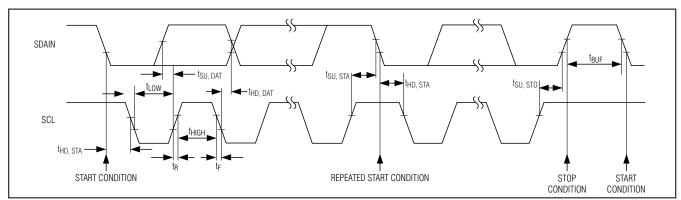


Figure 4. 2-Wire, Serial-Interface Timing Details

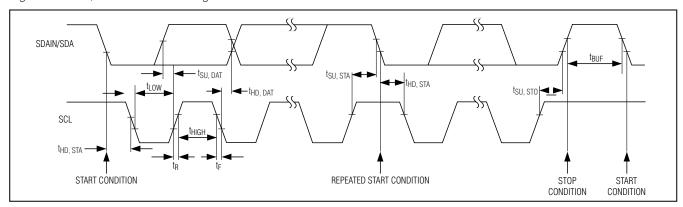


Figure 5. 3-Wire, Serial-Interface Timing Details

#### Serial Addressing

Each transmission consists of a START condition (Figure 6) sent by a master, followed by the MAX5965A/MAX5965B 7-bit slave address plus  $R/\overline{W}$  bit, a register address byte, one or more data bytes, and finally a STOP condition.

### START and STOP Conditions

Both SCL and SDA remain high when the interface is not busy. A master signals the beginning of a transmission with a START (S) condition by transitioning SDA from high to low while SCL is high. When the master finishes communicating with the slave, the master issues a STOP (P) condition by transitioning SDA from low to high while SCL is high. The STOP condition frees the bus for another transmission.

#### Bit Transfer

Each clock pulse transfers one data bit (Figure 7). The data on SDA must remain stable while SCL is high.

#### Acknowledge

The acknowledge bit is a clocked 9th bit (Figure 8) that the recipient uses to handshake receipt of each byte of data. Thus each byte effectively transferred requires 9 bits. The master generates the 9th clock pulse, and the recipient pulls down SDA (or the SDAOUT in the 3-wire interface) during the acknowledge clock pulse, so that the SDA line is stable low during the high period of the clock pulse. When the master transmits to the MAX5965A/MAX5965B, the MAX5965A/MAX5965B generate the acknowledge bit. When the MAX5965A/MAX5965B transmit to the master, the master generates the acknowledge bit.

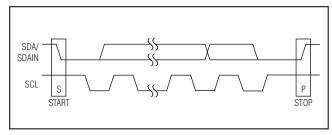


Figure 6. START and STOP Conditions

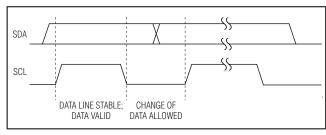


Figure 7. Bit Transfer

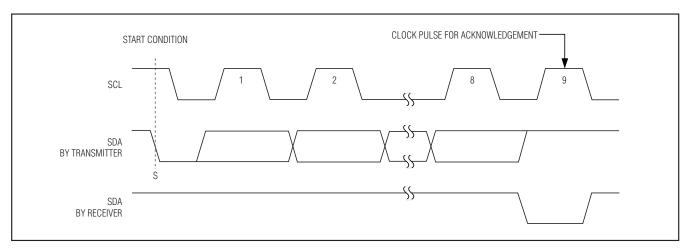


Figure 8. Acknowledge

#### Slave Address

The MAX5965A/MAX5965B have a 7-bit long slave address (Figure 9). The bit following the 7-bit slave address (bit eight) is the  $R/\overline{W}$  bit, which is low for a write command and high for a read command.

010 always represents the first 3 bits (MSBs) of the MAX5965A/MAX5965B slave address. Slave address bits A3, A2, A1, and A0 represent the states of the MAX5965A/MAX5965B's A3, A2, A1, and A0 inputs, allowing up to sixteen MAX5965A/MAX5965B devices to share the bus. The states of the A3, A2, A1, and A0 latch in upon the reset of the MAX5965A/MAX5965B into register R11h. The MAX5965A/MAX5965B monitor the bus continuously, waiting for a START condition followed by the MAX5965A/MAX5965B's slave address. When a MAX5965A/MAX5965B recognizes its slave address, the MAX5965A/MAX5965B acknowledge and are then ready for continued communication.

#### Global Addressing and Alert Response Protocol

The global address call is used in writing mode to write the same register to multiple devices (address 0x60). In read mode (address 0x61), the global address call is used as the alert response address. When responding to a global call, the MAX5965A/MAX5965B put their own address out on the data line whenever the interrupt is active. Every other device connected to the SDAOUT line that has an active interrupt also does this. After every bit transmitted, the MAX5965A/MAX5965B check that the data line effectively corresponds to the data it

is delivering. If it is not, it then backs off and frees the data line. This litigation protocol always allows the part with the lowest address to complete the transmission. The microcontroller can then respond to the interrupt and take proper actions. The MAX5965A/MAX5965B do not reset their own interrupt at the end of the alert response protocol. The microcontroller has to do it by clearing the event register through their CoR adresses or activating the CLR\_INT pushbutton.

### Message Format for Writing to the MAX5965A/MAX5965B

A write to the MAX5965A/MAX5965B comprises of the MAX5965A/MAX5965B's slave address transmission with the R/W bit set to 0, followed by at least 1 byte of information. The first byte of information is the command byte (Figure 10). The command byte determines which register of the MAX5965A/MAX5965B is written to by the next byte, if received. If the MAX5965A/ MAX5965B detect a STOP condition after receiving the command byte, the MAX5965A/MAX5965B take no further action beyond storing the command byte. Any bytes received after the command byte are data bytes. The first data byte goes into the internal register of the MAX5965A/MAX5965B selected by the command byte. If the MAX5965A/MAX5965B transmit multiple data bytes before the MAX5965A/MAX5965B detect a STOP condition, these bytes store in subsequent MAX5965A/ MAX5965B internal registers because the control byte address autoincrements.

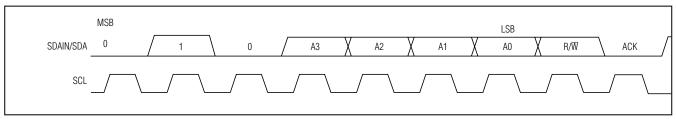


Figure 9. Slave Address

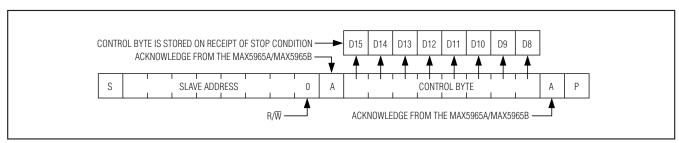


Figure 10. Control Byte Received

26 **// / X | //** |

#### Message Format for Reading

The MAX5965A/MAX5965B read using the MAX5965A/MAX5965B's internally stored command byte as an address pointer, the same way the stored command byte is used as an address pointer for a write. The pointer autoincrements after reading each data byte using the same rules as for a write. Thus, a read is initiated by first configuring the MAX5965A/MAX5965B's command byte by performing a write. The master now reads 'n' consecutive bytes from the MAX5965A/MAX5965B, with the first data byte read from the register addressed by the initialized command byte. When performing read-after-write verification, remember to reset the command byte's address because the stored control byte address autoincrements after the write.

#### Operation with Multiple Masters

When the MAX5965A/MAX5965B operate on a 2-wire interface with multiple masters, a master reading the MAX5965A/MAX5965B should use repeated starts between the write which sets the MAX5965A/MAX5965B's address pointer, and the read(s) that take the data from the location(s). It is possible for master 2 to take over the bus after master 1 has set up the

MAX5965A/MAX5965B's address pointer but before master 1 has read the data. If master 2 subsequently resets the MAX5965A/MAX5965B's address pointer then master 1's read may be from an unexpected location.

#### Command Address Autoincrementing

Address autoincrementing allows the MAX5965A/MAX5965B to be configured with fewer transmissions by minimizing the number of times the command address needs to be sent. The command address stored in the MAX5965A/MAX5965B generally increments after each data byte is written or read (Table 5). The MAX5965A/MAX5965B are designed to prevent overwrites on unavailable register addresses and unintentional wrap-around of addresses.

**Table 5. Autoincrement Rules** 

| COMMAND BYTE ADDRESS RANGE | AUTOINCREMENT BEHAVIOR                                     |
|----------------------------|--|
| 0x00 to 0x26               | Command address autoincrements after byte read or written  |
| 0x26                       | Command address remains at 0x26 after byte written or read |

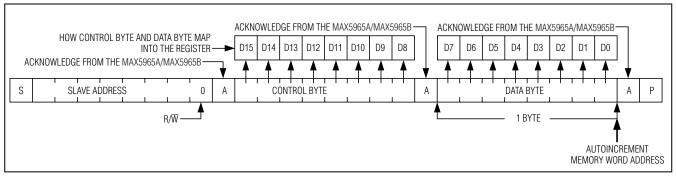


Figure 11. Control and Single Data Byte Received

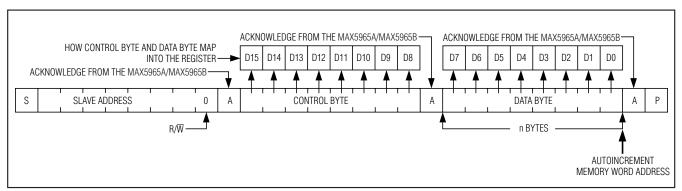


Figure 12. 'n' Data Bytes Received

### Register Map and Description

The interrupt register (Table 6) summarizes the event register status and is used to send an interrupt signal (INT goes low) to the controller. Writing a 1 to R1Ah[7] clears all interrupt and events registers. A reset sets R00h to 00h.

INT\_EN (R17h[7]) is a global interrupt mask (Table 7). The MASK\_ bits activate the corresponding interrupt bits in register R00h. Writing a 0 to INT\_EN (R17h[7]) disables the  $\overline{\text{INT}}$  output.

A reset sets R01h to AAA00A00b where A is the state of the AUTO input prior to the reset.

### Table 6. Interrupt Register

| ADDRE    | SS = 00h |     | DECODIDATION   |
|----------|----------|-----|--|
| SYMBOL   | BIT      | R/W | DESCRIPTION  |
| SUP_FLT  | 7        | R   | Interrupt signal for supply faults. SUP_FLT is the logic OR of all the bits [7:0] in register R0Ah/R0Bh (Table 12).      |
| TSTR_FLT | 6        | R   | Interrupt signal for startup failures. TSTR_FLT is the logic OR of bits [7:0] in register R08h/R09h (Table 11).          |
| IMAX_FLT | 5        | R   | Interrupt signal for current-limit violations. IMAX_FLT is the logic OR of bits [3:0] in register R06h/R07h (Table 10).  |
| CL_END   | 4        | R   | Interrupt signal for completion of classification. CL_END is the logic OR of bits [7:4] in register R04h/R05h (Table 9). |
| DET_END  | 3        | R   | Interrupt signal for completion of detection. DET_END is the logic OR of bits [3:0] in register R04h/R05h (Table 9).     |
| LD_DISC  | 2        | R   | Interrupt signal for load disconnection. LD_DISC is the logic OR of bits [7:4] in register R06h/R07h (Table 10).         |
| PG_INT   | 1        | R   | Interrupt signal for PGOOD status change. PG_INT is the logic OR of bits [7:4] in register R02h/R03h (Table 8).          |
| PEN_INT  | 0        | R   | Interrupt signal for power-enable status change. PEN_INT is the logic OR of bits [3:0] in register R02h/R03h (Table 8).  |

### **Table 7. Interrupt Mask Register**

| ADDRI  | ESS = 01h |     | DECODIDATION  |
|--------|-----------|-----|---|
| SYMBOL | BIT       | R/W | DESCRIPTION   |
| MASK7  | 7         | R/W | Interrupt mask bit 7. A logic-high enables the SUP_FLT interrupts. A logic-low disables the SUP_FLT interrupts.   |
| MASK6  | 6         | R/W | Interrupt mask bit 6. A logic-high enables the TSTR_FLT interrupts. A logic-low disables the TSTR_FLT interrupts. |
| MASK5  | 5         | R/W | Interrupt mask bit 5. A logic-high enables the IMAX_FLT interrupts. A logic-low disables the IMAX_FLT interrupts. |
| MASK4  | 4         | R/W | Interrupt mask bit 4. A logic-high enables the CL_END interrupts. A logic-low disables the CL_END interrupts.     |
| MASK3  | 3         | R/W | Interrupt mask bit 3. A logic-high enables the DET_END interrupts. A logic-low disables the DET_END interrupts.   |
| MASK2  | 2         | R/W | Interrupt mask bit 2. A logic-high enables the LD_DISC interrupts. A logic-low disables the LD_DISC interrupts.   |
| MASK1  | 1         | R/W | Interrupt mask bit 1. A logic-high enables the PG_INT interrupts. A logic-low disables the PG_INT interrupts.     |
| MASK0  | 0         | R/W | Interrupt mask bit 0. A logic-high enables the PEN_INT interrupts. A logic-low disables the PEN_INT interrupts.   |

The power event register (Table 8) records changes in the power status of the four ports. Any change in PGOOD\_ (R10h[7:4]) sets PG\_CHG\_ to 1. Any change in the PWR\_EN\_ (R10h[3:0]) sets PWEN\_CHG\_ to 1. PG\_CHG\_ and PWEN\_CHG\_ trigger on the edges of PGOOD\_ and PWR\_EN\_ and do not depend on the

actual level of the bits. The power event register has two addresses. When read through the R02h address, the content of the register is left unchanged. When read through the CoR R03h address, the register content is cleared. A reset sets R02h/R03h = 00h.

**Table 8. Power Event Register** 

|           |     | ADD | RESS |                                      |
|-----------|-----|-----|------|--------------------------------------|
| SYMBOL    | BIT | 02h | 03h  | DESCRIPTION                          |
|           |     | R/W | R/W  |                                      |
| PG_CHG4   | 7   | R   | CoR  | PGOOD change event for port 4        |
| PG_CHG3   | 6   | R   | CoR  | PGOOD change event for port 3        |
| PG_CHG2   | 5   | R   | CoR  | PGOOD change event for port 2        |
| PG_CHG1   | 4   | R   | CoR  | PGOOD change event for port 1        |
| PWEN_CHG4 | 3   | R   | CoR  | Power enable change event for port 4 |
| PWEN_CHG3 | 2   | R   | CoR  | Power enable change event for port 3 |
| PWEN_CHG2 | 1   | R   | CoR  | Power enable change event for port 2 |
| PWEN_CHG1 | 0   | R   | CoR  | Power enable change event for port 1 |

DET\_END\_/CL\_END\_ is set high whenever detection/ classification is completed on the corresponding port. A 1 in any of the CL\_END\_ bits forces R00h[4] to 1. A 1 in any of the DET\_END\_ bits forces R00h[3] to 1. As with any of the other events register, the detect event register

has two addresses. When read through the R04h address, the content of the register is left unchanged. When read through the CoR R05h address, the register content is cleared. A reset sets R04h/R05h = 00h.

**Table 9. Detect Event Register** 

|          |     | ADDI | RESS |                                    |
|----------|-----|------|------|------------------------------------|
| SYMBOL   | BIT | 04h  | 05h  | DESCRIPTION                        |
|          |     | R/W  | R/W  |                                    |
| CL_END4  | 7   | R    | CoR  | Classification completed on port 4 |
| CL_END3  | 6   | R    | CoR  | Classification completed on port 3 |
| CL_END2  | 5   | R    | CoR  | Classification completed on port 2 |
| CL_END1  | 4   | R    | CoR  | Classification completed on port 1 |
| DET_END4 | 3   | R    | CoR  | Detection completed on port 4      |
| DET_END3 | 2   | R    | CoR  | Detection completed on port 3      |
| DET_END2 | 1   | R    | CoR  | Detection completed on port 2      |
| DET_END1 | 0   | R    | CoR  | Detection completed on port 1      |

LD\_DISC\_ is set high whenever the corresponding port shuts down due to detection of load removal. IMAX\_FLT\_ is set high when the port shuts down due to an extended overcurrent event after a successful start-up. A 1 in any of the LD\_DISC\_ bits forces R00h[2] to 1. A 1 in any of the IMAX\_FLT\_ bits forces R00h[5] to 1.

As with any of the other events register, the fault event register has two addresses. When read through the R06h address, the content of the register is left unchanged. When read through the CoR R07h address, the register content is cleared. A reset sets R06h/R07h = 00h.

Table 10. Fault Event Register

|           |     | ADD | RESS |                       |
|-----------|-----|-----|------|-----------------------|
| SYMBOL    | BIT | 06h | 07h  | DESCRIPTION           |
|           |     | R/W | R/W  |                       |
| LD_DISC4  | 7   | R   | CoR  | Disconnect on port 4  |
| LD_DISC3  | 6   | R   | CoR  | Disconnect on port 3  |
| LD_DISC2  | 5   | R   | CoR  | Disconnect on port 2  |
| LD_DISC1  | 4   | R   | CoR  | Disconnect on port 1  |
| IMAX_FLT4 | 3   | R   | CoR  | Overcurrent on port 4 |
| IMAX_FLT3 | 2   | R   | CoR  | Overcurrent on port 3 |
| IMAX_FLT2 | 1   | R   | CoR  | Overcurrent on port 2 |
| IMAX_FLT1 | 0   | R   | CoR  | Overcurrent on port 1 |

If the port remains in current limit or the PGOOD condition is not met at the end of the startup period, the port shuts down and the corresponding STRT\_FLT\_ is set to 1. A 1 in any of the STRT\_FLT\_ bits forces R00h[6] to 1. IVC\_ is set to 1 whenever the port current exceeds the maximum allowed limit for the class (determined during the classification process). A 1 in any of IVC\_ forces R00h[6] to 1. When the CL\_DISC (R17h[2]) is set to 1,

the port also limits the load current according to its class as specified in the *Electrical Characteristics* table. As with any of the other events register, the startup event register has two addresses. When read through the R08h address, the content of the register is left unchanged. When read through the CoR R09h address, the register content is cleared. A reset sets R08h/R09h = 00h.

Table 11. Startup Event Register

|           |     | ADD | RESS |                                   |
|-----------|-----|-----|------|-----------------------------------|
| SYMBOL    | BIT | 08h | 09h  | DESCRIPTION                       |
|           |     | R/W | R/W  |                                   |
| IVC4      | 7   | R   | CoR  | Class overcurrent flag for port 4 |
| IVC3      | 6   | R   | CoR  | Class overcurrent flag for port 3 |
| IVC2      | 5   | R   | CoR  | Class overcurrent flag for port 2 |
| IVC1      | 4   | R   | CoR  | Class overcurrent flag for port 1 |
| STRT_FLT4 | 3   | R   | CoR  | Startup failed on port 4          |
| STRT_FLT3 | 2   | R   | CoR  | Startup failed on port 3          |
| STRT_FLT2 | 1   | R   | CoR  | Startup failed on port 2          |
| STRT_FLT1 | 0   | R   | CoR  | Startup failed on port 1          |

The MAX5965A/MAX5965B continuously monitor the power supplies and set the appropriate bits in the supply event register (Table 12). VDD\_OV/VEE\_OV is set to 1 whenever VDD/VEE exceeds its overvoltage threshold. VDD\_UV/VEE\_UV is set to 1 whenever VDD/VEE falls below its undervoltage threshold.

OSC\_FAIL is set to 1 whenever the amplitude of the oscillator signal at the OSC input falls below a level that might compromise the AC disconnect detection function. OSC\_FAIL generates an interrupt only if at least one of the ACD\_EN (R13h[7:4]) bits is set high.

A thermal shutdown circuit monitors the temperature of the die and resets the MAX5965A/MAX5965B if the temperature exceeds +150°C. TSD is set to 1 after the MAX5965A/MAX5965B return to normal operation. TSD is also set to 1 after every UVLO reset.

When  $V_{DD}$  and/or  $IV_{EE}I$  is below its UVLO threshold, the MAX5965A/MAX5965B are in reset mode and securely holds all ports off. When  $V_{DD}$  and  $IV_{EE}I$  rise to above their respective UVLO thresholds, the device comes out of reset as soon as the last supply crosses the UVLO threshold. The last supply corresponding UV and UVLO bits in the supply event register is set to 1.

A 1 in any supply event register's bits forces R00h[7] to 1. As with any of the other events register, the supply event register has two addresses. When read through the R0Ah address, the content of the register is left unchanged. When read through the CoR R0Bh address, the register content is cleared. A reset sets R0Ah/R0Bh to 00100001b if VDD comes up after VEE or to 00010100b if VEE comes up after VDD.

**Table 12. Supply Event Register** 

|                      |     | ADD | RESS |  |
|----------------------|-----|-----|------|--|
| SYMBOL               | BIT | 0Ah | 0Bh  | DESCRIPTION                                    |
|                      |     | R/W | R/W  |  |
| TSD                  | 7   | R   | CoR  | Overtemperature shutdown                       |
| V <sub>DD_OV</sub>   | 6   | R   | CoR  | V <sub>DD</sub> overvoltage condition          |
| V <sub>DD_UV</sub>   | 5   | R   | CoR  | V <sub>DD</sub> undervoltage condition         |
| VEE_UVLO             | 4   | R   | CoR  | V <sub>EE</sub> undervoltage lockout condition |
| V <sub>EE_OV</sub>   | 3   | R   | CoR  | V <sub>EE</sub> overvoltage condition          |
| VEE_UV               | 2   | R   | CoR  | VEE undervoltage condition                     |
| OSC_FAIL             | 1   | R   | CoR  | Oscillator amplitude is below limit            |
| V <sub>DD_UVLO</sub> | 0   | R   | CoR  | V <sub>DD</sub> undervoltage lockout condition |

The port status register (Table 13a) records the results of the detection and classification at the end of each phase in three encoding bits each. R0Ch contains the detection and classification status of port 1. R0Dh corresponds to port 2, R0Eh corresponds to port 3, and R0Fh corresponds to port 4. Tables 13b and 13c show the detection/classification result decoding charts, respectively. For CLC\_EN = 0, the detection result is shown in Table 13b. When CLC\_EN is set high, the MAX5965A/MAX5965B allow valid detection of high capacitive load of up to 150µF.

When 2-event classification is not enabled (ENx\_CL6 = 0), the classification status is reported in Table 13c. When 2-event classification is enabled (ENx\_CL6 = 1), the CLASS\_[2:0] bits are set to 000 and the classification result is reported in locations R2Ch\_R2Fh.

As a protection, when POFF\_CL (R17h[3], Table 21) is set to 1, the MAX5965A/MAX5965B prohibit turning on power to the port that returns a status 111 after classification. A reset sets 0Ch, 0Dh, 0Eh, and 0Fh = 00h.

### Table 13a. Port Status Registers

| ADDRESS = 0Ch, 0Dh, 0Eh, 0Fh |     |     | DECORIDATION |  |
|------------------------------|-----|-----|--------------|--|
| SYMBOL                       | BIT | R/W | DESCRIPTION  |  |
| Reserved                     | 7   | R   | Reserved     |  |
|                              | 6   | R   | CLASS_[2]    |  |
| CLASS_                       | 5   | R   | CLASS_[1]    |  |
|                              | 4   | R   | CLASS_[0]    |  |
| Reserved                     | 3   | R   | Reserved     |  |
|                              | 2   | R   | DET_ST_[2]   |  |
| DET_ST_                      | 1   | R   | DET_ST_[1]   |  |
|                              | 0   | R   | DET_ST_[0]   |  |

### Table 13b. Detection Result Decoding Chart

| DET_ST_[2:0]<br>(ADDRESS = 0Ch, 0Dh, 0Eh, 0Fh) | DETECTED | DESCRIPTION  |
|--|----------|--|
| 000  | None     | Detection status unknown   |
| 001  | DCP      | Positive DC supply connected at the port (VAGND - VOUT_ < 1V)                      |
| 010  | HIGH CAP | High capacitance at the port (> 8.5µF)   |
| 011  | RLOW     | Low resistance at the port, R <sub>PD</sub> < 15k $\Omega$                         |
| 100  | DET_OK   | Detection pass, $15k\Omega < R_{PD} < 33k\Omega$                                   |
| 101  | RHIGH    | High resistance at the port, $R_{PD} > 33k\Omega$                                  |
| 110  | OPEN0    | Open port (I < 10μA)   |
| 111  | DCN      | Negative DC supply connected to the port (V <sub>OUT</sub> - V <sub>EE</sub> < 2V) |

## Table 13c. Classification Result Decoding Chart

| CLASS_[2:0]<br>(ADDRESS = 0Ch, 0Dh, 0Eh, 0Fh) | CLASS RESULT             |
|---|--------------------------|
| 000   | Unknown                  |
| 001   | 1                        |
| 010   | 2                        |
| 011   | 3                        |
| 100   | 4                        |
| 101   | 5                        |
| 110   | 0                        |
| 111   | Current limit (> ICILIM) |

MIXIM

PGOOD\_ is set to 1 (Table 14) at the end of the power-up startup period if the power-good condition is met (0 < (Vout\_ - Vee) < PGth). The power-good condition must remain valid for more than tpgood to assert PGOOD\_. PGOOD\_ is reset to 0 whenever the output falls out of the power-good condition. A fault condition immediately forces PGOOD\_ low.

PWR\_EN\_ is set to 1 when the port power is turned on. PWR\_EN\_ resets to 0 as soon as the port turns off. Any transition of PGOOD\_ and PWR\_EN\_ bits set the corresponding bit in the power event registers R02h/R03h (Table 8). A reset sets R10h = 00h.

**Table 14. Power Status Register** 

| ADDRESS = 10h |     |     | DESCRIPTION                    |  |
|---------------|-----|-----|--------------------------------|--|
| SYMBOL        | BIT | R/W | DESCRIPTION                    |  |
| PGOOD4        | 7   | R   | Power-good condition on port 4 |  |
| PGOOD3        | 6   | R   | Power-good condition on port 3 |  |
| PGOOD2        | 5   | R   | Power-good condition on port 2 |  |
| PGOOD1        | 4   | R   | Power-good condition on port 1 |  |
| PWR_EN4       | 3   | R   | Power is enabled on port 4     |  |
| PWR_EN3       | 2   | R   | Power is enabled on port 3     |  |
| PWR_EN2       | 1   | R   | Power is enabled on port 2     |  |
| PWR_EN1       | 0   | R   | Power is enabled on port 1     |  |

A3, A2, A1, A0 (Table 15) represent the 4 LSBs of the MAX5965A/MAX5965B address (Table 4). During a reset, the device latches into R11h. These 4 bits

address from the corresponding inputs as well as the state of the MIDSPAN and AUTO inputs. Changes to those inputs during normal operation are ignored.

**Table 15. Address Input Status Register** 

| ADDRESS = 11h |     |     | DESCRIPTION                              |  |
|---------------|-----|-----|--|--|
| SYMBOL        | BIT | R/W | DESCRIPTION                              |  |
| Reserved      | 7   | R   | Reserved                                 |  |
| Reserved      | 6   | R   | Reserved                                 |  |
| A3            | 5   | R   | Device address, A3 pin latched-in status |  |
| A2            | 4   | R   | Device address, A2 pin latched-in status |  |
| A1            | 3   | R   | Device address, A1 pin latched-in status |  |
| A0            | 2   | R   | Device address, A0 pin latched-in status |  |
| MIDSPAN       | 1   | R   | MIDSPAN input's latched-in status        |  |
| AUTO          | 0   | R   | AUTO input's latched-in status           |  |

The MAX5965A/MAX5965B use 2 bits for each port to set the mode of operation. Set the modes according to Table 16a and 16b.

A reset sets R12h = AAAAAAAAb where A represents the latched-in state of the AUTO input prior to the reset. Use software to change the mode of operation. Software resets of ports (RESET\_P\_ bit, Table 23) do not affect the mode register.

Table 16a. Operating Mode Register

| ADDRI  | ESS = 12h |     | DESCRIPTION        |
|--------|-----------|-----|--------------------|
| SYMBOL | BIT       | R/W | DESCRIPTION        |
| P4_M1  | 7         | R/W | MODE[1] for port 4 |
| P4_M0  | 6         | R/W | MODE[0] for port 4 |
| P3_M1  | 5         | R/W | MODE[1] for port 3 |
| P3_M0  | 4         | R/W | MODE[0] for port 3 |
| P2_M1  | 3         | R/W | MODE[1] for port 2 |
| P2_M0  | 2         | R/W | MODE[0] for port 2 |
| P1_M1  | 1         | R/W | MODE[1] for port 1 |
| P1_M0  | 0         | R/W | MODE[0] for port 1 |

**Table 16b. Operating Mode Status** 

| MODE | DESCRIPTION |
|------|-------------|
| 00   | Shutdown    |
| 01   | Manual      |
| 10   | Semi-auto   |
| 11   | Auto        |

Setting DCD\_EN\_ to 1 enables the DC load disconnect detection feature (Table 17). Setting ACD\_EN\_ to 1 enables the AC load disconnect feature. If enabled, the load disconnect detection starts during power mode

and after startup when the corresponding PGOOD\_ bit in register R10h (Table 14) goes high. A reset sets R13h = 0000AAAAb where A represents the latched-in state of the AUTO input prior to the reset.

**Table 17. Load Disconnect Detection Enable Register** 

| ADDRESS = 13h |     |     | DESCRIPTION                              |  |
|---------------|-----|-----|--|--|
| SYMBOL        | BIT | R/W | DESCRIPTION                              |  |
| ACD_EN4       | 7   | R/W | Enable AC disconnect detection on port 4 |  |
| ACD_EN3       | 6   | R/W | Enable AC disconnect detection on port 3 |  |
| ACD_EN2       | 5   | R/W | Enable AC disconnect detection on port 2 |  |
| ACD_EN1       | 4   | R/W | Enable AC disconnect detection on port 1 |  |
| DCD_EN4       | 3   | R/W | Enable DC disconnect detection on port 4 |  |
| DCD_EN3       | 2   | R/W | Enable DC disconnect detection on port 3 |  |
| DCD_EN2       | 1   | R/W | Enable DC disconnect detection on port 2 |  |
| DCD_EN1       | 0   | R/W | Enable DC disconnect detection on port 1 |  |

Setting DET\_EN\_/CLASS\_EN\_ to 1 (Table 18) enables load detection/classification, respectively. Detection always has priority over classification. To perform classification without detection, set the DET\_EN\_ bit low and CLASS\_EN\_ bit high.

In manual mode, R14h works like a pushbutton. Set the bits high to begin the corresponding routine. The bit clears after the routine finishes.

When entering auto mode, R14h defaults to FFh. When entering semi or manual modes, R14h defaults to 00h. A reset or power-up sets R14h = AAAAAAAb where A represents the latched-in state of the AUTO input prior to the reset.

Table 18. Detection and Classification Enable Register

| ADDRESS = 14h |     |     | DESCRIPTION                     |  |
|---------------|-----|-----|---------------------------------|--|
| SYMBOL        | BIT | R/W | DESCRIPTION                     |  |
| CLASS_EN4     | 7   | R/W | Enable classification on port 4 |  |
| CLASS_EN3     | 6   | R/W | Enable classification on port 3 |  |
| CLASS_EN2     | 5   | R/W | Enable classification on port 2 |  |
| CLASS_EN1     | 4   | R/W | Enable classification on port 1 |  |
| DET_EN4       | 3   | R/W | Enable detection on port 4      |  |
| DET_EN3       | 2   | R/W | Enable detection on port 3      |  |
| DET_EN2       | 1   | R/W | Enable detection on port 2      |  |
| DET_EN1       | 0   | R/W | Enable detection on port 1      |  |

EN\_HP\_CL\_, EN\_HP\_ALL together with CL\_DISC (R17h[2]) and ENx\_CL6 (R1Ch[7:4]) are used to program the high-power mode. See Table 3 for details.

Setting BCKOFF\_ to 1 (Table 19) enables cadence timing on each port where the port backs off and waits 2.2s after each failed load discovery detection. The

IEEE 802.3af standard requires a PSE that delivers power through the spare pairs (midspan PSE) to have cadence timing.

A reset or power-up sets R15h = 0000XXXXb where 'X' is the logic AND of the MIDSPAN and AUTO inputs.

Table 19. Backoff and High-Power Enable Register

| ADDRESS = 15h |     |     | DESCRIPTION                     |  |
|---------------|-----|-----|---------------------------------|--|
| SYMBOL        | BIT | R/W | DESCRIPTION                     |  |
| EN_HP_ALL     | 7   | R/W | High-power detection enabled    |  |
| EN_HP_CL6     | 6   | R/W | Class 6 PD high-power enabled   |  |
| EN_HP_CL5     | 5   | R/W | Class 5 PD high-power enabled   |  |
| EN_HP_CL4     | 4   | R/W | Class 4 PD high-power enabled   |  |
| BCKOFF4       | 3   | R/W | Enable cadence timing on port 4 |  |
| BCKOFF3       | 2   | R/W | Enable cadence timing on port 3 |  |
| BCKOFF2       | 1   | R/W | Enable cadence timing on port 2 |  |
| BCKOFF1       | 0   | R/W | Enable cadence timing on port 1 |  |

TSTART[1,0] (Table 20a) programs the startup timers. Startup time is the time the port is allowed to be in current limit during startup. TFAULT[1,0] programs the fault time. Fault time is the time allowed for the port to be in current limit during normal operation. RSTR[1,0] programs the discharge rate of the TFAULT\_ counter and effectively sets the time the port remains off after an overcurrent fault. TDISC[1,0] programs the load disconnect detection time. The device turns off power to the port if it fails to provide a minimum power maintenance signal for longer than the load disconnect detection time (tDISC).

Set the bits in R16h to scale the tSTART, tFAULT, and tDISC to a multiple of their nominal value specified in the *Electrical Characteristics* table.

When the MAX5965A/MAX5965B shut down a port due to an extended overcurrent condition (either during startup or normal operation), if RSTR\_EN is set high, the part does not allow the port to power back on before the restart timer (Table 20b) returns to zero. This effectively sets a minimum duty cycle that protects the external MOSFET from overheating during prolonged output overcurrent conditions. A reset sets R16h = 00h.

### Table 20a. Timing Configuration Register

| ADDRESS = 16h |     |     | DESCRIPTION                             |  |
|---------------|-----|-----|---|--|
| SYMBOL        | BIT | R/W | DESCRIPTION                             |  |
| RSTR[1]       | 7   | R/W | Restart timer programming bit 1         |  |
| RSTR[0]       | 6   | R/W | Restart timer programming bit 0         |  |
| TSTART[1]     | 5   | R/W | Startup timer programming bit 1         |  |
| TSTART[0]     | 4   | R/W | Startup timer programming bit 0         |  |
| TFAULT[1]     | 3   | R/W | Overcurrent timer programming bit 1     |  |
| TFAULT[0]     | 2   | R/W | Overcurrent timer programming bit 0     |  |
| TDISC[1]      | 1   | R/W | Load disconnect timer programming bit 1 |  |
| TDISC[0]      | 0   | R/W | Load disconnect timer programming bit 0 |  |

### Table 20b. Startup, Fault, and Load Disconnect Timer Values for Timing Register

| BIT [1:0]<br>(ADDRESS = 16h) | RSTR        | tpisc                                  | <sup>t</sup> START               | †FAULT                           |
|------------------------------|-------------|--|----------------------------------|----------------------------------|
| 00                           | 16 x tfault | t <sub>DISC</sub> nominal (350ms, typ) | tstart nominal (60ms, typ)       | tFAULT nominal (60ms, typ)       |
| 01                           | 32 x tfault | 1/4 x t <sub>DISC</sub> nominal        | 1/2 x t <sub>START</sub> nominal | 1/2 x t <sub>FAULT</sub> nominal |
| 10                           | 64 x tfault | 1/2 x t <sub>DISC</sub> nominal        | 2 x t <sub>START</sub> nominal   | 2 x t <sub>FAULT</sub> nominal   |
| 11                           | 0 x tfault  | 2 x t <sub>DISC</sub> nominal          | 4 x t <sub>START</sub> nominal   | 4 x t <sub>FAULT</sub> nominal   |

Setting CL\_DISC to 1 (Table 21) enables port over class current protection, where the MAX5965A/MAX5965B scales down the overcurrent limit (VFLT\_LIM) according to the port classification status. This feature provides protection to the system against PDs that violate their maximum class current allowance.

The MAX5965 is programmed to switch to a high-power configuration and HP\_TIME is low, the higher current setting is enabled only after a successful startup so that the PD powers up as a normal 15W device. If HP\_TIME is set together with EN HP ALL, the higher current setting will

be active before startup. For Classes 4, 5, and 6, the corresponding enable bit in register R15h must be set together with EN\_HP\_ALL. In any other cases, the current level defaults to Class 0.

CL\_DISC, together with EN\_HP\_CL\_ (R15h[6:4]), EN\_HP\_ALL (R15h[7]), and ENx\_CL6 (R1Ch[7:4]) are used to program the high-power mode. See Table 3 for details.

Setting OUT\_ISO high (Table 21), forces DET\_ to a high-impedance state.

A reset sets R17h = 0xC0.

Table 21. Miscellaneous Configurations 1 Register

| ADDRESS = 17h |     |  | DESCRIPTION  |
|---------------|-----|--|--|
| SYMBOL        | BIT | R/W  | DESCRIPTION  |
| INT_EN        | 7   | R/W  | A logic-high enables INT functionality   |
| RSTR_EN       | 6   | R/W  | A logic-high enables the autorestart protection time off (as set by the RSTR[1:0] bits)                                      |
| Reserved      | 5   | _  | Reserved   |
| Reserved      | 4   | _  | Reserved   |
| POFF_CL       | 3   | R A logic-high prevents power-up after a classification failure (I > 50mA, valid only in mode) |  |
| CL_DISC       | 2   | R/W  | A logic-high enables reduced current-limit voltage threshold (V <sub>FLT_LIM</sub> ) according to port classification result |
| OUT_ISO       | 1   | R/W  | Forces DET_ to high impedance. Does not interfere with other circuit operation.  |
| HP_TIME       | 0   | R/W  | Enables high power after startup.  |

Power-enable pushbutton for semi and manual modes is found in Table 22. Setting PWR\_ON\_ to 1 turns on power to the corresponding port. Setting PWR\_OFF\_ to 1 turns off power to the port. PWR\_ON\_ is ignored when the port is already powered and during shutdown. PWR\_OFF\_ is ignored when the port is already off and

during shutdown. After execution, the bits reset to 0. During detection or classification, if PWR\_ON\_ goes high, the MAX5965A/MAX5965B gracefully terminate the current operation and turn on power to the port. The MAX5965A/MAX5965B ignore the PWR\_ON\_ in auto mode. A reset sets R19h = 00h.

Table 22. Power-Enable Pushbuttons Register

| ADDR     | RESS = 19h |     | DESCRIPTION                    |
|----------|------------|-----|--------------------------------|
| SYMBOL   | BIT        | R/W | DESCRIPTION                    |
| PWR_OFF4 | 7          | W   | A logic-high powers off port 4 |
| PWR_OFF3 | 6          | W   | A logic-high powers off port 3 |
| PWR_OFF2 | 5          | W   | A logic-high powers off port 2 |
| PWR_OFF1 | 4          | W   | A logic-high powers off port 1 |
| PWR_ON4  | 3          | W   | A logic-high powers on port 4  |
| PWR_ON3  | 2          | W   | A logic-high powers on port 3  |
| PWR_ON2  | 1          | W   | A logic-high powers on port 2  |
| PWR_ON1  | 0          | W   | A logic-high powers on port 1  |

Writing a 1 to CLR\_INT (Table 23) clears all the event registers and the corresponding interrupt bits in register R00h. Writing a 1 to RESET\_P\_ turns off power to the corresponding port and resets only the status and

event registers of that port. After execution, the bits reset to 0. Writing a 1 to RESET\_IC causes a global software reset, after which the register map is set back to its reset state. A reset sets R1Ah = 00h.

#### Table 23. Global Pushbuttons Register

| ADDRE    | SS = 1Ah |     | DESCRIPTION                               |
|----------|----------|-----|---|
| SYMBOL   | BIT      | R/W | DESCRIPTION                               |
| CLR_INT  | 7        | W   | A logic-high clears all interrupts        |
| Reserved | 6        | _   | Reserved                                  |
| Reserved | 5        | _   | Reserved                                  |
| RESET_IC | 4        | W   | A logic-high resets the MAX5965A/MAX5965B |
| RESET_P4 | 3        | W   | A logic-high resets port 4                |
| RESET_P3 | 2        | W   | A logic-high resets port 3                |
| RESET_P2 | 1        | W   | A logic-high resets port 2                |
| RESET_P1 | 0        | W   | A logic-high resets port 1                |

The ID register (Table 24) keeps track of the device ID number and revision. The MAX5965A/MAX5965B's

 $ID\_CODE[4:0] = 11001b$ . Contact the factory for REV[2:0] value.

Table 24. ID Register

| ADDR    | ESS = 1Bh |     | DESCRIPTION |
|---------|-----------|-----|-------------|
| SYMBOL  | BIT       | R/W | DESCRIPTION |
|         | 7         | R   | ID_CODE[4]  |
|         | 6         | R   | ID_CODE[3]  |
| ID_CODE | 5         | R   | ID_CODE[2]  |
|         | 4         | R   | ID_CODE[1]  |
|         | 3         | R   | ID_CODE[0]  |
|         | 2         | R   | REV[2]      |
| REV     | 1         | R   | REV[1]      |
|         | 0         | R   | REV[0]      |

Enable 2-event classification for a port by setting the corresponding ENx\_CL6 bit (Table 25). When the bit is enabled, the classification cycle will be repeated three times at 21.3ms intervals. The device keeps the output voltage around -9V between each cycle. The repetition of the classification cycles enables discovering of class 6 PDs. The ENx\_CL6 bit is active only in auto- or semi-mode.

**Note:** Performing three consecutive classifications in manual mode is not the same as performing 2-event classification in semi or auto mode.

Enable the SMODE function (Table 25) by setting EN\_WHDOG (R1Fh[7]) to 1. The SMODE\_ bit goes high when the watchdog counter reaches zero and the port(s) switch over to hardware-controlled mode. SMODE\_ also goes high each and every time the software tries to power on a port, but is denied since the port is in hardware mode. A reset sets R1Ch = 00h.

Table 25. SMODE and 2-Event Enable Register

| ADI     | DRESS = 10 | Ch            |                                       |  |
|---------|------------|---------------|---------------------------------------|--|
| SYMBOL  | BIT        | CoR or<br>R/W | DESCRIPTION                           |  |
| EN4_CL6 | 7          | R/W           | Port 4 2-event classification enabled |  |
| EN3_CL6 | 6          | R/W           | Port 3 2-event classification enabled |  |
| EN2_CL6 | 5          | R/W           | Port 2 2-event classification enabled |  |
| EN1_CL6 | 4          | R/W           | Port 1 2-event classification enabled |  |
| SMODE4  | 3          | CoR           | Port 4 hardware control flag          |  |
| SMODE3  | 2          | CoR           | Port 3 hardware control flag          |  |
| SMODE2  | 1          | CoR           | Port 2 hardware control flag          |  |
| SMODE1  | 0          | CoR           | Port 1 hardware control flag          |  |

Set EN\_WHDOG (R1Fh[7]) to 1 to enable the watchdog function. When activated, the watchdog timer counter, WDTIME[7:0], continuously decrements toward zero once every 164ms. Once the counter reaches zero (also called watchdog expiry), the MAX5965A/MAX5965B enter hardware-controlled mode and each port shifts to a mode set by the HWMODE\_ bit in register R1Fh (Table 27). Use software to set WDTIME (Table 26) and continuously set this register to some nonzero value before the register reaches zero to pre-

vent a watchdog expiry. In this way, the software gracefully manages the power to ports upon a system crash or switchover.

While in hardware-controlled mode, the MAX5965A/MAX5965B ignore all requests to turn the power on and the flag SMODE\_ indicates that the hardware has taken control of the MAX5965A/MAX5965B operation. In addition, the software is not allowed to change the mode of operation in hardware-controlled mode. A reset sets R1Eh = 00h.

**Table 26. Watchdog Register** 

| ADDI      | RESS = 1Eh |     | DESCRIPTION |
|-----------|------------|-----|-------------|
| SYMBOL    | BIT        | R/W | DESCRIPTION |
|           | 7          | R/W | WDTIME[7]   |
|           | 6          | R/W | WDTIME[6]   |
|           | 5          | R/W | WDTIME[5]   |
| ) A/DTIME | 4          | R/W | WDTIME[4]   |
| WDTIME    | 3          | R/W | WDTIME[3]   |
|           | 2          | R/W | WDTIME[2]   |
|           | 1          | R/W | WDTIME[1]   |
|           | 0          | R/W | WDTIME[0]   |

Setting EN\_WHDOG (Table 27) high activates the watchdog counter. When the counter reaches zero, the port switches to the hardware-controlled mode determined by the corresponding HWMODE\_ bit. A low in HWMODE\_ switches the port into shutdown by setting

the bits in register R12h to 00. A high in HWMODE\_switches the port into auto mode by setting the bits in register R12h to 11. If WD\_INT\_EN is set, an interrupt is sent if any of the SMODE bits are set. A reset sets R1Fh = 00h

Table 27. Switch Mode Register

| ADDF      | ADDRESS = 1Fh |     | DECORIDATION   |  |
|-----------|---------------|-----|--|--|
| SYMBOL    | BIT           | R/W | DESCRIPTION  |  |
| EN_WHDOG  | 7             | R/W | A logic-high enables the watchdog function   |  |
| WD_INT_EN | 6             | R/W | Enables interrupt on SMODE_ bits   |  |
| Reserved  | 5             | _   | Reserved   |  |
| Reserved  | 4             | _   | Reserved   |  |
| HWMODE4   | 3             | R/W | Port 4 switches to AUTO if logic-high and to SHUTDOWN if logic-low when watchdog timer expires |  |
| HWMODE3   | 2             | R/W | Port 3 switches to AUTO if logic-high and to SHUTDOWN if logic-low when watchdo expires        |  |
| HWMODE2   | 1             | R/W | Port 2 switches to AUTO if logic-high and to SHUTDOWN if logic-low when watchdog timer expires |  |
| HWMODE1   | 0             | R/W | Port 1 switches to AUTO if logic-high and to SHUTDOWN if logic-low when watchdog timer expires |  |

The CLC\_EN enables the large capacitor detection feature. When CLC\_EN is set the device can recognize a capacitor load up to 150µF. If the CLC\_EN is reset, the MAX5965A/MAX5965B perform normal detection.

AC\_TH allows programming of the threshold of the AC disconnect comparator. The threshold is defined as a current since the comparators verify that the peak of the current pulses sensed at the DET\_ input exceed a preset threshold. The current threshold is defined as follows:

 $IAC\_TH = 226.68\mu A + 28.33 \times NAC\_TH$  where NAC\_TH is the decimal value of AC\_TH.

When set low, DET\_BY inhibits port power-on if the discovery detection was bypassed in auto mode. When set high, DET\_BY allows the device to turn on power to a non-IEEE 802.3af load without doing detection. If

OSCF\_RS is set high, the OSC\_FAIL bit is ignored. A

reset or power-up sets R23h = 04h. Default  $IAC_TH$  is 340µA.

Table 28. Program Register

| ADDRESS = 23h |     |     | DESCRIPTION                             |  |
|---------------|-----|-----|---|--|
| SYMBOL        | BIT | R/W | DESCRIPTION                             |  |
| Reserved      | 7   | _   | Reserved                                |  |
| Reserved      | 6   | _   | Reserved                                |  |
| CLC_EN        | 5   | R/W | Large capacitor detection enable        |  |
| DET_BY        | 4   | R/W | Enables skipping detection in AUTO mode |  |
| OSCF_RS       | 3   | R/W | OSC_FAIL reset bit                      |  |
|               | 2   | R/W | AC_TH[2]                                |  |
| AC_TH         | 1   | R/W | AC_TH[1]                                |  |
|               | 0   | R/W | AC_TH[0]                                |  |

HP[2:0] programs the default power setting that is written upon the discovery of a class 4, 5, or 6 PD. A reset or power-up sets R24h = 00h.

The IVEE bits enable the current-limit scaling (Table 30). This feature is used to reduce the current limit for systems running at higher voltage to maintain the desired output power. Table 31 sets the current-limit scaling register. A reset or power-up sets R29h = 00h.

Table 29. High-Power Mode Register

| ADDRESS = 24h |     |     | DESCRIPTION |
|---------------|-----|-----|-------------|
| SYMBOL        | BIT | R/W | DESCRIPTION |
| Reserved      | 7   | _   | Reserved    |
|               | 6   | R/W | HP[2]       |
| HP            | 5   | R/W | HP[1]       |
|               | 4   | R/W | HP[0]       |
|               | 3   | _   | Reserved    |
| Reserved      | 2   | _   | Reserved    |
|               | 1   | _   | Reserved    |
|               | 0   | _   | Reserved    |

 Table 30. Miscellaneous Configurations 2

| ADDR     | ESS = 291 | DESCRIPTION |             |
|----------|-----------|-------------|-------------|
| SYMBOL   | BIT       | R/W         | DESCRIPTION |
|          | 7         | _           | Reserved    |
|          | 6         | _           | Reserved    |
| Reserved | 5         | _           | Reserved    |
|          | 4         | _           | Reserved    |
|          | 3         | _           | Reserved    |
| LSC_EN   | 2         | _           | LSC_EN      |
| IVEE     | 1         | R/W         | IVEE[1]     |
| IVEE     | 0         | R/W         | IVEE[0]     |

**Table 31. Current-Limit Scaling Register** 

| IVEE[1:0]<br>(ADDRESS = 29h) | CURRENT LIMIT (%) |
|------------------------------|-------------------|
| 00                           | Default           |
| 01                           | -5                |
| 10                           | -10               |
| 11                           | -15               |

The three ICUT\_ bits (Tables 32a and 32b) allow programming of the current-limit and overcurrent thresholds in excess of the IEEE 802.3af standard limit. The MAX5965A/MAX5965B can automatically set the ICUT register or can be manually written to by the software (see Table 3).

Class 1 and 2 limits can also be programmed by software independently from the classification status. See Table 3. A reset or power-up sets R2Ah = R2Bh = 00h.

#### Table 32a. ICUT Registers 1 and 2

| ADDF     | RESS = 2Ah |     | DESCRIPTION |
|----------|------------|-----|-------------|
| SYMBOL   | BIT        | R/W | DESCRIPTION |
| Reserved | 7          | _   | Reserved    |
| ICUT2    | 6          | R/W | ICUT2[2]    |
|          | 5          | R/W | ICUT2[1]    |
|          | 4          | R/W | ICUT2[0]    |
| Reserved | 3          | _   | Reserved    |
|          | 2          | R/W | ICUT1[2]    |
| ICUT1    | 1          | R/W | ICUT1[1]    |
|          | 0          | R/W | ICUT1[0]    |

#### Table 32b. ICUT Registers 3 and 4

| ADDRESS = 2Bh |     |     | DECORIDATION |  |  |  |  |  |
|---------------|-----|-----|--------------|--|--|--|--|--|
| SYMBOL        | BIT | R/W | DESCRIPTION  |  |  |  |  |  |
| Reserved      | 7   | _   | Reserved     |  |  |  |  |  |
|               | 6   | R/W | ICUT4[2]     |  |  |  |  |  |
| ICUT4         | 5   | R/W | ICUT4[1]     |  |  |  |  |  |
|               | 4   | R/W | ICUT4[0]     |  |  |  |  |  |
| Reserved      | 3   | _   | Reserved     |  |  |  |  |  |
|               | 2   | R/W | ICUT3[2]     |  |  |  |  |  |
| ICUT3         | 1   | R/W | ICUT3[1]     |  |  |  |  |  |
|               | 0   | R/W | ICUT3[0]     |  |  |  |  |  |

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Table 32c. ICUT Register Bit Values for Current-Limit Threshold

| ICUT_[2:0] (ADDRESS = 2Ah, 2Bh) | SCALE FACTOR | TYPICAL CURRENT-LIMIT THRESHOLD (mA) |
|---------------------------------|--------------|--------------------------------------|
| 000                             | 1x           | 375                                  |
| 001                             | 1.5x         | 563                                  |
| 010                             | 1.75x        | 656                                  |
| 011                             | 2x           | 750                                  |
| 100                             | 2.25x        | 844                                  |
| 101                             | 2.5x         | 938                                  |
| 110                             | 0.3x         | Class 1                              |
| 111                             | 0.53x        | Class 2                              |

#### **Table 33a. Classification Status Registers**

| ADDRESS = 2Ch, 2Dh, 2Eh, 2Fh |     |     | DESCRIPTION |
|------------------------------|-----|-----|-------------|
| SYMBOL                       | BIT | R/W | DESCRIPTION |
| Decembed                     | 7   | _   | Reserved    |
| Reserved                     | 6   | _   | Reserved    |

#### **Table 33b. Class Sequence States**

| CLS_[5:0]<br>(ADDRESS = 2Ch, 2Dh,<br>2Eh, 2Fh) | CLASS<br>SEQUENCE | ICUT_[2:0] |
|--|-------------------|------------|
| 000000   | 000 (Class 0)     | 000        |
| 000001   | 001               | 000        |
| 000010   | 010               | HP[2:0]    |
| 000011   | 011               | 000        |
| 000100   | 100               | 000        |
| 000101   | 101               | HP[2:0]    |
| 000110   | 110               | 000        |
| 000111   | 111 (Class 1)     | 110        |
| 001000   | 002               | 000        |
| 001001   | 020               | 011        |
| 001010   | 022               | 000        |
| 001011   | 200               | 000        |
| 001100   | 202               | 100        |
| 001101   | 220               | 000        |
| 001110   | 222 (Class 2)     | 111        |
| 001111   | 003               | 000        |
| 010000   | 030               | 010        |
| 010001   | 033               | 000        |
| 010010   | 300               | 000        |
| 010011   | 303               | 010        |
| 010100   | 330               | 000        |

| CLS_[5:0]<br>(ADDRESS = 2Ch, 2Dh,<br>2Eh, 2Fh) | CLASS<br>SEQUENCE | ICUT_[2:0] |
|--|-------------------|------------|
| 010101   | 333 (Class 3)     | 000        |
| 010110   | 004               | 000        |
| 010111   | 040               | 000        |
| 011000   | 044               | 000        |
| 011001   | 400               | 000        |
| 011010   | 404               | 000        |
| 011011   | 440               | 000        |
| 011100   | 444 (Class 4)     | HP[2:0]    |
| 011101   | 005               | 000        |
| 011110   | 050               | 000        |
| 011111   | 055               | 000        |
| 100000   | 500               | 000        |
| 100001   | 505               | 000        |
| 100010   | 550               | 000        |
| 100011   | 555 (Class 5)     | HP[2:0]    |
| 100100   | Reserved          | 000        |
| 100101   | Reserved          | 000        |
| 100110   | Reserved          | 000        |
| 100111   | Reserved          | 000        |
| 101000   | Illegal           | 000        |
| 101001   | Illegal           | 000        |

Table 33b. Class Sequence States (continued)

| CLS_[5:0]<br>(ADDRESS = 2Ch, 2Dh,<br>2Eh, 2Fh) | CLASS<br>SEQUENCE | ICUT_[2:0] |
|--|-------------------|------------|
| 101010   | Illegal           | 000        |
| 101011   | Illegal           | 000        |
| 101100   | Illegal           | 000        |
| 101101   | Illegal           | 000        |
| 101110   | Illegal           | 000        |
| 101111   | Illegal           | 000        |
| 110000   | Reserved          | 000        |
| 110001   | Reserved          | 000        |
| 110010   | Reserved          | 000        |
| 110011   | Reserved          | 000        |
| 110100   | Reserved          | 000        |

When the ENx\_CL6 (R1Ch[7:4]) bits are set, 2-event classification is enabled. Classification is repeated three times and the classification results are set according to Table 33b.

A Class 6 PD is defined by any sequence of the type [00x, 0x0, 0xx, x00, x0x, xx0] where 'x' can be 1, 2, 3, 4, or 5. All sequences made by the same class result define the class itself (for example, 222 defines Class 2). Any other sequence will be considered illegal and coded as 101xxx. For example, a sequence 232 or 203 will be illegal. The illegal sequences all default to class 0. A reset or power-up sets R2Ch = R2Dh = R2Eh = R2Fh = 00h.

The MAX5965A/MAX5965B provide current readout for each port during classification and normal power mode. The current per port information is separated

| CLS_[5:0]<br>(ADDRESS = 2Ch, 2Dh,<br>2Eh, 2Fh) | CLASS<br>SEQUENCE | ICUT_[2:0] |
|--|-------------------|------------|
| 110101   | Reserved          | 000        |
| 110110   | Reserved          | 000        |
| 110111   | Reserved          | 000        |
| 111000   | Reserved          | 000        |
| 111001   | Reserved          | 000        |
| 111010   | Reserved          | 000        |
| 111011   | Reserved          | 000        |
| 111100   | Reserved          | 000        |
| 111101   | Reserved          | 000        |
| 111110   | Reserved          | 000        |
| 111111   | Reserved          | 000        |

into 9 bits. They are organized into two consecutive registers for each one of the ports. The information can be quickly retrieved using the autoincrement option of the address pointer. To avoid the LSB register changing while reading the MSB, the information is frozen once the addressing byte points to any of the current readout registers.

During power mode, the current value can be calculated as

$$I_{PORT} = N_{IPD} \times 2mA$$

During classification, the current is

where  $N_{IPD}$  is the decimal value of the 9-bit word. The ADC saturates both at full scale and at zero. A reset sets R30h to R37h = 00h.

**Table 34. Current Registers** 

| ADDRESS = 301<br>35h, | n, 31h, 32h,<br>36h, 37h | 33h, 34h, | DESCRIPTION     |  |  |  |  |  |
|-----------------------|--------------------------|-----------|-----------------|--|--|--|--|--|
| SYMBOL                | BIT                      | R/W       |                 |  |  |  |  |  |
|                       | 7                        | RO        | IPD_[8]         |  |  |  |  |  |
|                       | 6                        | RO        | IPD_[7]         |  |  |  |  |  |
|                       | 5                        | RO        | IPD_[6]         |  |  |  |  |  |
| IPD_                  | 4                        | RO        | IPD_[5]         |  |  |  |  |  |
| IFD_                  | 3                        | RO        | IPD_[4]         |  |  |  |  |  |
|                       | 2                        | RO        | IPD_[3]         |  |  |  |  |  |
|                       | 1                        | RO        | IPD_[2]         |  |  |  |  |  |
|                       | 0                        | RO        | IPD_[1]/IPD_[0] |  |  |  |  |  |

**Table 35. Register Summary** 

| ADDR       | REGISTER NAME                          | R/W       | PORT | BIT 7      | BIT 6        | BIT 5        | BIT 4                | BIT 3               | BIT 2              | BIT 1      | BIT 0                 | RESET<br>STATE    |
|------------|--|-----------|------|------------|--------------|--------------|----------------------|---------------------|--------------------|------------|-----------------------|-------------------|
| INTERF     | RUPTS                                  |           |      | •          |              | •            | •                    |                     | •                  | •          | •                     | •                 |
| 00h        | Interrupt                              | RO        | G    | SUP_FLT    | TSTR_FLT     | IMAX_FLT     | CL_END               | DET_END             | LD_DISC            | PG_INT     | PEN_INT               | 0000,0000         |
| 01h        | Interrupt Mask                         | R/W       | G    | MASK7      | MASK6        | MASK5        | MASK4                | MASK3               | MASK2              | MASK1      | MASK0                 | AAA0,0A00         |
| EVENT      |  |           |      | ı          |              | ı            | ı                    | ı                   | I                  | ı          | ı                     |                   |
| 02h        | Power Event                            | RO        | 4321 |            |              |              |                      | PWEN_               | PWEN_              | PWEN       | PWEN                  | 0000,0000         |
| 03h        | Power Event CoR                        | CoR       | _    | PG_CHG4    | PG_CHG3      | PG_CHG2      | PG_CHG1              | CHG4                | CHG3               | CHG2       | CHG1                  | _                 |
| 04h        | Detect Event                           | RO        | 4321 |            |              |              |                      |                     |                    |            |                       | 0000,0000         |
| 05h        | Detect Event CoR                       | CoR       |      | CL_END4    | CL_END3      | CL_END2      | CL_END1              | DET_END4            | DET_END3           | DET_END2   | DET_END1              | _                 |
| 06h        | Fault Event                            | RO        | 4321 |            |              |              |                      |                     |                    |            |                       | 0000,0000         |
| 07h        | Fault Event CoR                        | CoR       | _    | LD_DISC4   | LD_DISC3     | LD_DISC2     | LD_DISC1             | IMAX_FLT4           | IMAX_FLT3          | IMAX_FLT2  | IMAX_FLT1             | _                 |
| 08h        | Startup Event                          | RO        | 4321 |            |              |              |                      |                     |                    |            |                       | 0000,0000         |
| 09h        | Startup Event CoR                      | CoR       |      | IVC4       | IVC3         | IVC2         | IVC1                 | STRT_FLT4           | STRT_FLT3          | STRT_FLT2  | STRT_FLT1             | _                 |
| 0Ah        | Supply Event                           | RO        | 4321 |            |              |              |                      |                     |                    |            |                       | _                 |
| 0Bh        | Supply Event CoR                       | CoR       | _    | TSD        | $V_{DD\_OV}$ | $V_{DD\_UV}$ | V <sub>EE_UVLO</sub> | V <sub>EE_OV</sub>  | V <sub>EE_UV</sub> | OSC_FAIL   | V <sub>DD_UVLO</sub>  | _                 |
| STATU      |  | 0011      |      |            |              |              |                      |                     |                    |            |                       |                   |
| 0Ch        | Port 1 Status                          | RO        | 1    | Reserved   | CLS1[2]      | CLS1[1]      | CLS1[0]              | Reserved            | DET_ST1[2]         | DET_ST1[1] | DET_ST1[0]            | 0000,0000         |
| 0Dh        | Port 2 Status                          | RO        | 2    | Reserved   | CLS2[2]      | CLS2[1]      | CLS2[0]              | Reserved            | DET_ST2[2]         | DET_ST2[1] | DET_ST2[0]            | 0000,0000         |
| 0Eh        | Port 3 Status                          | RO        | 3    | Reserved   | CLS2[2]      | CLS2[1]      | CLS2[0]              | Reserved            | DET_ST3[2]         | DET_ST3[1] | DET_ST3[0]            | 0000,0000         |
|            |  | _         |      | Reserved   |              |              |                      |                     |                    |            |                       |                   |
| 0Fh<br>10h | Port 4 Status                          | RO<br>RO  | 4321 | PGOOD4     | CLS4[2]      | CLS4[1]      | CLS4[0]              | Reserved<br>PWR_EN4 | DET_ST4[2]         | DET_ST4[1] | DET_ST4[0]<br>PWR_EN1 | 0000,0000         |
| TUIT       | Power Status                           | hU        | 4321 | PGOOD4     | PGOOD3       | PGOOD2       | PGOOD1               | PWH_EIN4            | PWR_EN3            | PWR_EN2    | PWH_EINT              |                   |
| 11h        | Address Input Status                   | RO        | G    | Reserved   | Reserved     | А3           | A2                   | A1                  | A0                 | MIDSPAN    | AUTO                  | 00A3A2,<br>A1A0MA |
| CONFI      | GURATION                               |           |      |            |              |              |                      |                     |                    |            |                       |                   |
| 12h        | Operating Mode                         | R/W       | 4321 | P4_M1      | P4_M0        | P3_M1        | P3_M0                | P2_M1               | P2_M0              | P1_M1      | P1_M0                 | AAAA,AAAA         |
| 13h        | Load Disconnect<br>Detection Enable    | R/W       | 4321 | ACD_EN4    | ACD_EN3      | ACD_EN2      | ACD_EN1              | DCD_EN4             | DCD_EN3            | DCD_EN2    | DCD_EN1               | 0000,AAAA         |
| 14h        | Detection and<br>Classification Enable | R/W       | 4321 | CLASS_EN4  | CLASS_EN3    | CLASS_EN2    | CLASS_EN1            | DET_EN4             | DET_EN3            | DET_EN2    | DET_EN1               | AAAA,AAAA         |
| 15h        | Backoff and High-<br>Power Enable      | R/W       | 4321 | EN_HP_ALL  | EN_HP_CL6    | EN_HP_CL5    | EN_HP_CL4            | BCKOFF4             | BCKOFF3            | BCKOFF2    | BCKOFF1               | 0000,XXXX         |
| 16h        | Timing Configuration                   | R/W       | G    | RSTR[1]    | RSTR[0]      | TSTART[1]    | TSTART[0]            | TFAULT[1]           | TFAULT[0]          | TDISC[1]   | TDISC[0]              | 0000,0000         |
| 17h        | Miscellaneous Configuration 1          | R/W       | G    | INT_EN     | RSTR_EN      | Reserved     | Reserved             | POFF_CL             | CL_DISC            | OUT_ISO    | HP_TIME               | 1100,0000         |
| DIISHB     | UTTONS                                 | l         |      |            |              |              |                      |                     |                    |            |                       |                   |
| 18h        | Reserved                               | R/W       | G    | Reserved   | Reserved     | Reserved     | Reserved             | Reserved            | Reserved           | Reserved   | Reserved              |                   |
| 19h        | Power Enable                           | WO        | 4321 | PWR_OFF4   | PWR_OFF3     | PWR_OFF2     | PWR_OFF1             | PWR_ON4             | PWR_ON3            | PWR_ON2    | PWR_ON1               | 0000,0000         |
| 1Ah        | Global                                 | WO        | G    | CLR_INT    | Reserved     | Reserved     | RESET_IC             | RESET_P4            | RESET_P3           | RESET_P2   | RESET_P1              | 0000,0000         |
| GENER      | l .                                    | VVO       | u    | OLIT_IIVI  | Heserveu     | Heserveu     | TILOLI_IC            | TILOLI_I 4          | TILOLI_I O         | TILOLI_I Z | TILOLI_I I            | 0000,0000         |
| 1Bh        | ID                                     | RO        | G    | ID CODE[4] | ID CODE[3]   | ID_CODE[2]   | ID CODE[1]           | ID CODE[0]          | REV[2]             | REV[1]     | REV[0]                | 1100,0000         |
|            | SMODE and 2-Event                      | CoR       |      |            |              |              |                      |                     |                    |            |                       |                   |
| 1Ch        | Enable                                 | or<br>R/W | 4321 | EN4_CL6    | EN3_CL6      | EN2_CL6      | EN1_CL6              | SMODE4              | SMODE3             | SMODE2     | SMODE1                | 0000,0000         |
| 1Dh        | Reserved                               | _         | G    | Reserved   | Reserved     | Reserved     | Reserved             | Reserved            | Reserved           | Reserved   | Reserved              | _                 |
| 1Eh        | Watchdog                               | R/W       | G    | WDTIME[7]  | WDTIME[6]    | WDTIME[5]    | WDTIME[4]            | WDTIME[3]           | WDTIME[2]          | WDTIME[1]  | WDTIME[0]             | 0000,0000         |
| 1Fh        | Switch Mode                            | R/W       | 4321 | EN_WHDOG   | WD_INT_EN    | Reserved     | Reserved             | HWMODE4             | HWMODE3            | HWMODE2    | HWMODE1               | 0000,0000         |

#### **Table 35. Register Summary (continued)**

| ADDR  | REGISTER NAME                    | R/W   | PORT | BIT 7    | BIT 6    | BIT 5    | BIT 4    | BIT 3    | BIT 2    | BIT 1    | BIT 0    | RESET<br>STATE |
|-------|----------------------------------|-------|------|----------|----------|----------|----------|----------|----------|----------|----------|----------------|
| MAXIM | AXIM RESERVED                    |       |      |          |          |          |          |          |          |          |          |                |
| 20h   | Reserved                         | _     | G    | Reserved | _              |
| 21h   | Reserved                         | -     | G    | Reserved | _              |
| 22h   | Reserved                         | I     | G    | Reserved | _              |
| 23h   | Program                          | R/W   | 4321 | Reserved | Reserved | CLC_EN   | DET_BY   | OSCF_RS  | AC_TH[2] | AC_TH[1] | AC_TH[0] | _              |
| 24h   | High-Power Mode                  | R/W   | G    | Reserved | HP[2]    | HP[1]    | HP[0]    | Reserved | Reserved | Reserved | Reserved | 0000,0000      |
| 25h   | Reserved                         | ı     | G    | Reserved | 0000,0000      |
| 26h   | Reserved                         | ı     | G    | Reserved | 0000,0000      |
| 27h   | Reserved                         | ı     | G    | Reserved | _              |
| 28h   | Reserved                         | -     | G    | Reserved | _              |
| 29h   | Miscellaneous<br>Configuration 2 | R/W   | 1234 | Reserved | Reserved | Reserved | Reserved | Reserved | LSC_EN   | IVEE[1]  | IVEE[0]  | 0000,0000      |
| 2Ah   | ICUT Registers 1 and 2           | R/W   | 21   | Reserved | ICUT2[2] | ICUT2[1] | ICUT2[0] | Reserved | ICUT1[2] | ICUT1[1] | ICUT1[0] | 0000,0000      |
| 2Bh   | ICUT Registers 3 and 4           | R/W   | 43   | Reserved | ICUT4[2] | ICUT4[1] | ICUT4[0] | Reserved | ICUT3[2] | ICUT3[1] | ICUT3[0] | 0000,0000      |
| CLASS | IFICATION STATUS RE              | GISTE | RS   |          |          |          |          |          |          |          |          |                |
| 2Ch   | Port 1 Class                     | RO    | 1    | Reserved | Reserved | CLS1[5]  | CLS1[4]  | CLS1[3]  | CLS1[2]  | CLS1[1]  | CLS1[0]  | 0000,0000      |
| 2Dh   | Port 2 Class                     | RO    | 2    | Reserved | Reserved | CLS2[5]  | CLS2[4]  | CLS2[3]  | CLS2[2]  | CLS2[1]  | CLS2[0]  | 0000,0000      |
| 2Eh   | Port 3 Class                     | RO    | 3    | Reserved | Reserved | CLS3[5]  | CLS3[4]  | CLS3[3]  | CLS3[2]  | CLS3[1]  | CLS3[0]  | 0000,0000      |
| 2Fh   | Port 4 Class                     | RO    | 4    | Reserved | Reserved | CLS4[5]  | CLS4[4]  | CLS4[3]  | CLS4[2]  | CLS4[1]  | CLS4[0]  | 0000,0000      |
| CURRE | NT REGISTER                      |       |      |          |          |          |          |          |          |          |          |                |
| 30h   | Current Port 1 (MSB)             | RO    | 1    | IPD1[8]  | IPD1[7]  | IPD1[6]  | IPD1[5]  | IPD1[4]  | IPD1[3]  | IPD1[2]  | IPD1[1]  | 0000,0000      |
| 31h   | Current Port 1 (LSB)             | RO    | 1    | Reserved | IPD1[0]  | 0000,0000      |
| 32h   | Current Port 2 (MSB)             | RO    | 2    | IPD2[8]  | IPD2[7]  | IPD2[6]  | IPD2[5]  | IPD2[4]  | IPD2[3]  | IPD2[2]  | IPD2[1]  | 0000,0000      |
| 33h   | Current Port 2 (LSB)             | RO    | 2    | Reserved | IPD2[0]  | 0000,0000      |
| 34h   | Current Port 3 (MSB)             | RO    | 3    | IPD3[8]  | IPD3[7]  | IPD3[6]  | IPD3[5]  | IPD3[4]  | IPD3[3]  | IPD3[2]  | IPD3[1]  | 0000,0000      |
| 35h   | Current Port 3 (LSB)             | RO    | 3    | Reserved | IPD3[0]  | 0000,0000      |
| 36h   | Current Port 4 (MSB)             | RO    | 4    | IPD4[8]  | IPD4[7]  | IPD4[6]  | IPD4[5]  | IPD4[4]  | IPD4[3]  | IPD4[2]  | IPD4[1]  | 0000,0000      |
| 37h   | Current Port 4 (LSB)             | RO    | 4    | Reserved | IPD4[0]  | 0000,0000      |

<sup>\*</sup>UV and UVLO bits of VEE and VDD asserted depends on the order VEE and VDD supplies are brought up.

M = MIDSPAN state before reset.

A3...0 = ADDRESS input states before reset.

46 \_\_\_\_\_\_\_**/V**|/X|/**V**|

A = AUTO pin state before reset.

#### **Applications Information**

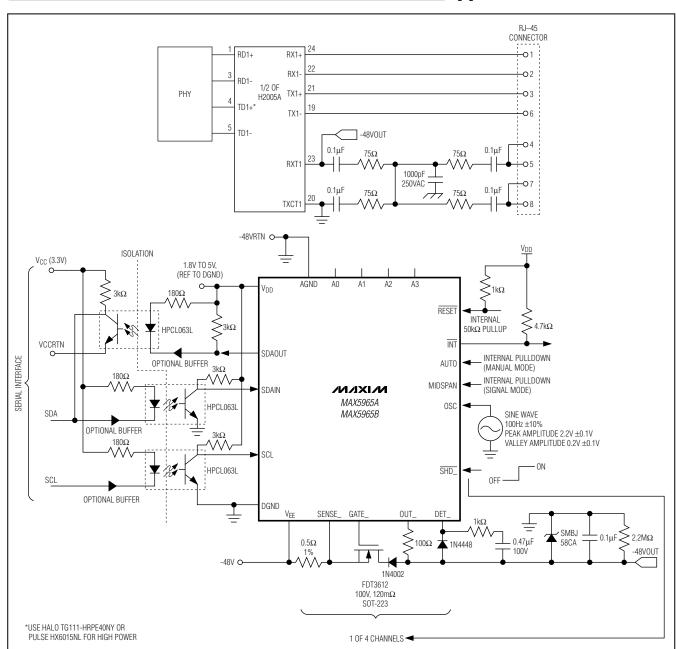


Figure 13. PoE System Diagram with LAN Transformer

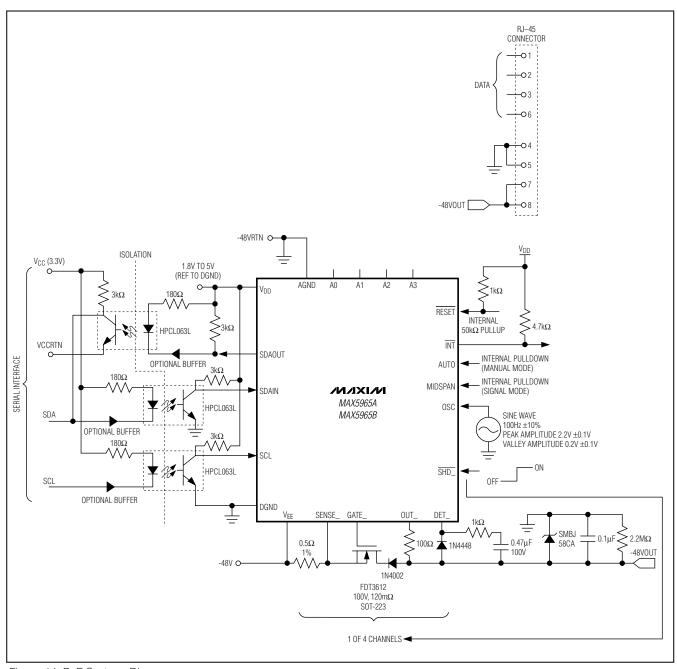


Figure 14. PoE System Diagram

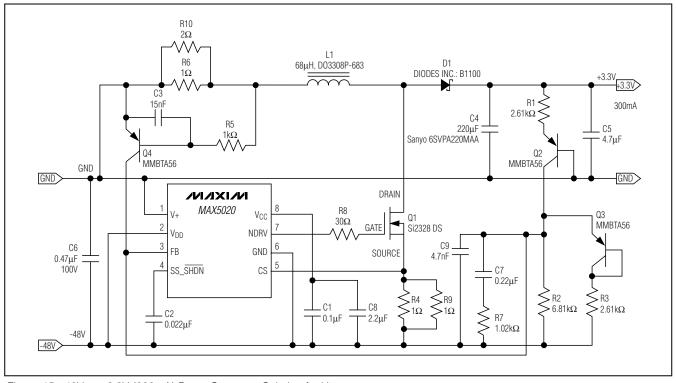


Figure 15. -48V to +3.3V (300mA) Boost Converter Solution for VDIG

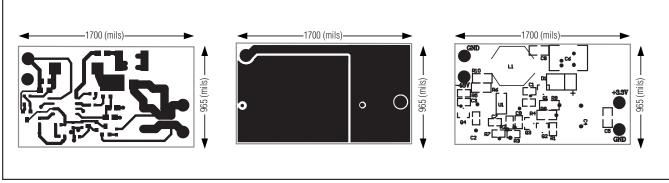


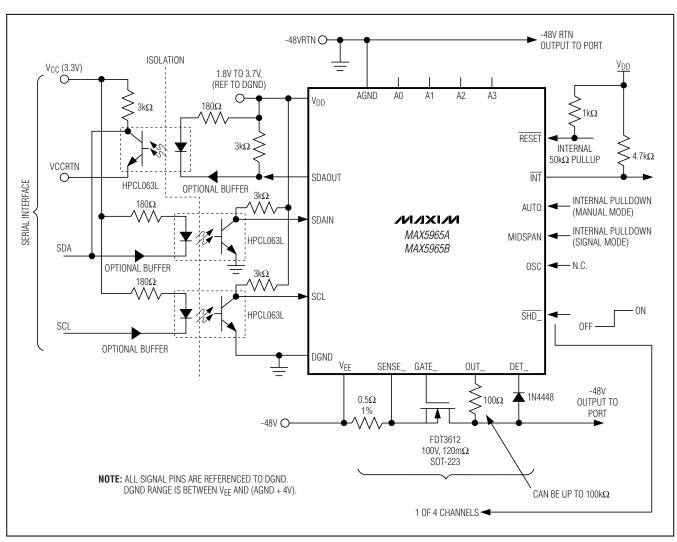
Figure 16. Layout Example for Boost Converter Solution for VDIG

#### Component List for VDIG Supply

| DESIGNATION | DESCRIPTION  |
|-------------|--|
| C1          | 0.1µF, 25V ceramic capacitor                         |
| C2          | 0.022µF, 25V ceramic capacitor                       |
| C3          | 15nF, 25V ceramic capacitor                          |
| C4          | 220µF capacitor Sanyo 6SVPA220MAA                    |
| C5          | 4.7μF, 16V ceramic capacitor                         |
| C6          | 0.47µF, 100V ceramic capacitor                       |
| C7          | 0.22µF, 16V ceramic capacitor                        |
| C8          | 2.2µF, 16V ceramic capacitor                         |
| C9          | 4.7nF, 16V ceramic capacitor                         |
| D1          | B1100 100V Schottky diode                            |
| L1          | 68µH inductor<br>Coilcraft DO3308P-683 or equivalent |

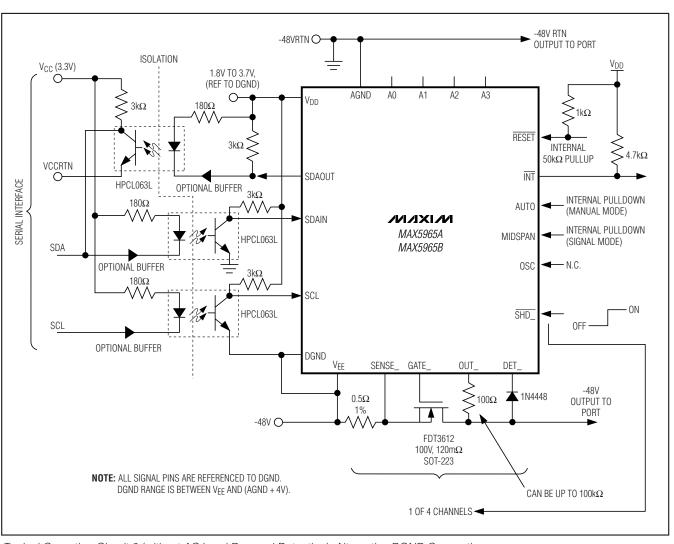
| DESIGNATION | DESCRIPTION                                  |
|-------------|--|
| Q1          | Si2328DS<br>Vishay n-channel MOSFET, SOT23   |
| Q2, Q3, Q4  | MMBTA56 small-signal PNP                     |
| R1, R3      | 2.61kΩ ±1% resistors                         |
| R2          | 6.81kΩ ±1% resistor                          |
| R4, R6, R9  | 1Ω ±1% resistors                             |
| R5          | 1kΩ ±1% resistor                             |
| R7          | 1.02kΩ ±1% resistor                          |
| R8          | 30Ω ±1% resistor                             |
| R10         | 2Ω ±1% resistor                              |
| U1          | High-voltage PWM IC<br>MAX5020ESA (8-pin SO) |

#### **Typical Operating Circuits**



Typical Operating Circuit 1 (without AC Load Removal Detection)

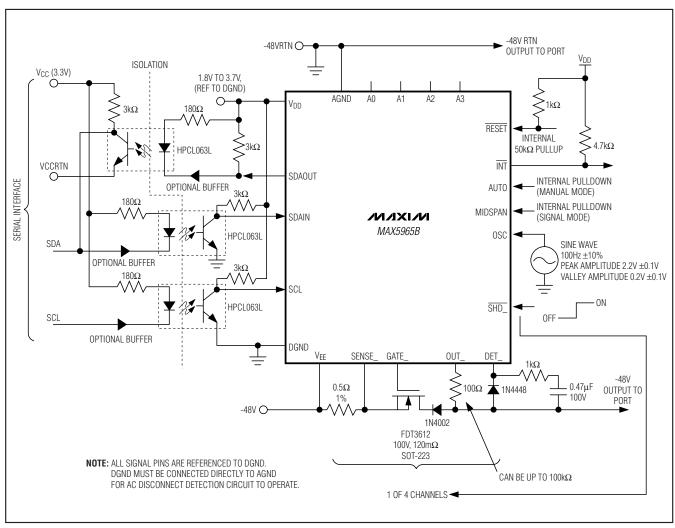
#### Typical Operating Circuits (continued)



Typical Operating Circuit 2 (without AC Load Removal Detection); Alternative DGND Connection

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#### Typical Operating Circuits (continued)



Typical Operating Circuit 3 (with AC Load Removal Detection)

#### Chip Information

#### \_Package Information

For the latest package outline information and land patterns (footprints), go to <a href="https://www.maxim-ic.com/packages">www.maxim-ic.com/packages</a>. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

| PACKAGE<br>TYPE | PACKAGE<br>CODE | OUTLINE NO.    | LAND<br>PATTERN NO. |
|-----------------|-----------------|----------------|---------------------|
| 36 SSOP         | A36+4           | <u>21-0040</u> | <u>90-0096</u>      |

PROCESS: BICMOS

#### **Revision History**

| REVISION<br>NUMBER | REVISION DATE | DESCRIPTION   | PAGES<br>CHANGED                  |
|--------------------|---------------|---|-----------------------------------|
| 0                  | 7/09          | Initial release   |                                   |
| 1                  | 1/10          | Revised Features, Register Map and Description section, and Tables 32 and 37.   | 1, 37, 41, 45                     |
| 2                  | 5/11          | Removed "pre-" from IEEE standard, updated <i>Typical Operating Characteristics</i> , and text throughout the data sheet. | 1, 8–12, 15, 18, 22,<br>31, 40–47 |
| 3                  | 3/12          | Corrected power mode formula.   | 44                                |

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