Datasheet

For Electric Cars & Hybrid Cars

Isolation Voltage 2,500Vrms High Voltage Detection IC

BM67290FV-C

General Description

This is a voltage detector IC for DC-DC converter. Aside from being capable of converting input voltage to duty, it has built in protection functions against low voltage, overvoltage and active overvoltage.

Key Specifications

- Isolation Voltage: 2,500Vrms (Max)
- Power Source Voltage Range (high voltage side): 8.0V to 24V
- Power Source Voltage Range (low voltage side): 3.0V to 5.5V
- Reference Voltage : 5V±1.5%
- Oscillation Frequency Variability: 10kHz to 250kHz (Typ)

Features

- Built-in input PWM modulation circuit
- Built-in low voltage lock out circuit
- Built-in input under voltage protection function
- Built-in input overvoltage protection function
- Built-in magnetic isolator
- Built-in active overvoltage protection function
- Built-in reference voltage output

Package

(Typ) (Typ) (Max)
6.50mm x 8.10mm x 2.01mm

SSOP-B20W

Application

- DC-DC converter

Typical Application Circuit

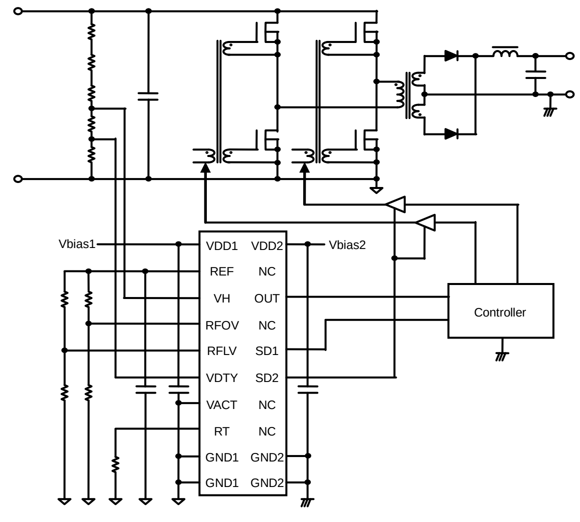


Figure 1. Example of a Typical Application Circuit of DC-DC Converter

○Product structure: Silicon integrated circuit ○This product has no designed protection against radioactive rays

Pin Configuration

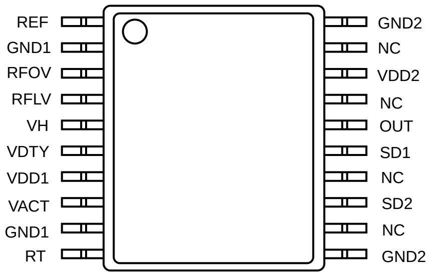
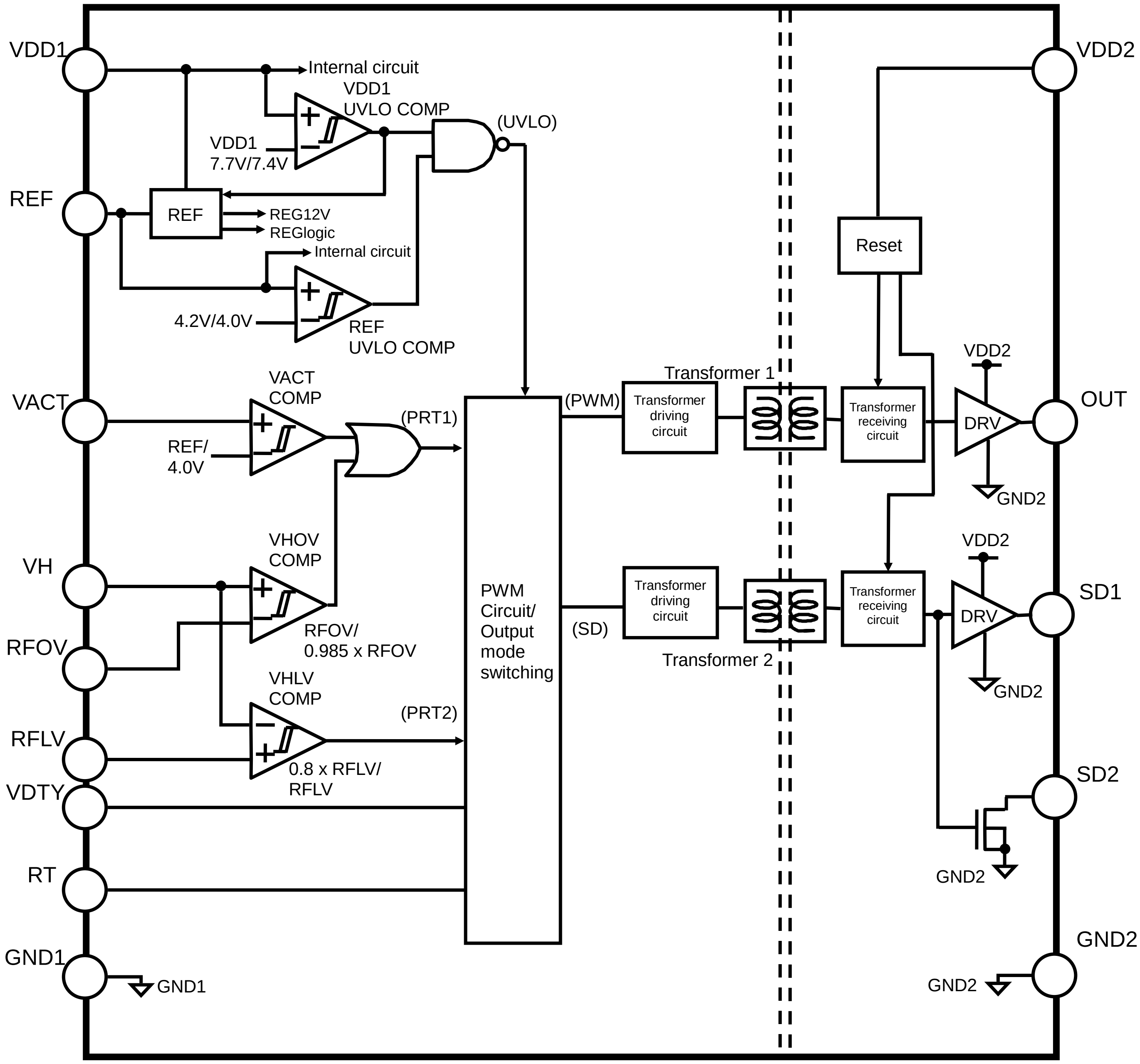


Figure 2. BM67290FV-C Package (SSOP-B20W)

Pin Descriptions

Terminal Number	Code	I/O	Function
1	REF	O	Reference voltage terminal
2	GND1	-	Grounding terminal 1 (high voltage side)
3	RFOV	I	Input overvoltage protection value setting terminal
4	RFLV	I	Input low voltage protection value setting terminal
5	VH	I	Input voltage signal terminal
6	VDTY	I	Input voltage signal terminal for Duty
7	VDD1	-	Power source terminal 1 (high voltage side)
8	VACT	I	Active voltage signal terminal
9	GND1	-	Grounding terminal 1 (high voltage side)
10	RT	I	Timing resistance terminal
11	GND2	-	Grounding terminal 2 (low voltage side)
12	NC	-	Disconnected terminal
13	SD2	O	Protective cutoff terminal 2
14	NC	-	Disconnected terminal
15	SD1	O	Protective cutoff terminal 1
16	OUT	O	Input voltage monitoring condition output signal terminal
17	NC	-	Disconnected terminal
18	VDD2	-	Power source terminal 2 (low voltage side)
19	NC	-	Disconnected terminal
20	GND2	-	Grounding terminal 2 (low voltage side)

Block Diagram



Explanation of Operation

(1) Timing when VDD2 is ON first before VDD1

VDD2 powers SD1, SD2 and OUT. When VDD2 turns ON, SD1=H, SD2=L and OUT=L initially.
Then, when VDD1 turns ON and reaches VthVDD1H, REF turns ON. When REF reaches VthREF, CT turns ON.
Once the above conditions are satisfied, DUTY will be outputted to OUT pin at CLK’s 2nd pulse. At the same time, SD1 becomes L and SD2 becomes Hi-Z.

Figure 3. VDD2 Start to VDD1 Start Timing Chart

(2) Timing when VDD1 is ON first before VDD2

When VDD1 turns ON and reaches VthVDD1, REF turns ON. When REF reaches VthREF, CT turns ON.
When VDD2 turns ON, SD1=H, SD2=L and OUT=L initially..
When VDD2 reaches VthVDD2, DUTY will be immediately outputted to OUT pin at the next CLK pulse.
SD1 and SD2 behavior at CLK's 2nd pulse is still the same with (1), SD1=L and SD2=Hi-Z at CLK's 2nd pulse.

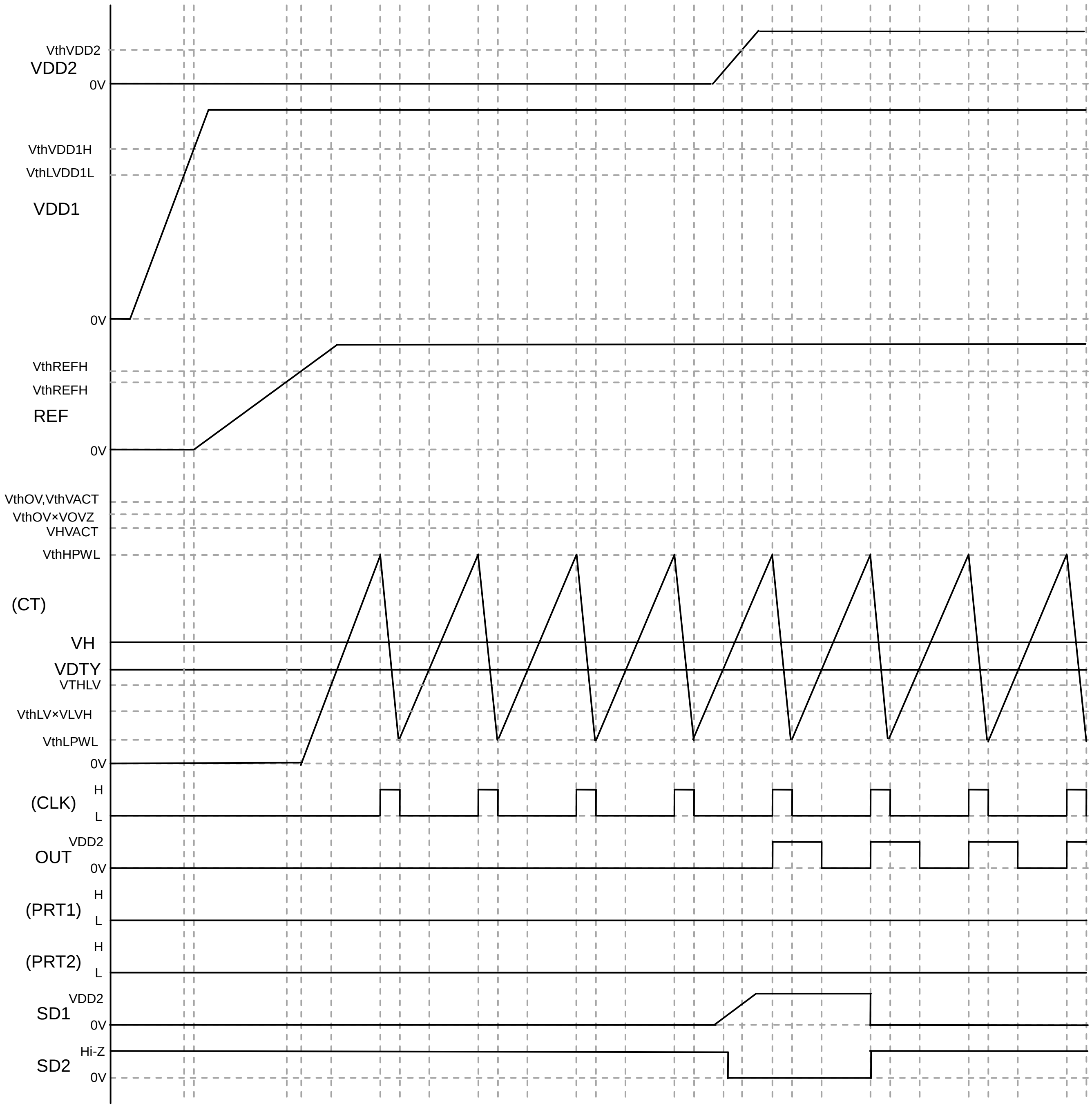


Figure 4. VDD1 Start to VDD2 Start Timing Chart

(3) Timing when VDD1 is turned OFF before VDD2

When VDD1 reaches VthLVDD1, REF and CT immediately stop. Outputs become SD1=H, SD2=L and OUT=L.

Figure 5. VDD1 Stop to VDD2 Stop Timing Chart

(4) Timing when VDD2 is tuned OFF before VDD1

When VDD2 reaches VthLVDD2, the outputs become SD1=H, SD2=L and OUT=L even if REF and CT are still active.

Figure 6. VDD2 Stop to VDD1 Stop Timing Chart

(5) Normal Operation

During normal operation, the internal oscillator (CT) and internal clock (CLK) are active.
OUT turns L every time CT is above VDTY.
OUT turns H every time CLK rises.
Since protection circuits are not active, SD1=L and SD2=Hi-Z.

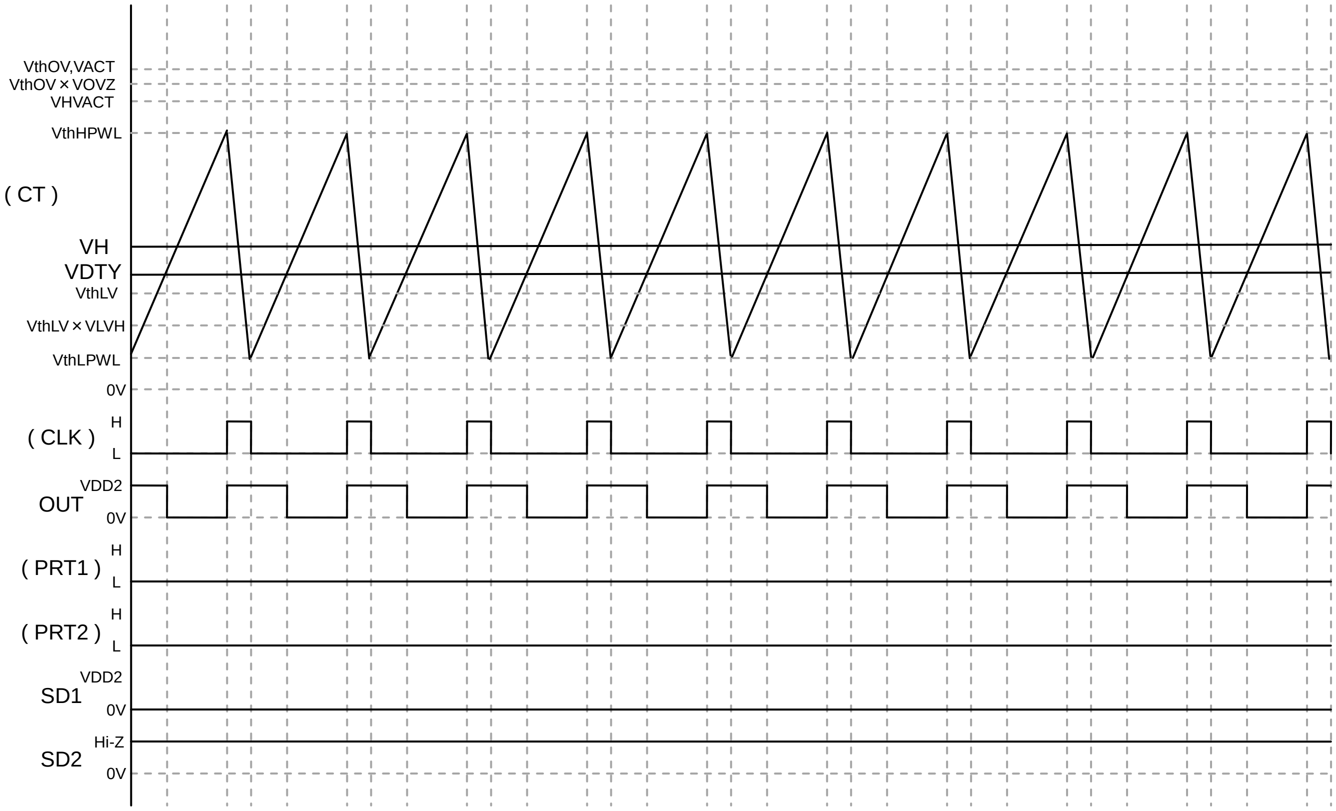


Figure 7. Normal Operation Timing Chart

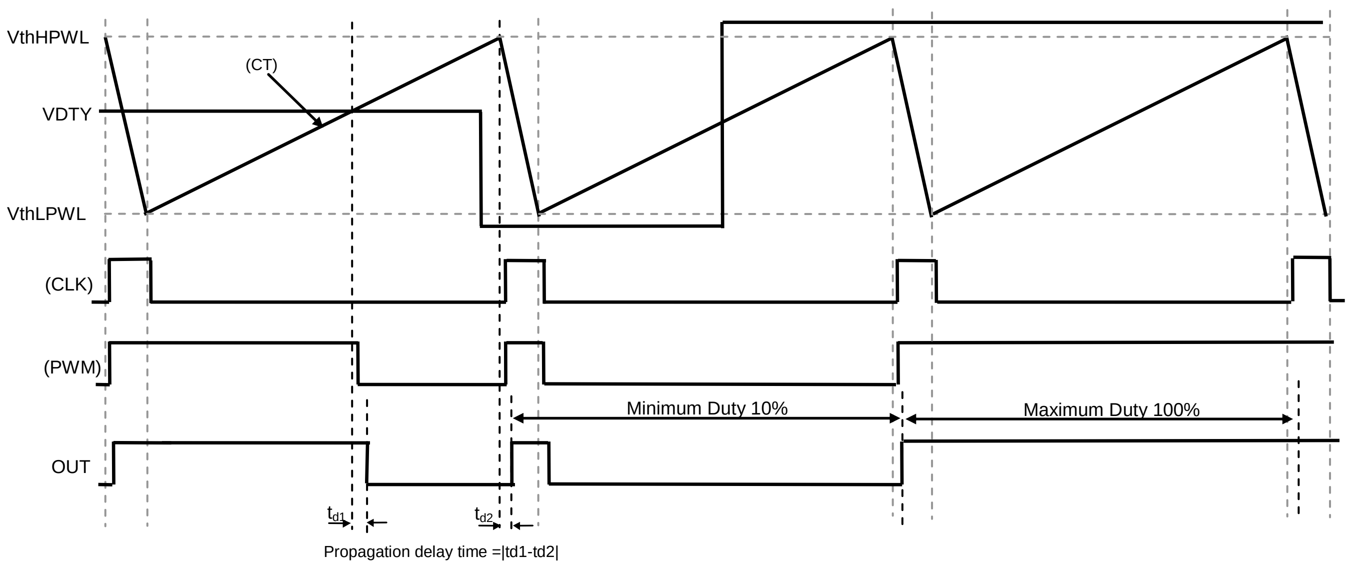


Figure 8. Propagation Delay Time, Minimum Duty, Maximum Duty

The output from OUT terminal varies its Duty in accordance with VDTY voltage. Duty becomes higher as VDTY voltage increases. The relationship between VDTY voltage and output Duty is shown in the graph below. The output Duty becomes 100% when VDTY voltage is above VthHPWL (Typ 4.275V) and minimum duty is achieved when VDTY voltage is below VthLPWL (Typ 0.225 V).

Duty= Min duty + (VDTY-0.225V)/A
frequency =10kHz : Min duty=10.0%, A=0.04500
frequency =100kHz : Min duty=10.9%, A=0.04545
frequency =250kHz : Min duty=12.1%, A=0.04607

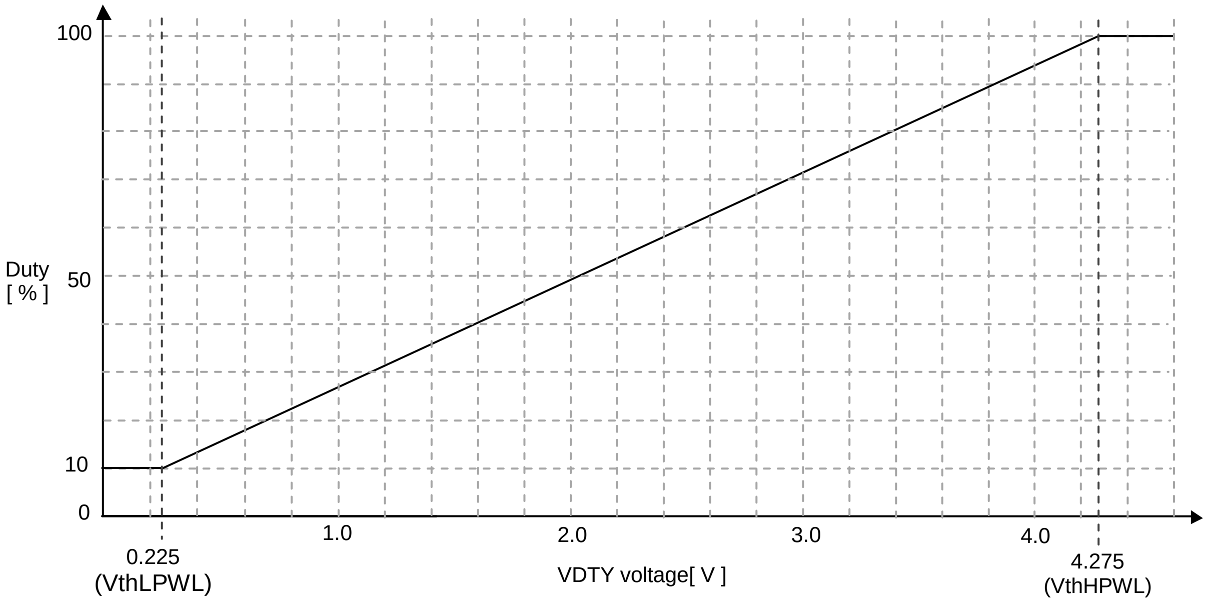


Figure 9. VDTY Voltage-Output Duty Property

(6) Overvoltage Detection (active overvoltage protection, input overvoltage protection)

Overvoltage is detected when VACT > VthACT (for active overvoltage protection) and VH>VthOV (for input overvoltage protection). PRT1 immediately turns to "H" and the protection circuit is activated.
At this time, OUT=H, SD1=H, and SD2=L.
When the protection circuit is deactivated (VACT<VHVACT for active OVP and VH <VthOV×VOVZ for input OVP), OUT returns to normal operation, SD1=L and SD2=Hi-Z at CLK's 2nd pulse..

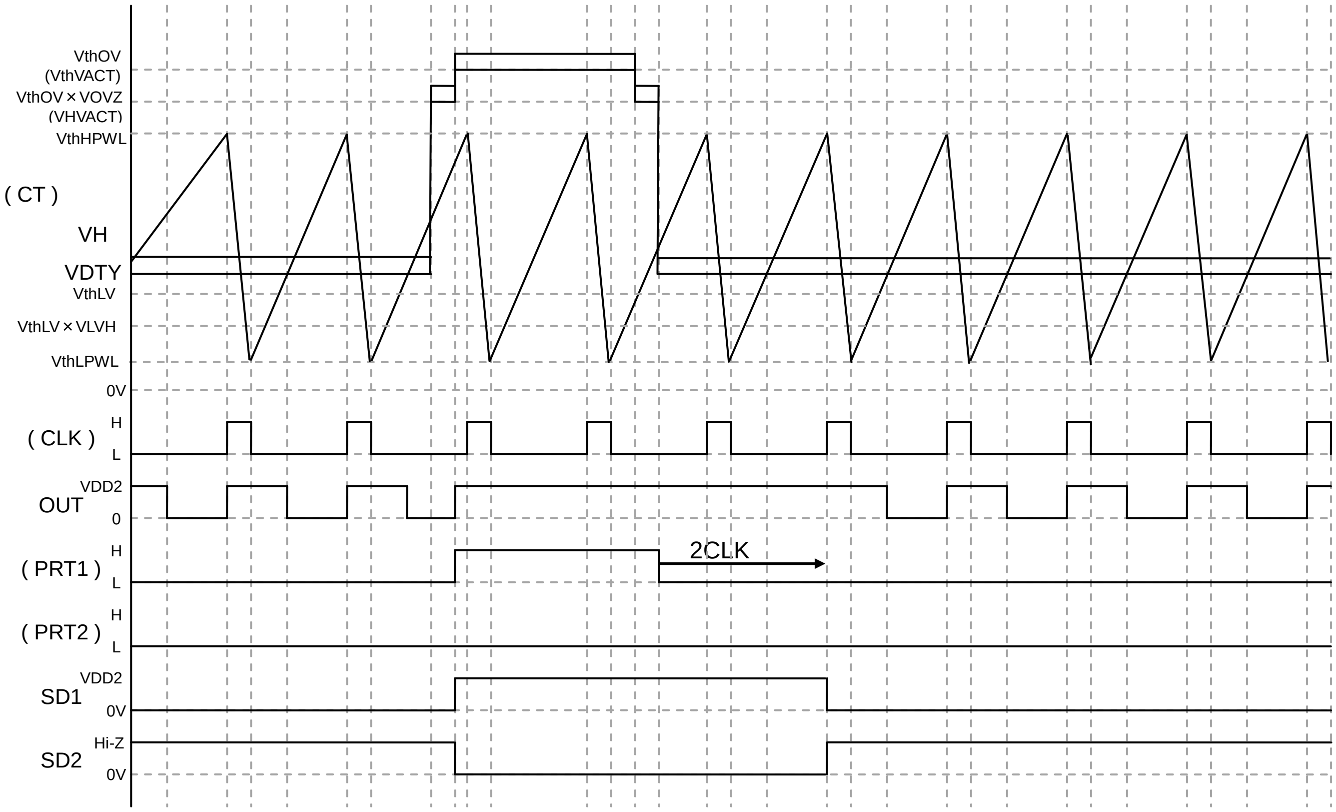


Figure 10. Protection Detection (active overvoltage protection, input overvoltage protection) Timing Chart

(7) Under Voltage Detection (input low voltage protection)

When VH < VthLV×VLVH, input low voltage protection is activated. PRT2 immediately turns H.
At this time, OUT="L", SD1="H", and SD2="L".
When VH > VthLV, the protection circuit is deactivated and PRT2=L. OUT returns to normal operation, SD1 turns L and SD2 turns Hi-Z at CLK's 2nd pulse.

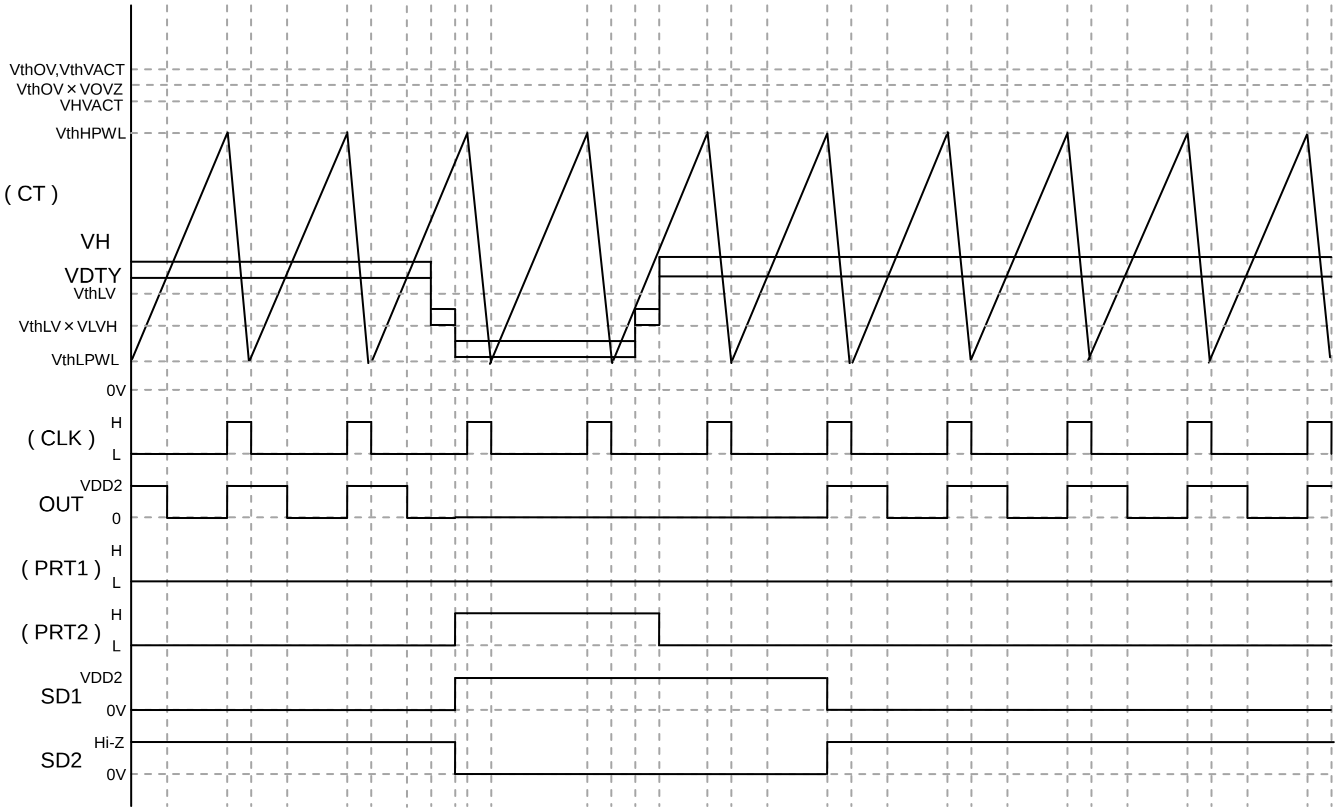


Figure 11. Protection Detection (input low voltage protection) Timing Chart

(8) UVLO Detection

This IC is equipped with UVLO circuits for VDD1 voltage, REF voltage and VDD2 voltage.
When any undervoltage is detected, OUT=L, SD1=H and SD2=L.

No	VDD1 UVLO	VDD2 UVLO	REF UVLO	OUT	SD1	SD2
1	L	L	L	L	H	L
2	L	L	H	L	H	L
3	L	H	L	L	H	L
4	L	H	H	L	H	L
5	H	L	L	L	H	L
6	H	L	H	L	H	L
7	H	H	L	L	H	L
8	H	H	H	DUTY OUTPUT	PROTECTION OUTPUT	PROTECTION OUTUT

H:Release L:Detection

Figure 12. Output Logic of the UVLO

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Power Source Terminal (VDD1)	V_{DD1}	-0.3 to +30 (Note 1)	V
Power Source Terminal (VDD2)	V_{DD2}	-0.3 to +7 (Note 2)	V
Input Voltage (VH)	V_{H}	-0.3 to VDD1+0.3 or +30 (Note 1)	V
Input Voltage (VDTY)	V_{DTY}	-0.3 to VDD1+0.3 or +30 (Note 1)	V
Input Voltage (VACT)	V_{ACT}	-0.3 to VDD1+0.3 or +30 (Note 1)	V
Input Voltage (RFOV)	V_{RFOV}	-0.3 to VDD1+0.3 or +30 (Note 1)	V
Input Voltage (RFLV)	V_{RFLV}	-0.3 to VDD1+0.3 or +30 (Note 1)	V
Output Voltage (OUT)	V_{OUT}	-0.3 to VDD2+0.3 or +7 (Note 2)	V
Output Voltage (SD1)	V_{SD1}	-0.3 to VDD2+0.3 or +7 (Note 2)	V
Output Voltage (SD2)	V_{SD2}	-0.3 to +20 (Note 2)	V
Operating Temperature Range	Topr	-40 to +125	°C
Storage Temperature Range	Tstg	-55 to+150	°C
Junction Temperature	Tjmax	150	°C

(Note 1) Based on GND1
(Note 2) Based on GND2

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Thermal Resistance(Note3)

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s(Note 5)	2s2p(Note 6)	
Fill the package name				
Junction to Ambient	θ_{JA}	151.5	80.6	°C/W
Junction to Top Characterization Parameter(Note 4)	Ψ_{JT}	47	40	°C/W

*(Note3)*Based on JESD51-2A(Still-Air)
*(Note4)*The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
*(Note5)*Using a PCB board based on JESD51-3.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3mm x 76.2mm x 1.57mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70μm

*(Note 6)*Using a PCB board based on JESD51-7.

Layer Number of Measurement Board	Material	Board Size
4 Layers	FR-4	114.3mm x 76.2mm x 1.6mmt

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70μm	74.2mm x 74.2mm	35μm	74.2mm x 74.2mm	70μm

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Power Source Voltage VDD1	V_{DD1}	8.0	10	24	V
Power Source Voltage VDD2	V_{DD2}	3.0	5	5.5	V
Reference Voltage Output Current	I_{REF}	0	-	5 (Note 7)	mA
Reference Voltage Output Capacity	C_{REF}	1.0	-	4.7	μF
Timing Resistance	R_{RT}	4	10	100	kΩ
Oscillation Frequency	f_{OSC}	10	100	250	kHz
In-phase Input Voltage Range VDD1<11.5V	V_{ICML}	0	-	V_{DD1}-2.5	V
In-phase Input Voltage Range VDD1≥ 11.5V	V_{ICMH}	0	-	9.0	V
Input Protection Diode Current	I_{DIO}	-	-	2.0	mA

(Note 7) Should not exceed Tj=150℃.

Insulation Related Characteristics (UL1577 conformity)

Parameter	Symbol	Characteristic	Unit
Insulation Resistance (V_{IO}=500V)	R_S	$>10^9$	Ω
Insulation Withstand Voltage / 1min.	V_{ISO}	2500	Vrms
Insulation Test Voltage / 1s	V_{ISO}	3000	Vrms

Electrical Characteristics

(Unless, otherwise specified, V_{DD1}=8V to 24.0V, V_{DD2}=3.0V to 5.5V, Ta=-40°C to +125°C, R_T=10kΩ, described with direction of flow from IC as +)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
[Whole]						
Input Voltage Range	V_{DD1}	8.0	-	24.0	V	
	V_{DD2}	3.0	-	5.5	V	
VDD1 Circuit Current	I_{DD1}	-	4.6	10.0	mA	RT=10kΩ , V_{DTY}=2.25V
VDD2 Circuit Current	I_{DD2}	-	0.2	1.0	mA	RT=10kΩ , V_{DTY}=2.25V
[Low Voltage Malfunction Prevention Circuit]						
Startup Threshold Voltage	$V_{thVDD1H}$	7.5	7.7	7.9	V	
Cutoff Threshold Voltage	$V_{thVDD1L}$	7.2	7.4	7.6	V	
Operation Voltage Hysteresis	$V_{hysVDD1}$	0.2	0.3	0.4	V	
Startup Threshold Voltage	V_{thREFH}	4.0	4.2	4.4	V	
Cutoff Threshold Voltage	V_{thREFL}	3.8	4.0	4.2	V	
Operation Voltage Hysteresis	V_{hysREF}	0.1	0.2	0.3	V	
[Reference Voltage]						
Output Voltage	V_{REF}	4.925	5.000	5.075	V	IREF=0mA to 5mA
Output Drive Current	I_{ref}	5	-	-	mA	
[PWM Part]						
Oscillation Frequency	f_{OSC}	90	100	110	kHz	RT=10kΩ
Duty Precision 10kHz	DutyL	52.0	55.0	58.0	%	VDTY=2.25V, H duty
Duty Precision 100kHz	DutyM	52.5	55.5	58.5	%	VDTY=2.25V, H duty
Duty Precision 250kHz	DutyH	53.0	56.0	59.0	%	VDTY=2.25V, H duty
Duty Temperature Property/Electric Property Variation Ratio (Comparison with Ta=25℃, VDD1=10V)	ΔDuty	-	1	-	%	Design assurance
Threshold Voltage During Discharge	V_{thHPWL}	4.1	4.275	4.45	V	
Threshold Voltage During Charge	V_{thLPWL}	0.15	0.225	0.3	V	
Input Bias Current	I_{bVDTY}	-1.0	-	1.0	μA	VDTY=0V to 9V
Propagation Delay Time 1	t_{d1}	-	-	500	ns	
Propagation Delay Time 2	t_{d2}	-	-	500	ns	
Propagation Delay Time Difference	t_{d1}-t_{d2}	-	-	50	ns	
[OUT Terminal]						
Output Voltage	V_{OUTL}	-	-	0.5	V	I_{SINK} = -20mA
	V_{OUTH}	V_{DD2}-0.5	-	V_{DD2}	V	I_{SOURCE} = 20mA

Electrical Characteristics – continued

(Unless, otherwise specified, V_{DD1}=8V to 24.0V, V_{DD2}=3.0V to 5.5V, Ta=-40°C to +125°C, R_T=10kΩ, described with direction of flow from IC as +)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
[SD1 Terminal]						
Output Voltage	V_{SD1L}	-	-	0.5	V	I_{SINK} = -20mA
	V_{SD1H}	V_{DD2}-0.5	-	V_{DD2}	V	I_{SOURCE} = 20mA
[SD2 Terminal]						
SD2 Voltage Operation	V_{SD2}	-	-	0.5	V	I_{SOURCE} = 20mA
Output Off-leak Current	$I_{OFFLEAKSD2}$	-	-	10	μA	SD2 = 20V
[Input Low Voltage Protection Part]						
Protection Operation/ Protection Cancellation Voltage Ratio	V_{LVH}	0.78	0.80	0.82	-	RFLV=1.2V, VH=1.5V to down
Protection Cancellation Threshold Voltage	V_{thLV}	1.15	1.20	1.25	V	RFLV=1.2V, V_H=0V to up
Protection Operation Delay Time	t_{dlyLV}	-	-	1.0	μs	RFLV=1.2V, VH=1.5V to 0.5V to SD1:L to H, SD2 : H to L
RFLV Input Bias Current	I_{bRFLV}	-1.0	-	1.0	μA	VH= RFLV=0V to 9V
VH Input Bias Current	I_{bVH}	-1.0	-	1.0	μA	VH= RFLV=0V to 9V
[Active Overvoltage Protection Part]						
Overvoltage Threshold Voltage	V_{thVACT}	4.9	5.0	5.1	V	VACT=3.5V to up
Protection Cancellation Threshold Voltage	V_{HVACT}	3.9	4.0	4.1	V	VACT=5.5V to down
Protection Operation Delay Time	$t_{dlyVACT}$	-	-	1.0	μs	VACT=4.5V to 5.5V to SD1：L to H, SD2：H to L
VACT Input Bias Current	I_{bVACT}	-1.0	-	1.0	μA	VACT=0V to 9V
[Input Overvoltage Protection Part]						
Protection Operation/ Protection Cancellation Voltage Ratio	V_{OVZ}	0.970	0.985	1.000	-	RFOV=5.0V, V_H=5.5V to down
Protection Operation Threshold Voltage	V_{thOV}	4.9	5.0	5.1	V	RFOV=5.0V,V_H=0V to up
Protection Operation Delay Time	t_{dlyOV}	-	-	1.0	μs	RFOV=5.0V, VH=4.5V to 5.5V to SD1 : L to H, SD2 : H to L
RLOV Input Bias Current	I_{bRFOV}	-1.0	-	1.0	μA	VH= RFOV=0V to 9V

Typical Performance Curves

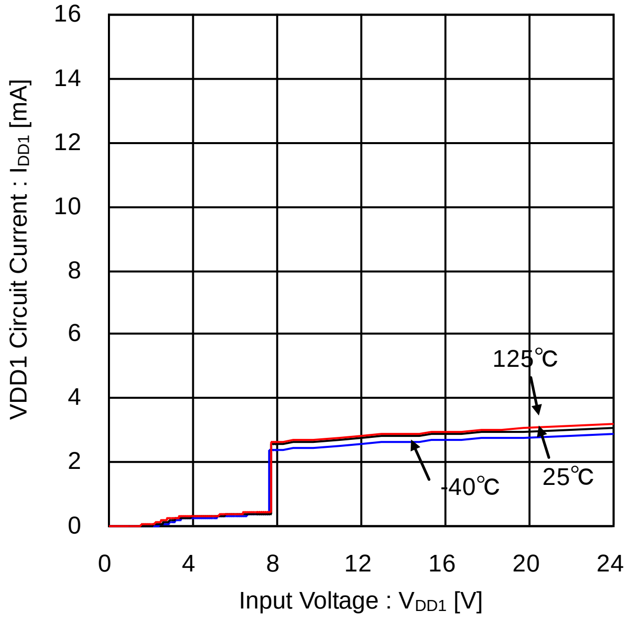


Figure 13. VDD1 Circuit Current 10kHz vs Input Voltage

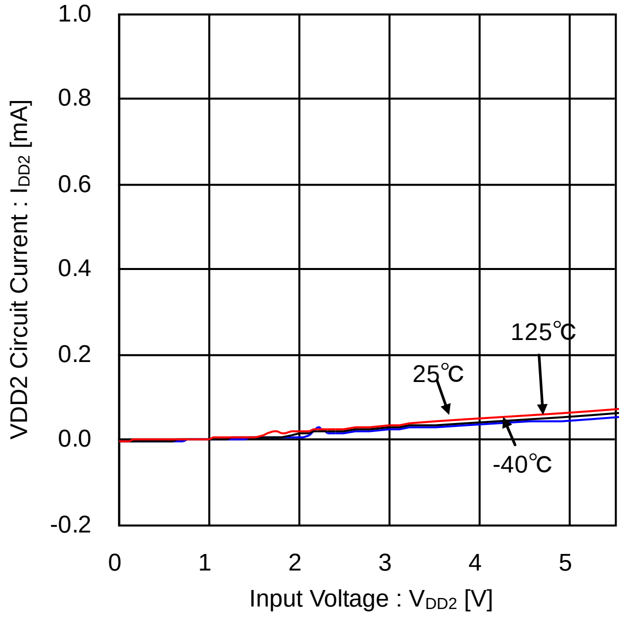


Figure 14. VDD2 Circuit Current 10kHz vs Input Voltage

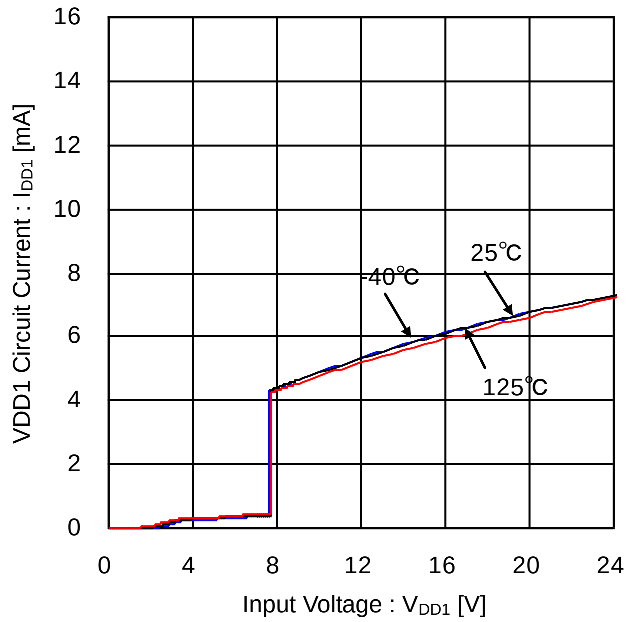


Figure 15. VDD1 Circuit Current 100kHz vs Input Voltage

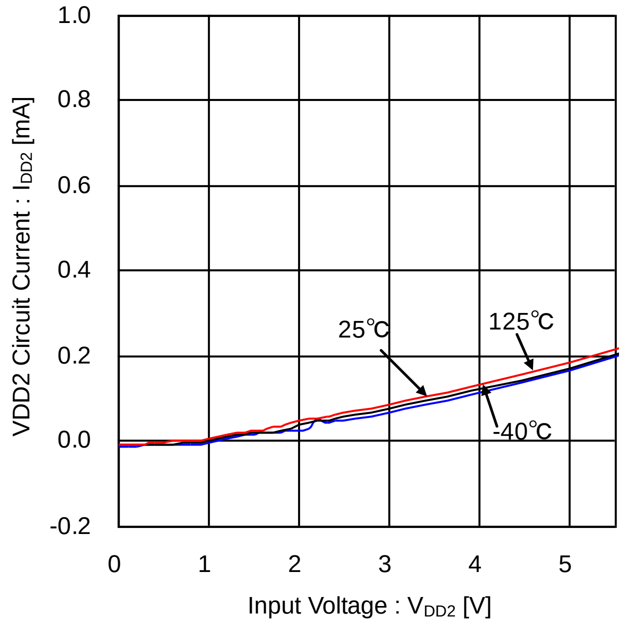


Figure 16. VDD2 Circuit Current 100kHz vs Input Voltage

Typical Performance Curves - continued

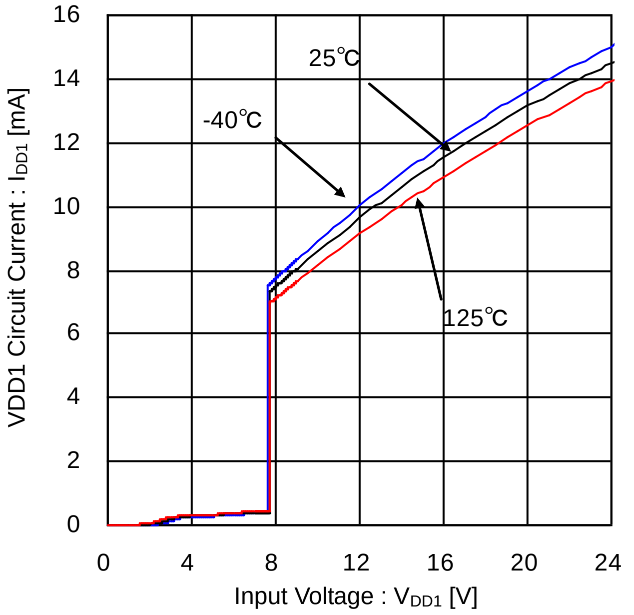


Figure 17. VDD1 Circuit Current 250kHz
vs Input Voltage

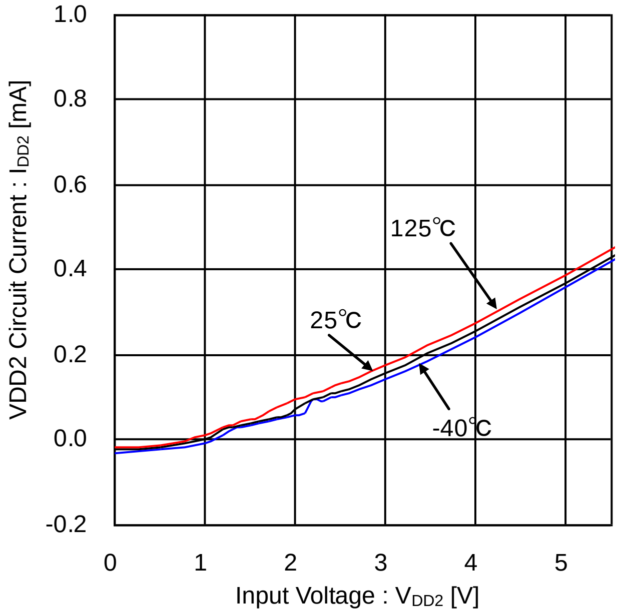


Figure 18. VDD2 Circuit Current 250kHz
vs Input Voltage

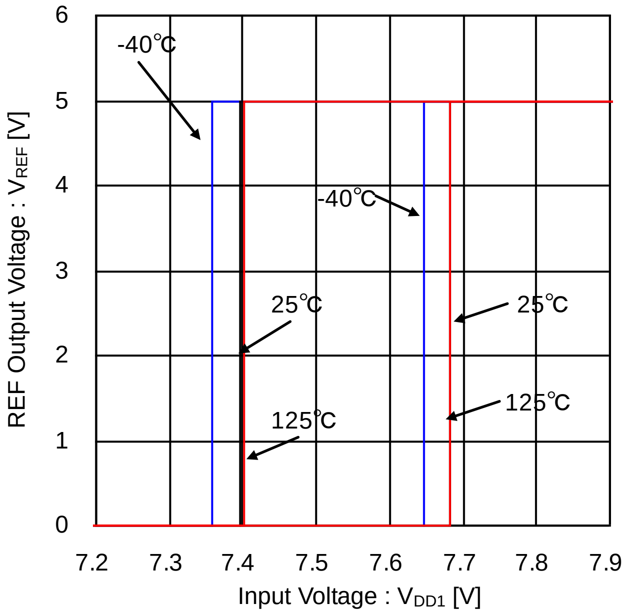


Figure 19. REF Output Voltage vs Input Voltage
(VDD1 Startup/Shutdown Threshold)

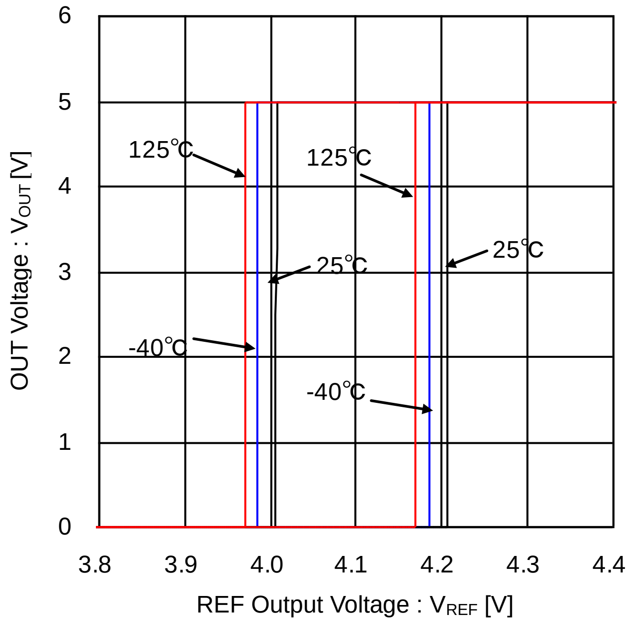


Figure 20. OUT Voltage vs REF Output Voltage
(REF Startup/Shutdown Threshold)

Typical Performance Curves - continued

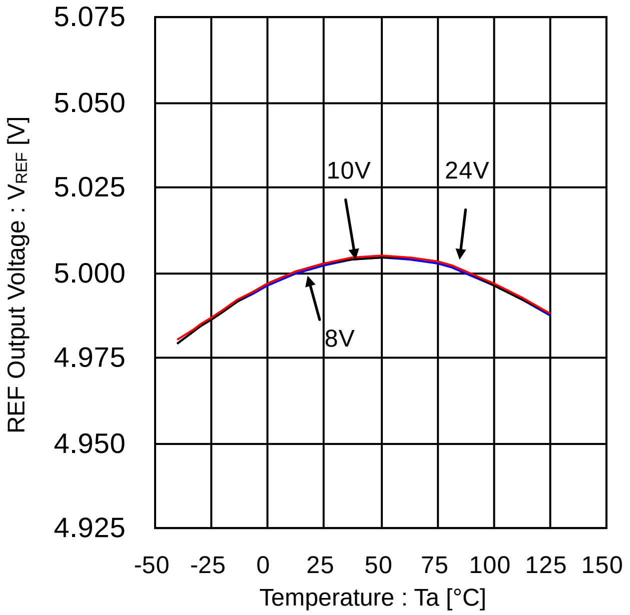


Figure 21. REF Output Voltage vs Temperature

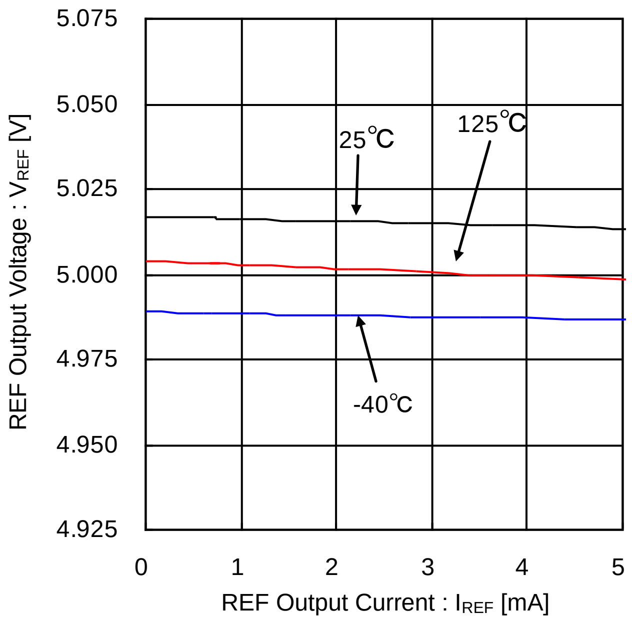


Figure 22. REF Output Voltage vs REF Output Current (REF Output Load Regulation (V_{DD1}=10V))

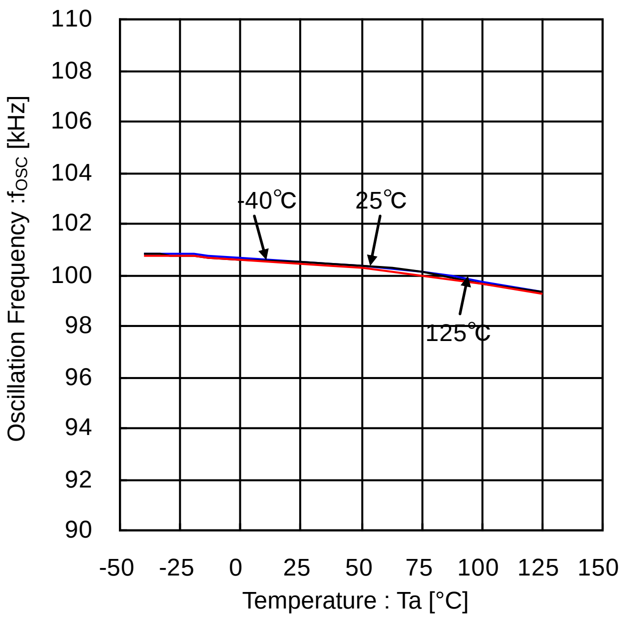


Figure 23. Oscillation Frequency at 100kHz vs Temperature

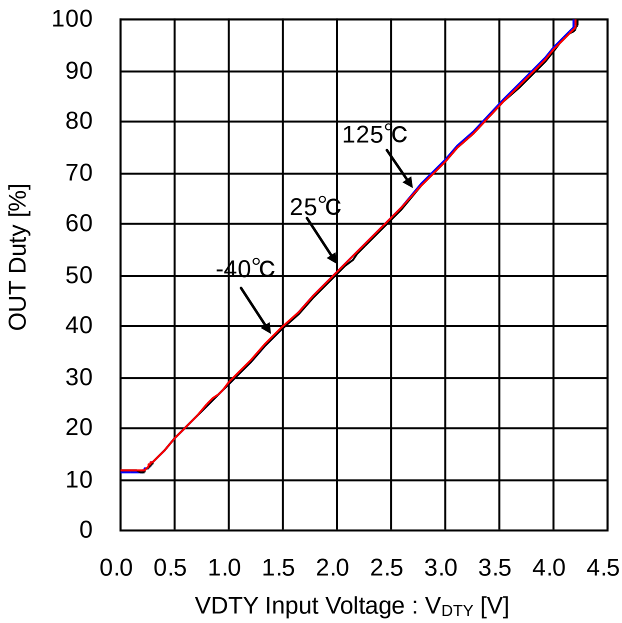


Figure 24. OUT Duty vs VDTY Input Voltage (VDTY-DUTY Characteristic at 100kHz)

Typical Performance Curves - continued

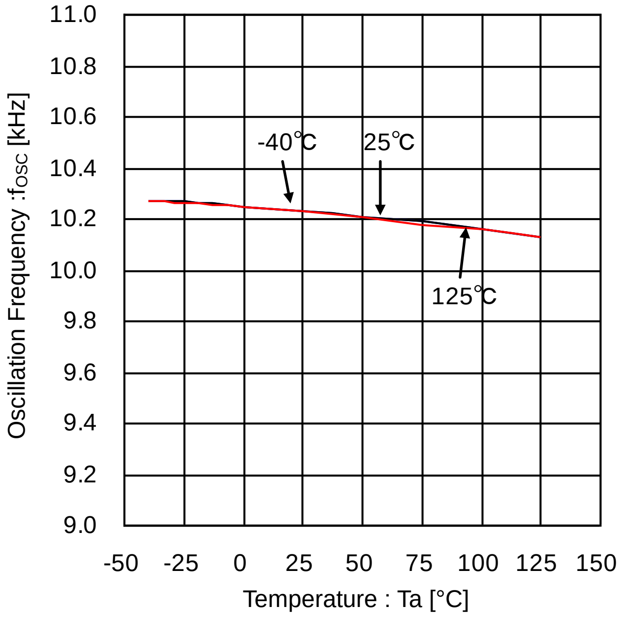


Figure 25. Oscillation Frequency at 10kHz vs Temperature

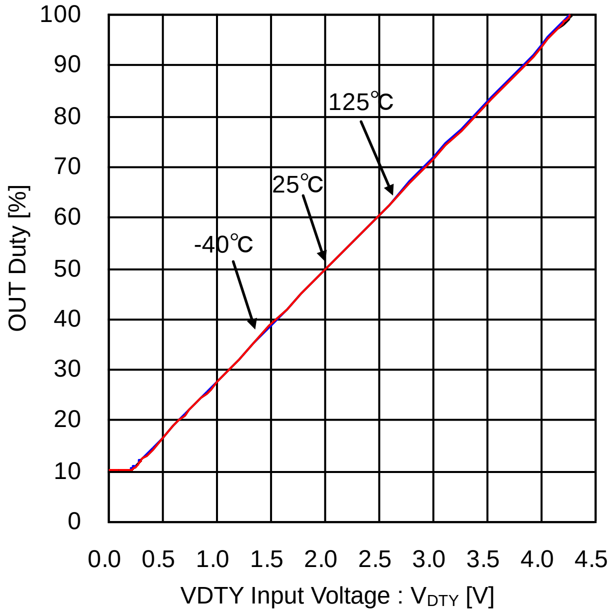


Figure 26. OUT Duty vs VDTY Input Voltage (VDTY-DUTY Characteristic at 10kHz)

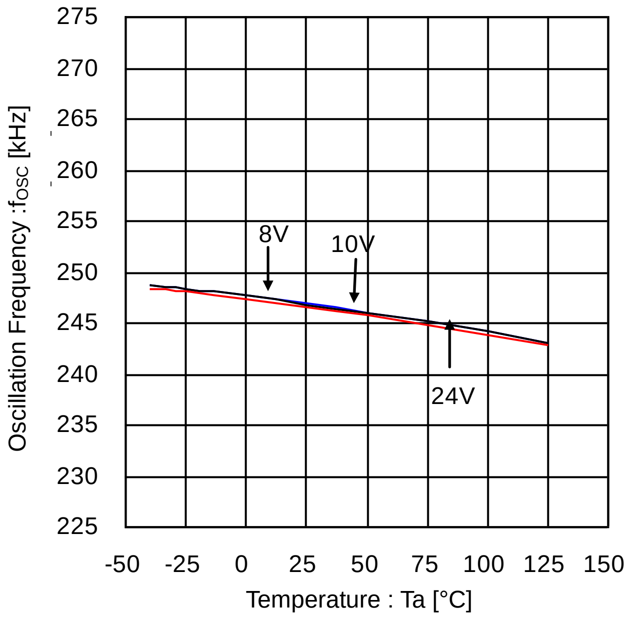


Figure 27. Oscillation Frequency at 250kHz vs Temperature

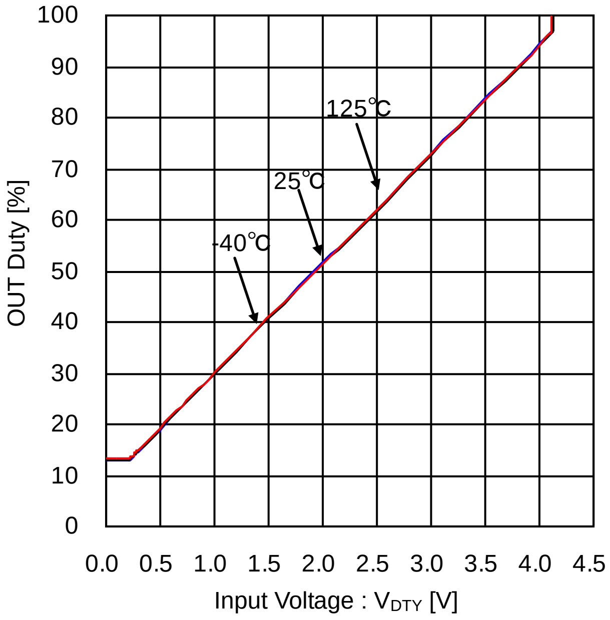


Figure 28. OUT Duty vs Input Voltage (VDTY-DUTY Characteristic at 250kHz)

Typical Performance Curves - continued

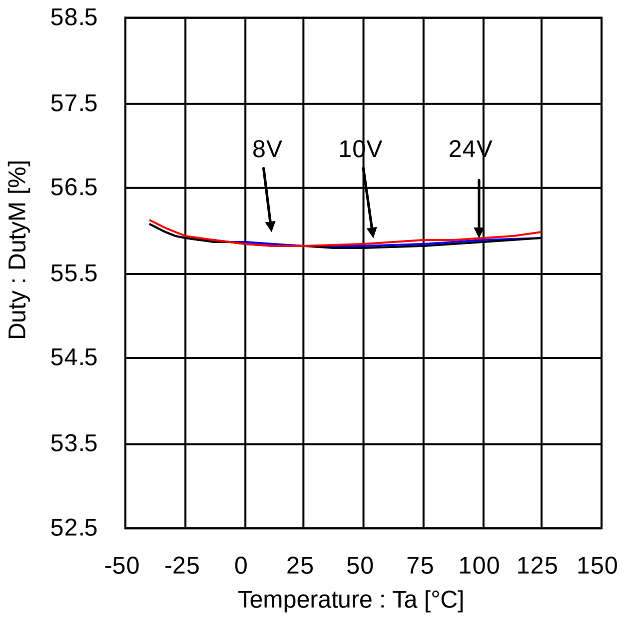


Figure 29. Duty at 100kHz vs Temperature

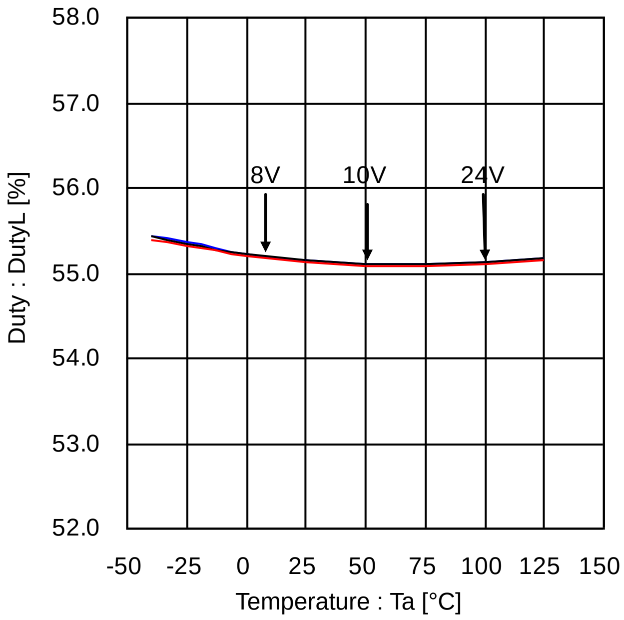


Figure 30. Duty at 10kHz vs Temperature

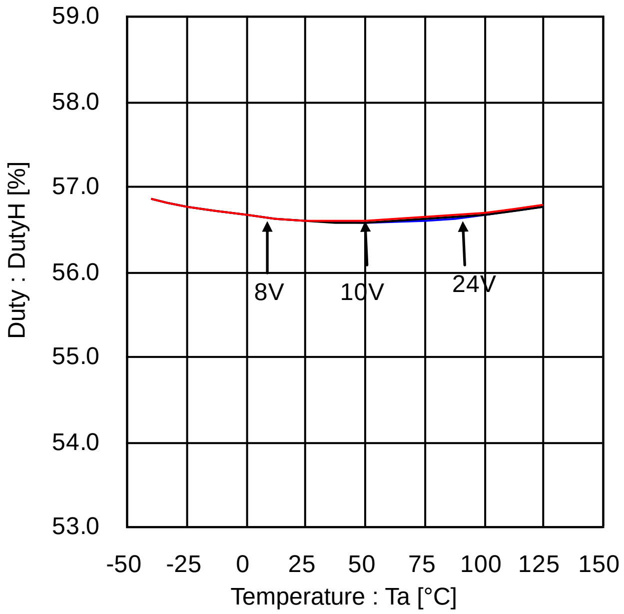


Figure 31. Duty at 250kHz vs Temperature

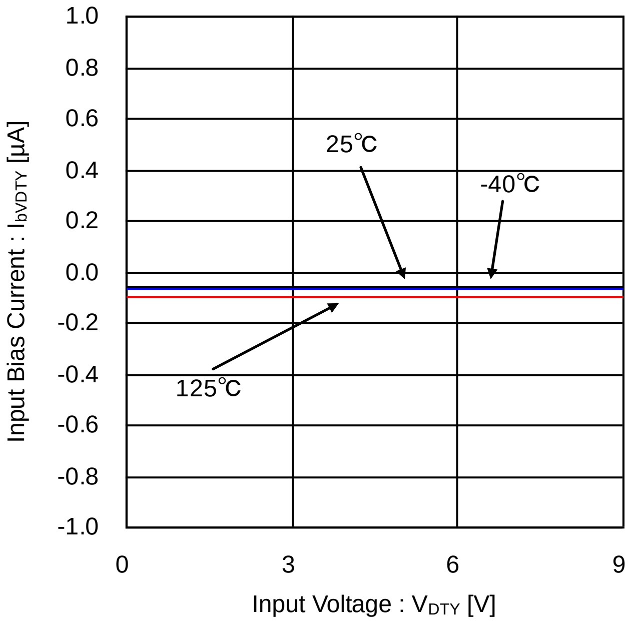


Figure 32. Input Bias Current vs VDTY Input Voltage

Typical Performance Curves - continued

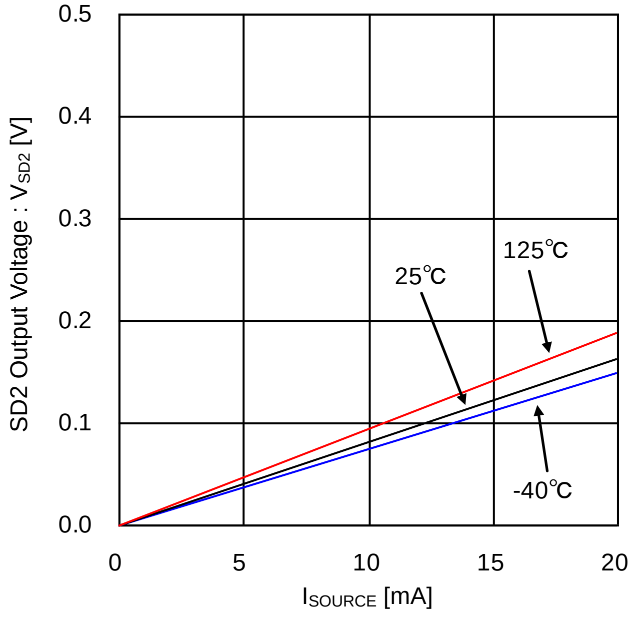


Figure 33. SD2 Output Voltage

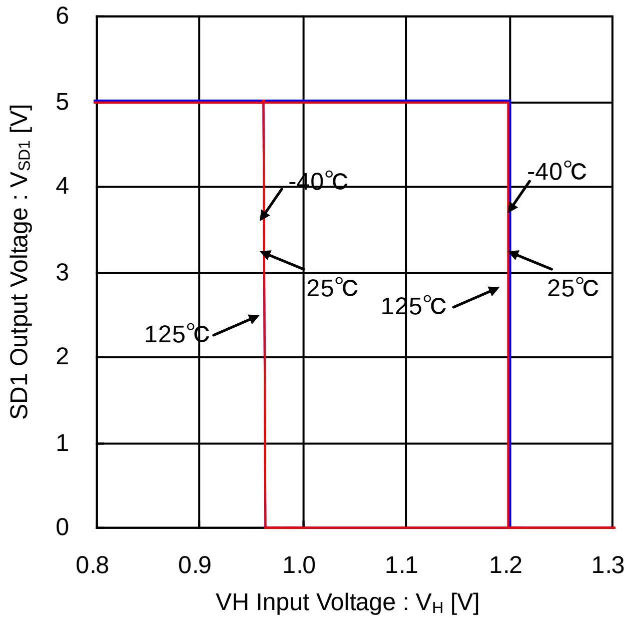


Figure 34. SD1 Output Voltage vs VH Input Voltage (Low Voltage Detect/Release Threshold)

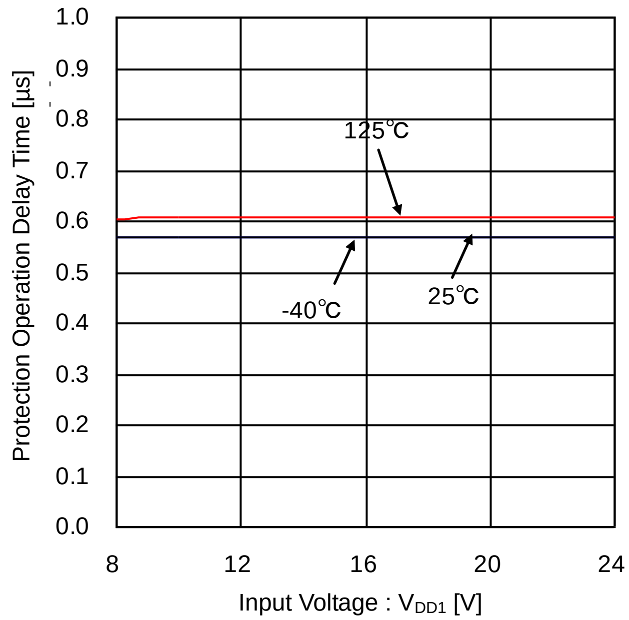


Figure 35. Protection Operation Delay Time vs Input Voltage (Low Voltage Detect Delay Time)

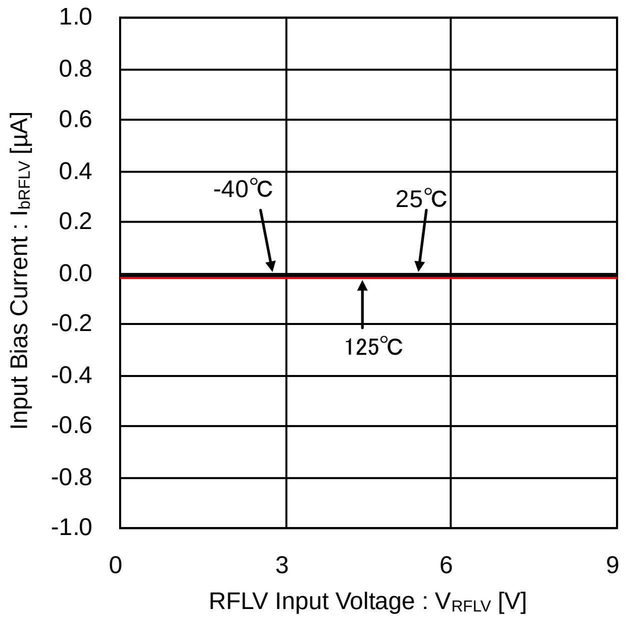


Figure 36. Input Bias Current vs RFLV Input Voltage

Typical Performance Curves - continued

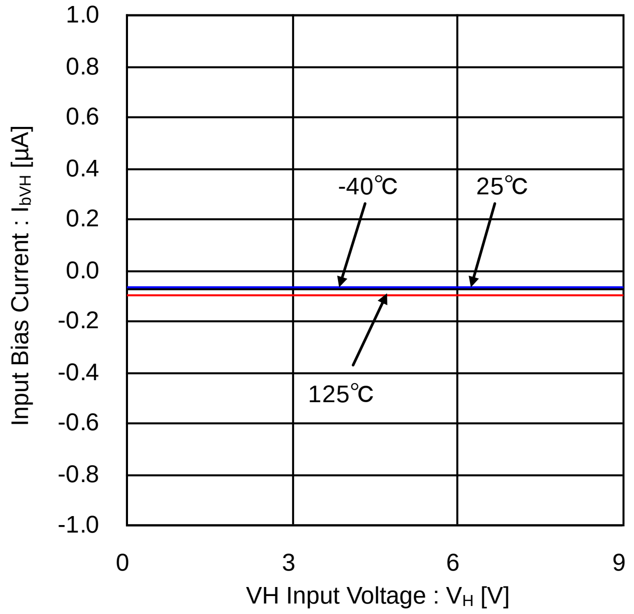


Figure 37. Input Bias Current vs VH Input Voltage

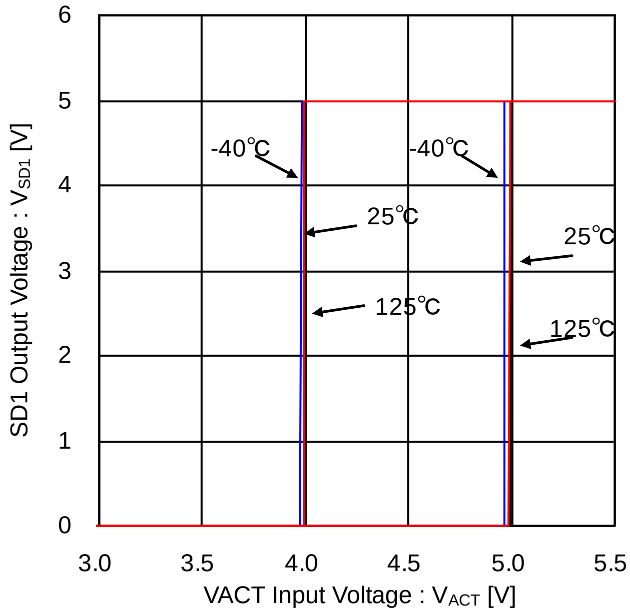


Figure 38. SD1 Output Voltage vs VACT Input Voltage
(Active High Voltage Detect/Release Threshold)

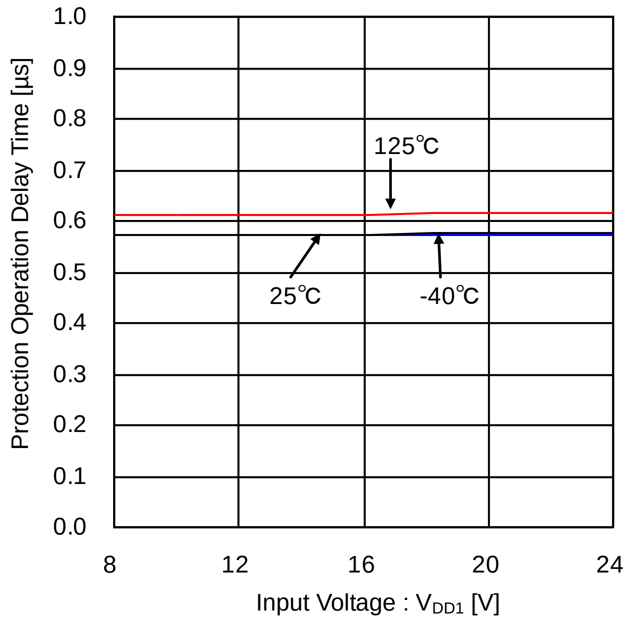


Figure 39. Protection Operation Delay Time vs Input Voltage
(Active High Voltage Detect Delay Time)

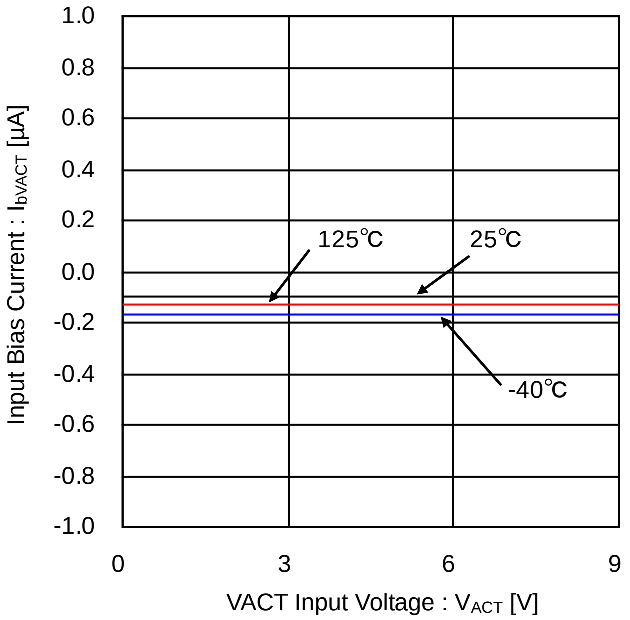


Figure 40. Input Bias Current vs VACT Input Voltage

Typical Performance Curves - continued

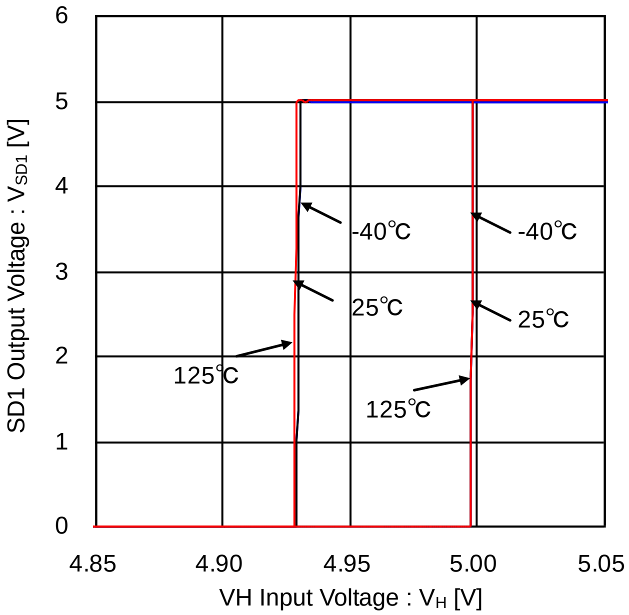


Figure 41. SD1 Output Voltage vs VH Input Voltage
(High Voltage Detect/Release Threshold)

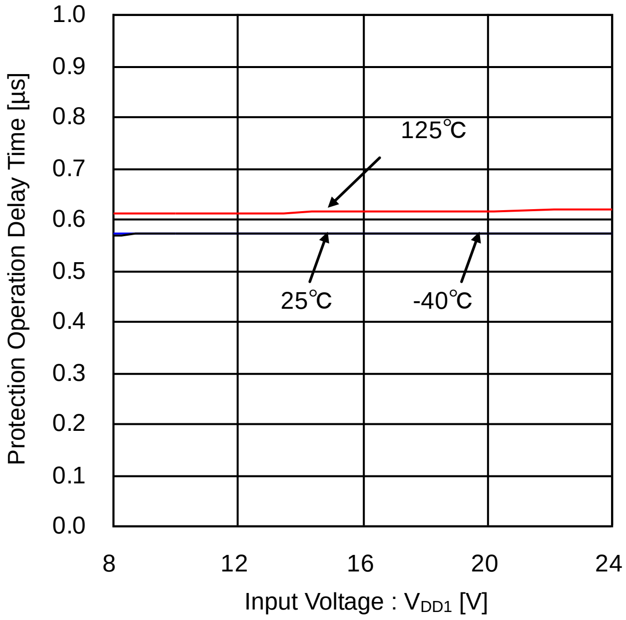


Figure 42. Protection Operation Delay Time
vs Input Voltage
(High Voltage Detect/Release Threshold)

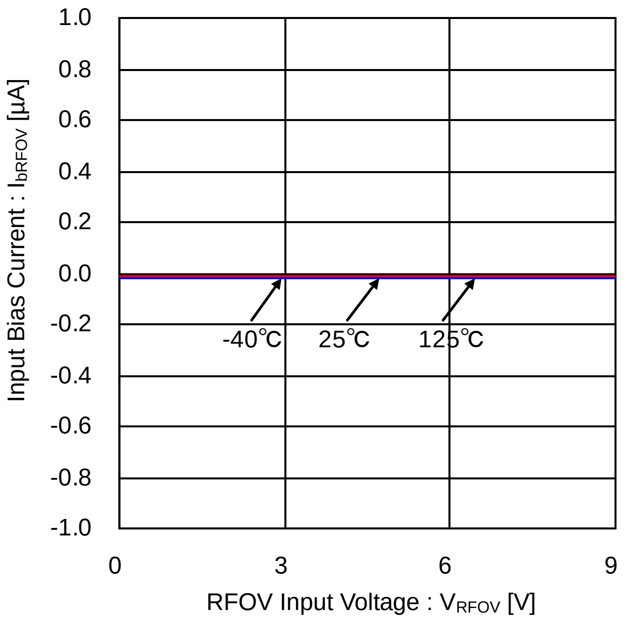


Figure 43. Input Bias Current vs RFOV Input Voltage

External Resistor

(1) VH,VDTY External Resistors

VH terminal is used to monitor the occurrences of over and under voltage condition.
VDTY is used to determine the output Duty.
Voltage is provided to both terminals by a voltage divider circuit.
Over voltage is detected when VH voltage> RFOV, while under voltage is detected when VH< RFLV voltage×0.8.
Voltage-divider resistor ratio is determined according to the high voltage to be monitored and to be detection voltage.
When R3 of Figure 44 is removed, internal diodes clamp VH and VDTY voltages to VDD+Vf. At this condition, design the values of R1 and R2 that will keep VH and VDTY currents below 2mA.

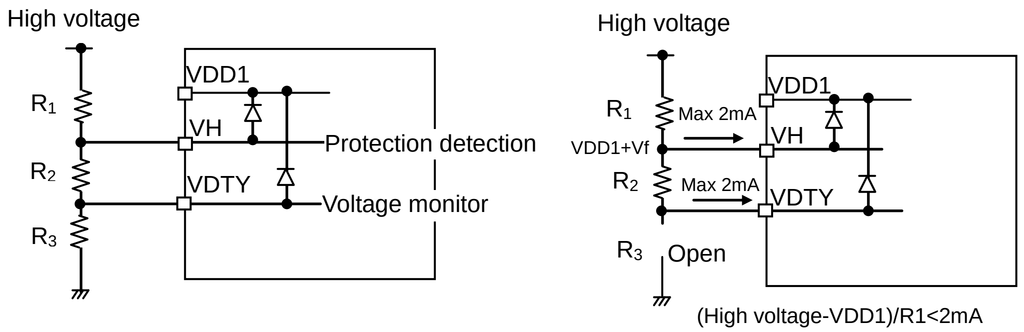


Figure 44. VH,VDTY Partial Resistance

(2) RFOV,RFLV External Resistors

RFOV sets the reference value for OVP, while RFLV sets the reference for UVP.
The resistor values to be used should always keep the load current of REF below 5mA.

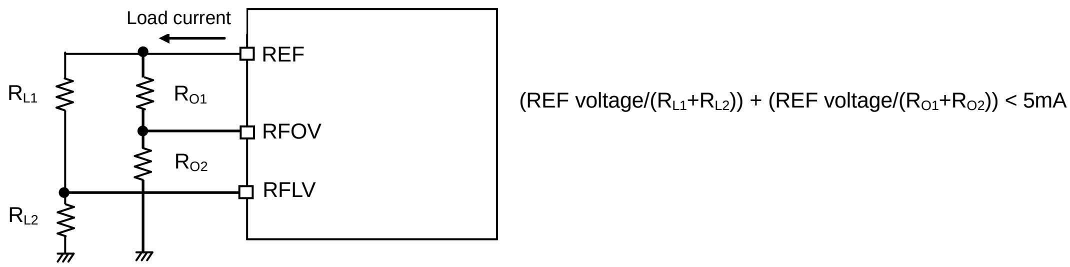


Figure 45. RFOV,RFLV Partial Resistance

(3) RT External Resistors

RT terminal is used to set the current of the internal reference oscillator.
Reference frequency is F_OSC=(1.0*10^6)/(RT resistance) [kHz].
Upper limit of set frequency is 250 kHz (RT=4kΩ), and lower limit is 10 kHz (RT=100kΩ).

RT Resistance	Frequency
100kΩ	10kHz
10kΩ	100kHz
4kΩ	250kHz

Figure 46. RT Resistance and Frequency

(4) SD2 Resistance

SD2 terminal is an open drain output terminal. Connect pull-up resistor between SD2 and power source to use it. RSD resistance value should keep the current of SD2 terminal below 20mA.

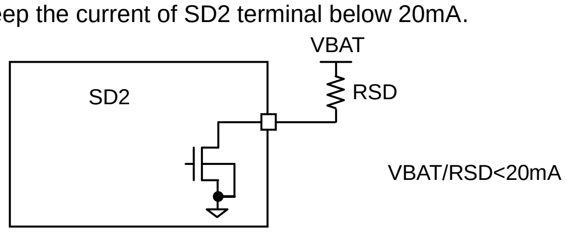
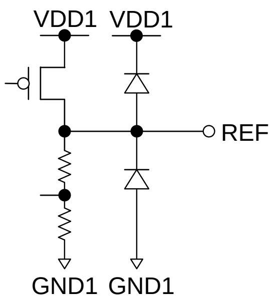


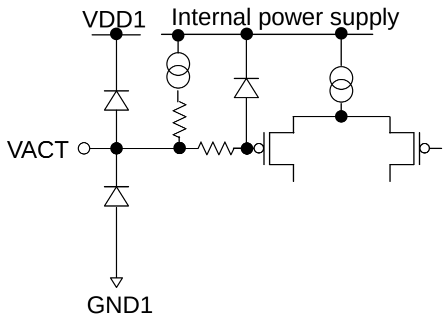
Figure 47. SD2 Resistance

I/O Equivalent Circuits

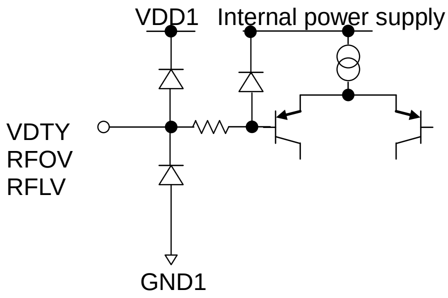
○REF



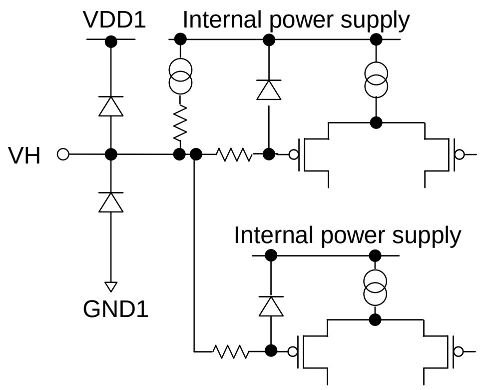
○VACT



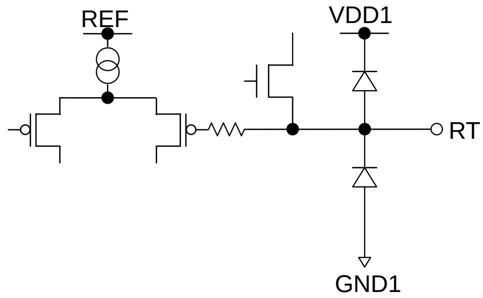
○VDTY, RFOV, RFLV



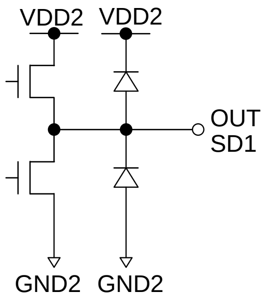
○VH



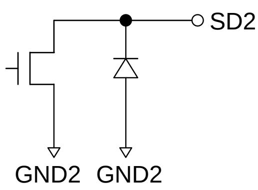
○RT



○OUT,SD1



○SD2



Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply terminals.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded, the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned OFF completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. **Unused Input Terminals**
    Input terminals of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input terminals should be connected to the power supply or ground line.

Operational Notes – continued

12. Regarding Input Pins of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

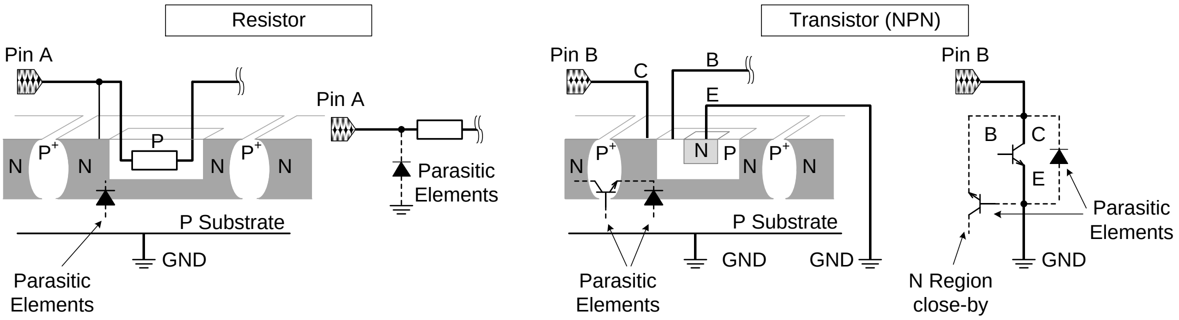


Figure 49. Example of Monolithic IC Structure

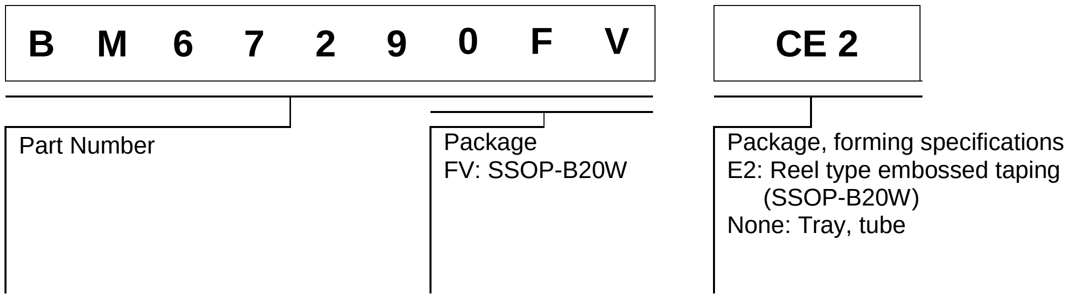
13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

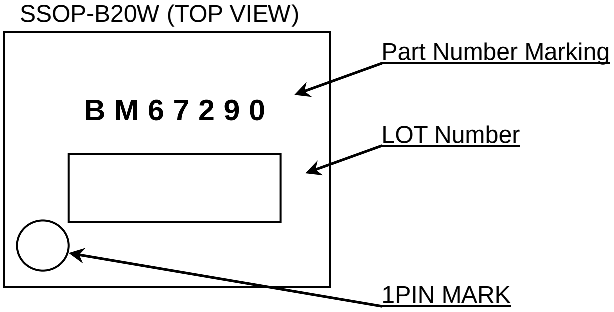
14. Over-Current Protection Circuit (OCP)

This IC has a built-in overcurrent protection circuit that activates when the output is accidentally shorted. However, it is strongly advised not to subject the IC to prolonged shorting of the output.

Ordering Information

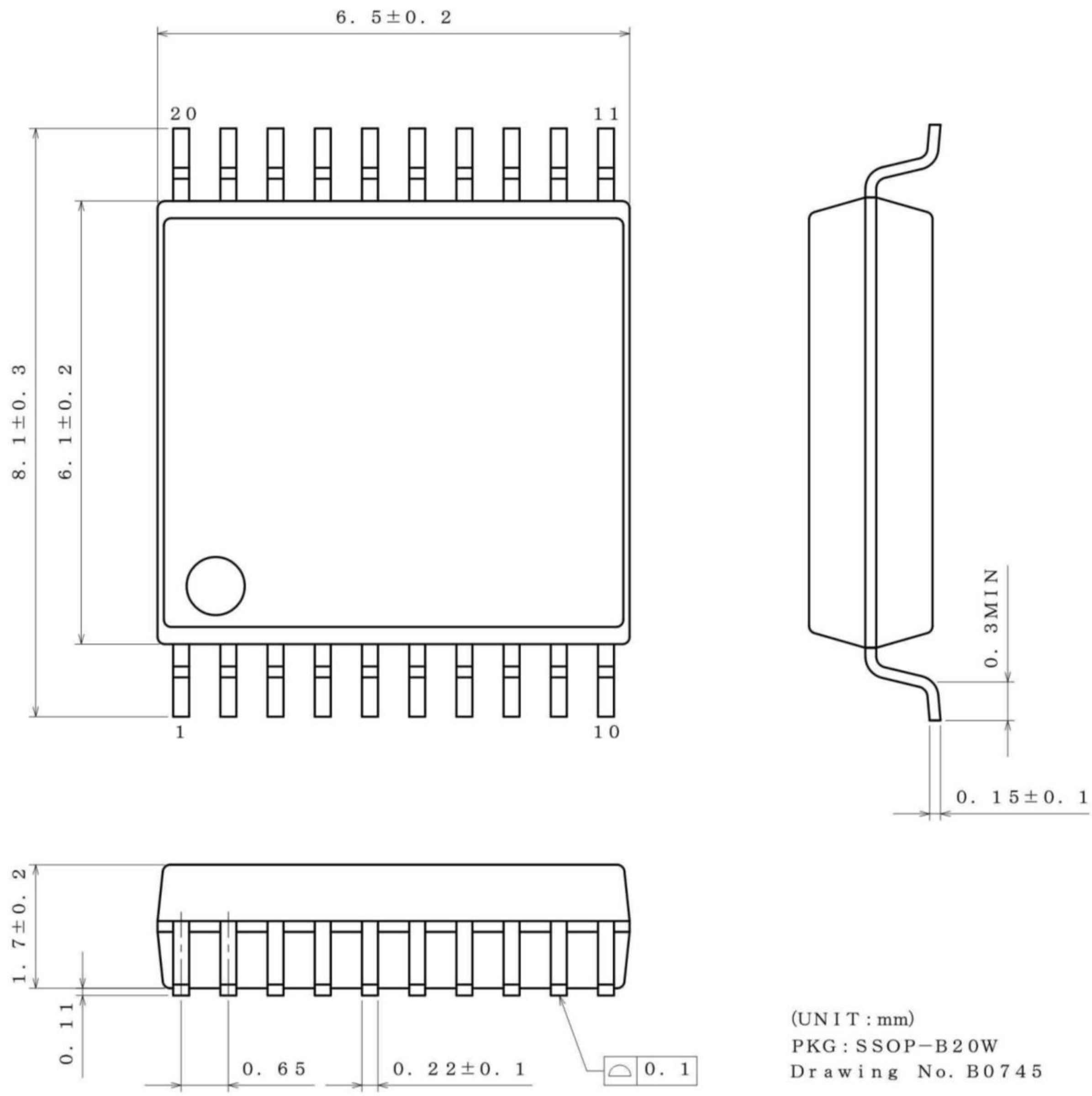


Marking Diagram



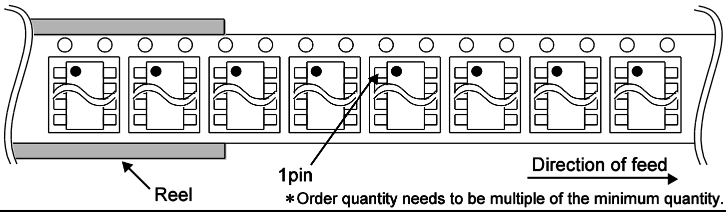
Physical Dimension, Tape and Reel Information

Package Name	SSOP-B20W



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

Revision History

Date	Revision	Changes
10.Nov.2014	001	New Release
19.Jul.2016	002	P1 Modify Figure 1 P12 Modify VH,VDTY,VACT,RFOV,RFLV Absolute Maximum Ratings P12 Modify OUT,SD1 Absolute Maximum Ratings P12 Delete Power Dissipation P13 Add Thermal Resistance P13 Modify Note7 P13 Add Insulation Related Characteristics P14 Modify Duty Temperature Property/Electric Property Variation Ratio Symbol ⊿DUTY/DUTY ⇒⊿DUTY P15 Modify RLOV⇒RFOV P15 Isurce⇒Isource P21 Modify I_{bvdty}⇒I_{bRFLV} P22 Modify I_{bvdty}⇒I_{bVH} P23 Modify I_{bvdty}⇒I_{bVACT} P23 Modify I_{bvdty}⇒I_{bRFOV} P24 Modify Figure.14⇒Figure.44 P25 Modify OUT/SD1 Equivalent Circuits GND⇒GND2

Notice

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

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2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

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This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
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   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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