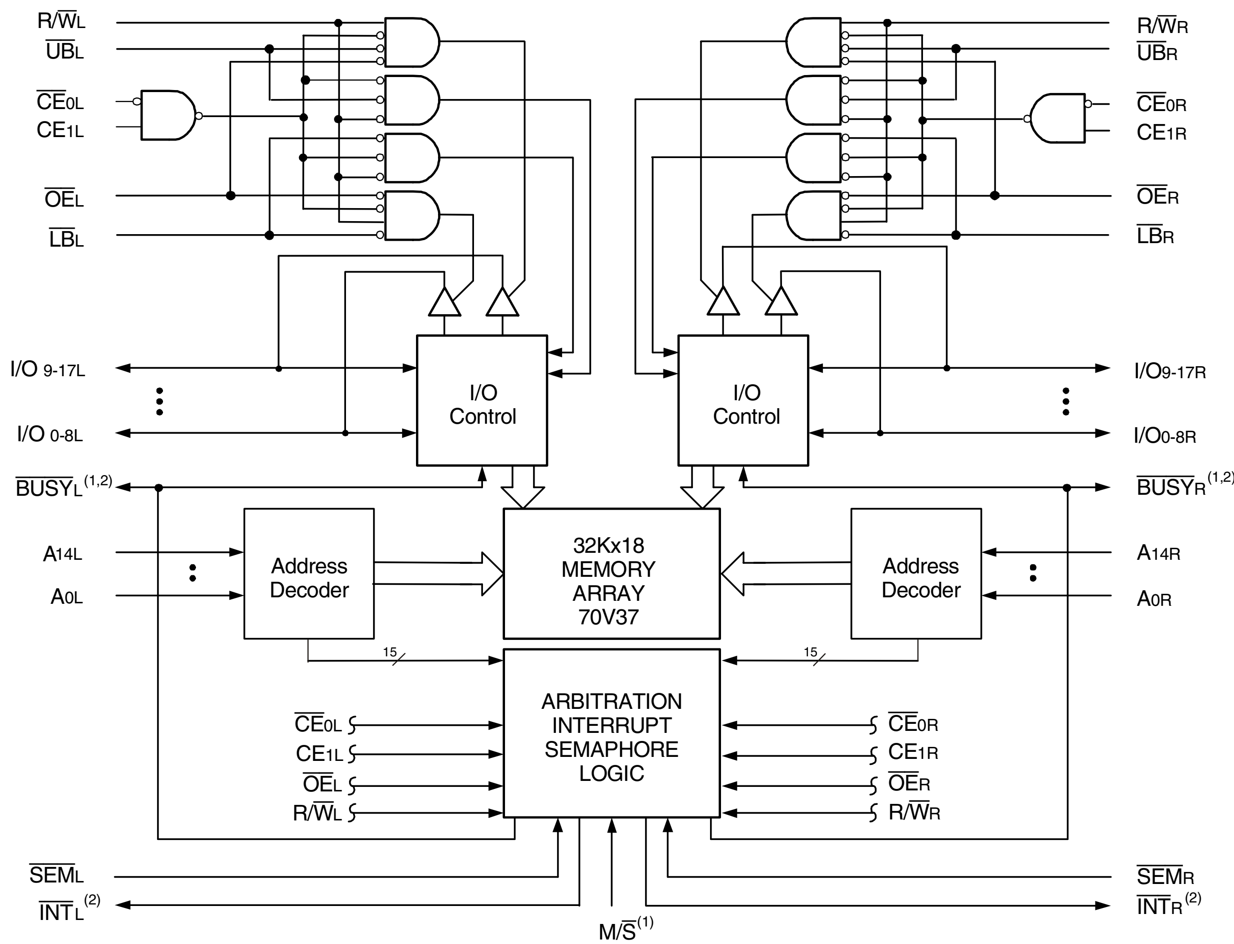
HIGH-SPEED 3.3V 32K x 18 DUAL-PORT STATIC RAM

IDT70V37L

Features

- True Dual-Ported memory cells which allow simultaneous access of the same memory location
- High-speed access
  - *Commercial: 15/20ns (max.)*
  - *Industrial: 20ns (max.)*
- Low-power operation
  - *IDT70V37L*
    Active: 440mW (typ.)
    Standby: 660μW (typ.)
- Dual chip enables allow for depth expansion without external logic
- IDT70V37 easily expands data bus width to 36 bits or more using the Master/Slave select when cascading more than one device
- M/S̄ = VIH for BUSY̅ output flag on Master, M/S̄ = VIL for BUSY̅ input on Slave
- Busy and Interrupt Flags
- On-chip port arbitration logic
- Full on-chip hardware support of semaphore signaling between ports
- Fully asynchronous operation from either port
- Separate upper-byte and lower-byte controls for multiplexed bus and bus matching compatibility
- LVTTL-compatible, single 3.3V (±0.3V) power supply
- Available in a 100-pin TQFP
- Industrial temperature range (–40°C to +85°C) is available for selected speeds
- Green parts available, see ordering information

Functional Block Diagram



NOTES:
1. BUSY̅ is an input as a Slave (M/S̄=VIL) and an output when it is a Master (M/S̄=VIH).
2. BUSY̅ and INT̅ are non-tri-state totem-pole outputs (push-pull).

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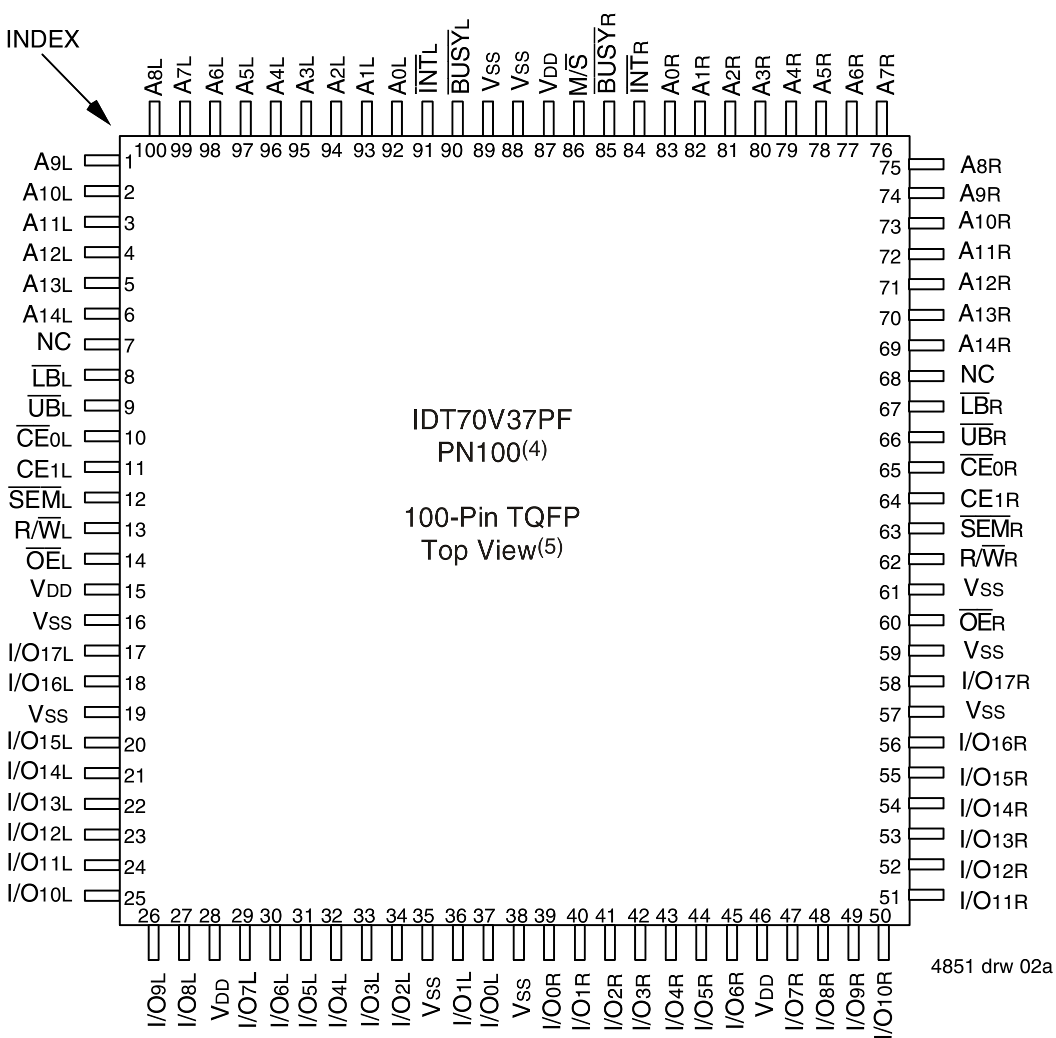
Description

The IDT70V37 is a high-speed 32K x 18 Dual-Port Static RAM. The IDT70V37 is designed to be used as a stand-alone 576K-bit Dual-Port RAM or as a combination MASTER/SLAVE Dual-Port RAM for 36-bit-or-more word system. Using the IDT MASTER/SLAVE Dual-Port RAM approach in 36-bit or wider memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

This device provides two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature controlled by the chip enables (either $\overline{CE}_0$ or CE_1) permit the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using CMOS high-performance technology, these devices typically operate on only 440mW of power. The IDT70V37 is packaged in a 100-pin Thin Quad Flatpack (TQFP).

Pin Configurations(1,2,3)



NOTES:
1. All VDD pins must be connected to power supply.
2. All VSS pins must be connected to ground.
3. Package body is approximately 14mm x 14mm x 1.4mm.
4. This package code is used to reference the package diagram.
5. This text does not indicate orientation of the actual part-marking.

Pin Names

Left Port	Right Port	Names
$\overline{CE}_{0L}$, CE_{1L}	$\overline{CE}_{0R}$, CE_{1R}	Chip Enables
R/$\overline{W}_L$	R/$\overline{W}_R$	Read/Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
A_{0L} - A_{14L}	A_{0R} - A_{14R}	Address
I/O_{0L} - I/O_{17L}	I/O_{0R} - I/O_{17R}	Data Input/Output
$\overline{SEM}_L$	$\overline{SEM}_R$	Semaphore Enable
$\overline{UB}_L$	$\overline{UB}_R$	Upper Byte Select
$\overline{LB}_L$	$\overline{LB}_R$	Lower Byte Select
$\overline{INT}_L$	$\overline{INT}_R$	Interrupt Flag
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Busy Flag
M/$\overline{S}$		Master or Slave Select
V_{DD}		Power (3.3V)
V_{SS}		Ground (0V)

4851 tbl 01

Absolute Maximum Ratings(1)

Symbol	Rating	Commercial & Industrial	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-65 to +150	°C
I_{OUT}	DC Output Current	50	mA

4851 tbl 02

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed V_{DD} + 0.3V for more than 25% of the cycle time or 10ns maximum, and is limited to $\leq$ 20mA for the period of $V_{TERM} \geq V_{DD}$ + 0.3V.

Maximum Operating Temperature and Supply Voltage(1)

Grade	Ambient Temperature(1)	GND	V_{DD}
Commercial	0°C to +70°C	0V	3.3V $\pm$ 0.3V
Industrial	-40°C to +85°C	0V	3.3V $\pm$ 0.3V

4851 tbl 03

NOTE:
1. This is the parameter T_A. This is the "instant on" case temperature.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	3.0	3.3	3.6	V
V_{SS}	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.0	—	V_{DD}+0.3(2)	V
V_{IL}	Input Low Voltage	-0.3(1)	—	0.8	V

4851 tbl 04

NOTES:
1. $V_{IL} \geq$ -1.5V for pulse width less than 10ns.
2. V_{TERM} must not exceed V_{DD} + 0.3V.

Capacitance(1) (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	9	pF
C_{OUT}(2)	Output Capacitance	V_{OUT} = 0V	10	pF

4851 tbl 05

NOTES:
1. This parameter is determined by device characterization but is not production tested.
2. C_{OUT} also references $C_{I/O}$.

Truth Table I – Chip Enable[1,2]

$\overline{CE}$	$\overline{CE}_0$	CE_1	Mode
L	V_{IL}	V_{IH}	Port Selected (TTL Active)
	$\le$ 0.2V	$\ge V_{DD}$ -0.2V	Port Selected (CMOS Active)
H	V_{IH}	X	Port Deselected (TTL Inactive)
	X	V_{IL}	Port Deselected (TTL Inactive)
	$\ge V_{DD}$ -0.2V	X[3]	Port Deselected (CMOS Inactive)
	X[3]	$\le$0.2V	Port Deselected (CMOS Inactive)

4852 tbl 06

NOTES:
1. Chip Enable references are shown above with the actual $\overline{CE}_0$ and CE_1 levels; $\overline{CE}$ is a reference only.
2. 'H' = V_{IH} and 'L' = V_{IL}.
3. CMOS standby requires 'X' to be either $\le$ 0.2V or $\ge V_{DD}$-0.2V.

Truth Table II – Non-Contention Read/Write Control

Inputs[1]						Outputs		Mode
$\overline{CE}$[2]	R/$\overline{W}$	$\overline{OE}$	$\overline{UB}$	$\overline{LB}$	$\overline{SEM}$	I/O_{9-17}	I/O_{0-8}	
H	X	X	X	X	H	High-Z	High-Z	Deselected: Power-Down
X	X	X	H	H	H	High-Z	High-Z	Both Bytes Deselected
L	L	X	L	H	H	$DATA_{IN}$	High-Z	Write to Upper Byte Only
L	L	X	H	L	H	High-Z	$DATA_{IN}$	Write to Lower Byte Only
L	L	X	L	L	H	$DATA_{IN}$	$DATA_{IN}$	Write to Both Bytes
L	H	L	L	H	H	$DATA_{OUT}$	High-Z	Read Upper Byte Only
L	H	L	H	L	H	High-Z	$DATA_{OUT}$	Read Lower Byte Only
L	H	L	L	L	H	$DATA_{OUT}$	$DATA_{OUT}$	Read Both Bytes
X	X	H	X	X	X	High-Z	High-Z	Outputs Disabled

4851 tbl 07

NOTES:
1. A_{0L} — $A_{14L} \neq A_{0R}$ — A_{14R}
2. Refer to Truth Table I - Chip Enable.

Truth Table III – Semaphore Read/Write Control[1]

Inputs[1]						Outputs		Mode
$\overline{CE}$[2]	R/$\overline{W}$	$\overline{OE}$	$\overline{UB}$	$\overline{LB}$	$\overline{SEM}$	I/O_{9-17}	I/O_{0-8}	
H	H	L	X	X	L	$DATA_{OUT}$	$DATA_{OUT}$	Read Data in Semaphore Flag
X	H	L	H	H	L	$DATA_{OUT}$	$DATA_{OUT}$	Read Data in Semaphore Flag
H	↑	X	X	X	L	$DATA_{IN}$	$DATA_{IN}$	Write I/O_0 into Semaphore Flag
X	↑	X	H	H	L	$DATA_{IN}$	$DATA_{IN}$	Write I/O_0 into Semaphore Flag
L	X	X	L	X	L	——	——	Not Allowed
L	X	X	X	L	L	——	——	Not Allowed

4851 tbl 08

NOTES:
1. There are eight semaphore flags written to I/O_0 and read from all the I/Os (I/O_0-I/O_{17}). These eight semaphore flags are addressed by A_0-A_2.
2. Refer to Truth Table I - Chip Enable.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V_{DD} = 3.3V ± 0.3V)

Symbol	Parameter	Test Conditions	70V37L		Unit
			Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current(1)	V_{DD} = 3.6V, V_{IN} = 0V to V_{DD}	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$(2) = V_{IH}, V_{OUT} = 0V to V_{DD}	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = +4mA	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	V

4851 tbl 09

NOTES:
1. At V_{DD} ≤ 2.0V, input leakages are undefined.
2. Refer to Truth Table I - Chip Enable.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range(5) (V_{DD} = 3.3V ± 0.3V)

Symbol	Parameter	Test Condition	Version		70V37L15 Com'l Only		70V37L20 Com'l & Ind		Unit
					Typ.(1)	Max.	Typ.(1)	Max.	
I_{DD}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL}, Outputs Disabled $\overline{SEM}$ = V_{IH} f = f_{MAX}(2)	COM'L	L	145	235	135	205	mA
			IND	L	—	—	135	220	
I_{SB1}	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L$ = $\overline{CE}_R$ = V_{IH} $\overline{SEM}_R$ = $\overline{SEM}_L$ = V_{IH} f = f_{MAX}(2)	COM'L	L	40	70	35	55	mA
			IND	L	—	—	35	65	
I_{SB2}	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}_{"A"}$ = V_{IL} and $\overline{CE}_{"B"}$ = V_{IH}(4) Active Port Outputs Disabled, f=f_{MAX}(2), $\overline{SEM}_R$ = $\overline{SEM}_L$ = V_{IH}	COM'L	L	100	155	90	140	mA
			IND	L	—	—	90	150	
I_{SB3}	Full Standby Current (Both Ports - All CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{DD} - 0.2V, V_{IN} ≥ V_{DD} - 0.2V or V_{IN} ≤ 0.2V, f = 0(3) $\overline{SEM}_R$ = $\overline{SEM}_L$ ≥ V_{DD} - 0.2V	COM'L	L	0.2	3.0	0.2	3.0	mA
			IND	L	—	—	0.2	3.0	
I_{SB4}	Full Standby Current (One Port - All CMOS Level Inputs)	$\overline{CE}_{"A"}$ ≤ 0.2V and $\overline{CE}_{"B"}$ ≥ V_{DD} - 0.2V(4), $\overline{SEM}_R$ = $\overline{SEM}_L$ ≥ V_{DD} - 0.2V, V_{IN} ≥ V_{DD} - 0.2V or V_{IN} ≤ 0.2V, Active Port Outputs Disabled, f = f_{MAX}(2)	COM'L	L	95	150	90	135	mA
			IND	L	—	—	90	145	

4851 tbl 10

NOTES:
1. V_{DD} = 3.3V, T_A = +25°C, and are not production tested. $I_{DD\ DC}$ = 90mA (Typ.)
2. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/t_{RC}, and using "AC Test Conditions" of input levels of GND to 3V.
3. f = 0 means no address or control lines change.
4. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
5. Refer to Truth Table I - Chip Enable.

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns Max.
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	Figures 1 and 2

4851 tbl 11

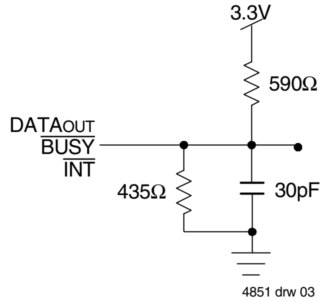


Figure 1. AC Output Load

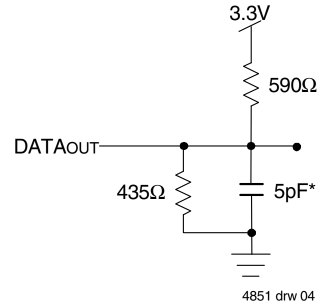
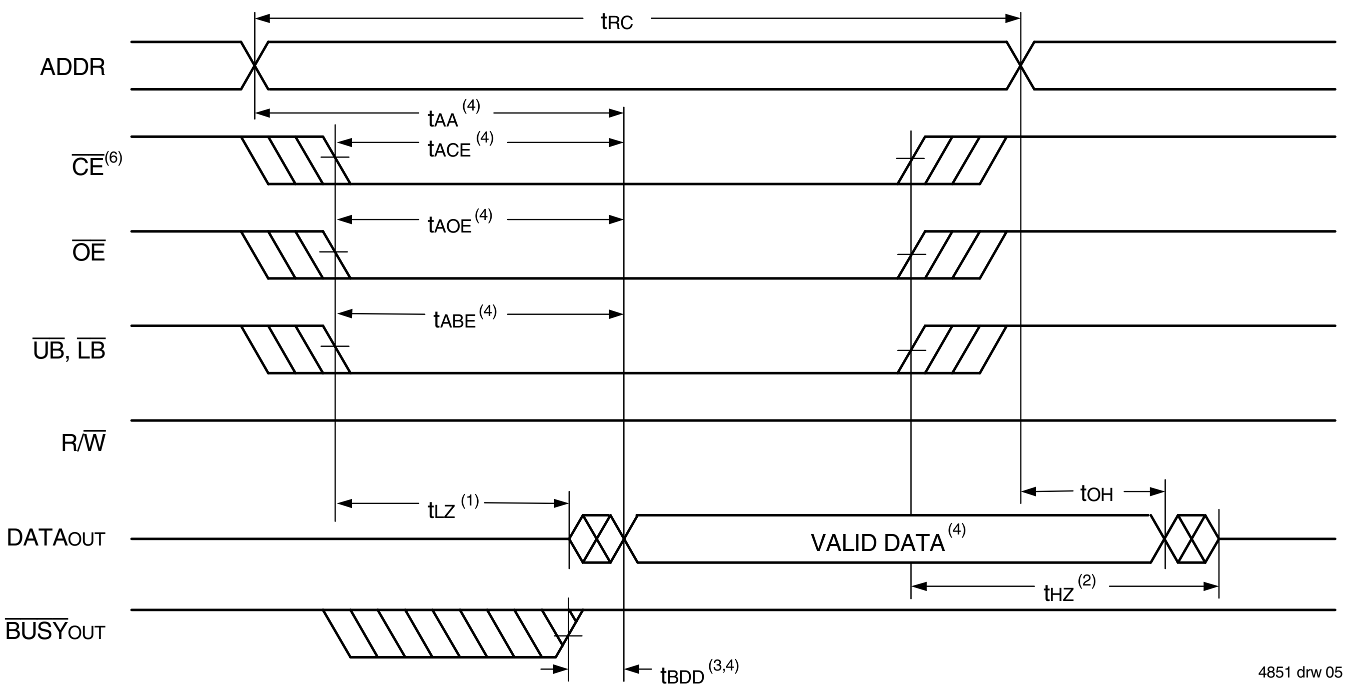
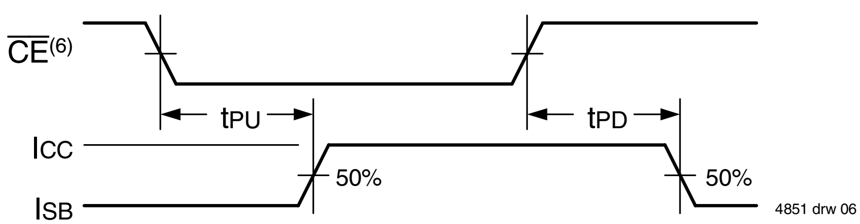


Figure 2. Output Test Load
(for t_{LZ}, t_{HZ}, t_{WZ}, t_{OW})
* Including scope and jig.

Waveform of Read Cycles(5)



Timing of Power-Up Power-Down



NOTES:
1. Timing depends on which signal is asserted last, $\overline{OE}$, $\overline{CE}$, $\overline{LB}$ or $\overline{UB}$.
2. Timing depends on which signal is de-asserted first $\overline{CE}$, $\overline{OE}$, $\overline{LB}$ or $\overline{UB}$.
3. t_{BDD} delay is required only in cases where the opposite port is completing a write operation to the same address location. For simultaneous read operations $\overline{BUSY}$ has no relation to valid output data.
4. Start of valid data depends on which timing becomes effective last t_{AOE}, t_{ACE}, t_{AA} or t_{BDD}.
5. $\overline{SEM}$ = V_{IH}.
6. Refer toTruth Table I - Chip Enable.

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range

Symbol	Parameter	70V37L15 Com'l Only		70V37L20 Com'l & Ind		Unit
		Min.	Max.	Min.	Max.	
READ CYCLE						
t_{RC}	Read Cycle Time	15	—	20	—	ns
t_{AA}	Address Access Time	—	15	—	20	ns
t_{ACE}	Chip Enable Access Time(3)	—	15	—	20	ns
t_{ABE}	Byte Enable Access Time(3)	—	15	—	20	ns
t_{AOE}	Output Enable Access Time	—	10	—	12	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	ns
t_{LZ}	Output Low-Z Time(1,2)	3	—	3	—	ns
t_{HZ}	Output High-Z Time(1,2)	—	10	—	10	ns
t_{PU}	Chip Enable to Power Up Time(2)	0	—	0	—	ns
t_{PD}	Chip Disable to Power Down Time(2)	—	15	—	20	ns
t_{SOP}	Semaphore Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	10	—	10	—	ns
t_{SAA}	Semaphore Address Access Time	—	15	—	20	ns

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AC Electrical Characteristics Over the Operating Temperature and Supply Voltage

Symbol	Parameter	70V37L15 Com'l Only		70V37L20 Com'l & Ind		Unit
		Min.	Max.	Min.	Max.	
WRITE CYCLE						
t_{WC}	Write Cycle Time	15	—	20	—	ns
t_{EW}	Chip Enable to End-of-Write(3)	12	—	15	—	ns
t_{AW}	Address Valid to End-of-Write	12	—	15	—	ns
t_{AS}	Address Set-up Time(3)	0	—	0	—	ns
t_{WP}	Write Pulse Width	12	—	15	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	ns
t_{DW}	Data Valid to End-of-Write	10	—	15	—	ns
t_{HZ}	Output High-Z Time(1,2)	—	10	—	10	ns
t_{DH}	Data Hold Time(4)	0	—	0	—	ns
t_{WZ}	Write Enable to Output in High-Z(1,2)	—	10	—	10	ns
t_{OW}	Output Active from End-of-Write(1,2,4)	0	—	0	—	ns
t_{SWRD}	$\overline{SEM}$ Flag Write to Read Time	5	—	5	—	ns
t_{SPS}	$\overline{SEM}$ Flag Contention Window	5	—	5	—	ns

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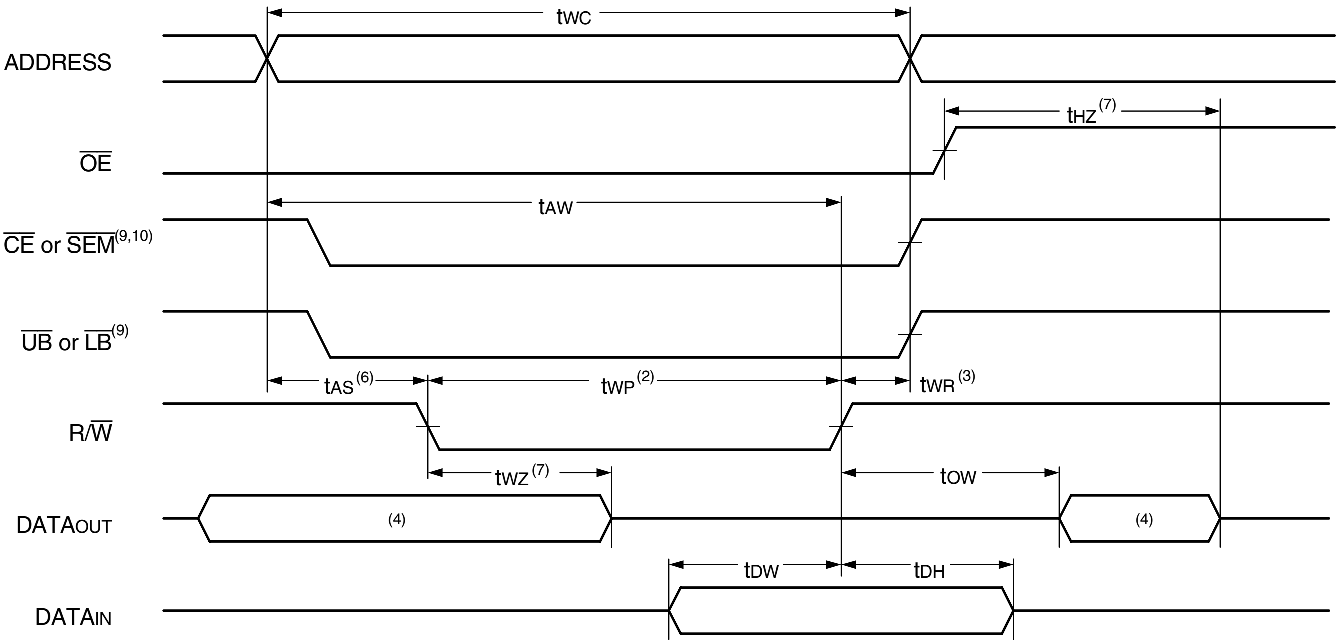
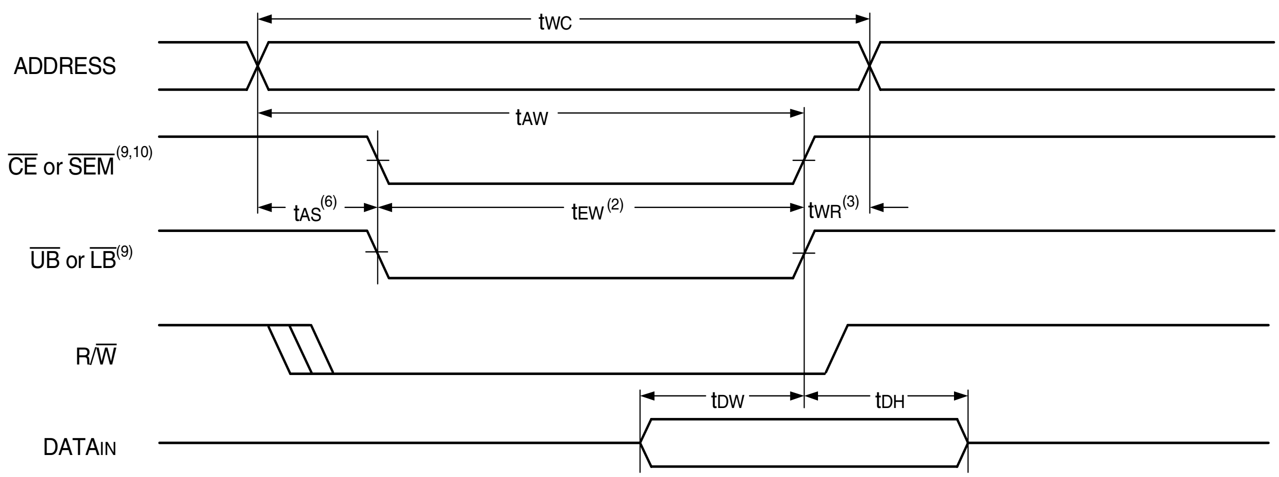
NOTES:
1. Transition is measured 0mV from Low or High-impedance voltage with Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. To access RAM, $\overline{CE}$= V_{IL} and $\overline{SEM}$ = V_{IH}. To access semaphore, $\overline{CE}$ = V_{IH} and $\overline{SEM}$ = V_{IL}. Either condition must be valid for the entire t_{EW} time.
4. The specification for t_{DH} must be met by the device supplying write data to the RAM under all operating conditions. Although t_{DH} and t_{OW} values will vary over voltage and temperature, the actual t_{DH} will always be smaller than the actual t_{OW}.

Timing Waveform of Write Cycle No. 1, R/$\overline{W}$ Controlled Timing(1,5,8)



4851 drw 07

Timing Waveform of Write Cycle No. 2, $\overline{CE}$ Controlled Timing(1,5)

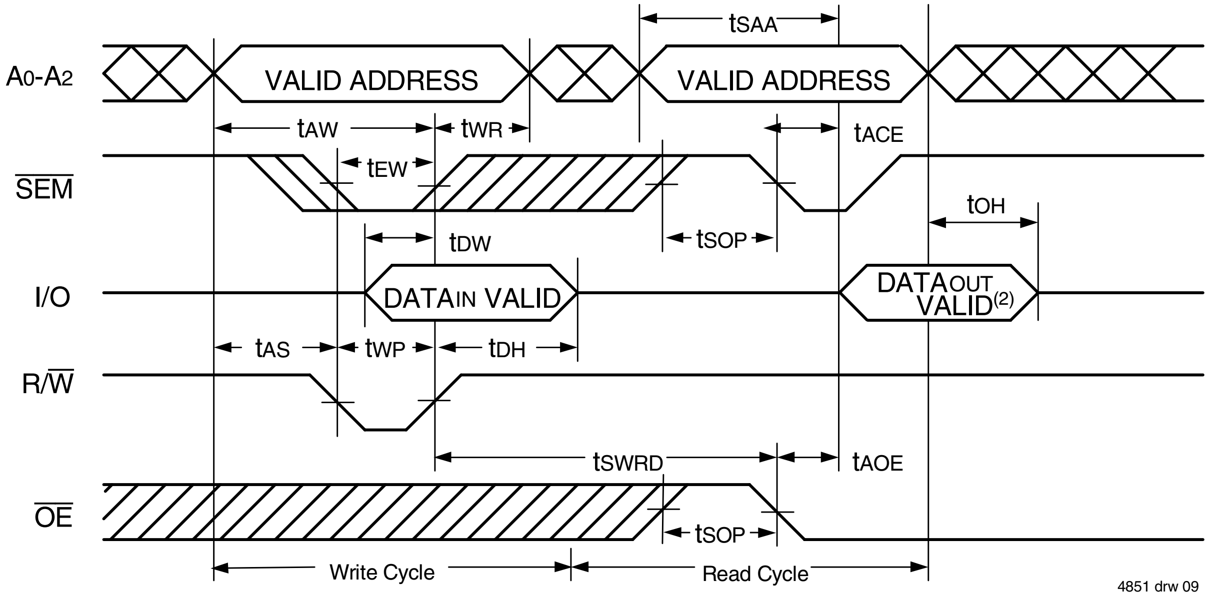


4851 drw 08

NOTES:

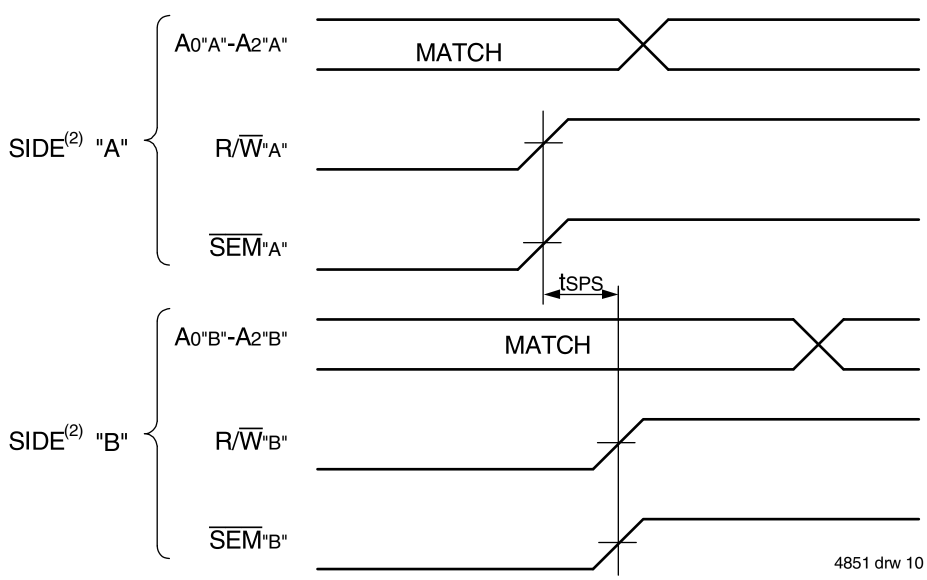
1. R/$\overline{W}$ or $\overline{CE}$ or $\overline{UB}$ and $\overline{LB}$ = V_{IH} during all address transitions.
2. A write occurs during the overlap (t_{EW} or t_{WP}) of a $\overline{CE}$ = V_{IL} and a R/$\overline{W}$ = V_{IL} for memory array writing cycle.
3. t_{WR} is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ (or $\overline{SEM}$ or R/$\overline{W}$) going HIGH to the end of write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CE}$ or $\overline{SEM}$ = V_{IL} transition occurs simultaneously with or after the R/$\overline{W}$ = V_{IL} transition, the outputs remain in the High-impedance state.
6. Timing depends on which enable signal is asserted last, $\overline{CE}$ or R/$\overline{W}$.
7. This parameter is guaranteed by device characterization, but is not production tested. Transition is measured 0mV from steady state with the Output Test Load (Figure 2).
8. If $\overline{OE}$ = V_{IL} during R/W controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ = V_{IH} during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.
9. To access RAM, $\overline{CE}$ = V_{IL} and $\overline{SEM}$ = V_{IH}. To access semaphore, $\overline{CE}$ = V_{IH} and $\overline{SEM}$ = V_{IL}. t_{EW} must be met for either condition.
10. Refer to Truth Table I - Chip Enable.

Timing Waveform of Semaphore Read after Write Timing, Either Side[1]



NOTES:
1. CE = VIH or UB and LB = VIH for the duration of the above timing (both write and read cycle) (Refer to Truth Table I - Chip Enable).
2. "DATAOUT VALID" represents all I/O's (I/O0 - I/O17) equal to the semaphore value.

Timing Waveform of Semaphore Write Contention[1,3,4]



NOTES:
1. DOR = DOL = VIL, CEL = CER = VIH or both UB and LB = VIH (Refer to Truth Table I - Chip Enable).
2. All timing is the same for left and right ports. Port "A" may be either left or right port. "B" is the opposite from port "A".
3. This parameter is measured from R/W"A" or SEM"A" going HIGH to R/W"B" or SEM"B" going HIGH.
4. If tSPS is not satisfied, the semaphore will fall positively to one side or the other, but there is no guarantee which side will be granted the semaphore flag.

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range

		70V37L15 Com'l Only		70V37L20 Com'l & Ind		
Symbol	Parameter	Min.	Max.	Min.	Max.	Unit
$\overline{BUSY}$ TIMING (M/$\overline{S}$=VIH)						
t_{BAA}	$\overline{BUSY}$ Access Time from Address Match	—	15	—	20	ns
t_{BDA}	$\overline{BUSY}$ Disable Time from Address Not Matched	—	15	—	20	ns
t_{BAC}	$\overline{BUSY}$ Access Time from Chip Enable Low	—	15	—	20	ns
t_{BDC}	$\overline{BUSY}$ Access Time from Chip Enable High	—	15	—	17	ns
t_{APS}	Arbitration Priority Set-up Time(2)	5	—	5	—	ns
t_{BDD}	$\overline{BUSY}$ Disable to Valid Data(3)	—	15	—	17	ns
t_{WH}	Write Hold After $\overline{BUSY}$(5)	12	—	15	—	ns
$\overline{BUSY}$ TIMING (M/$\overline{S}$=VIL)						
t_{WB}	$\overline{BUSY}$ Input to Write(4)	0	—	0	—	ns
t_{WH}	Write Hold After $\overline{BUSY}$(5)	12	—	15	—	ns
PORT-TO-PORT DELAY TIMING						
t_{WDD}	Write Pulse to Data Delay(1)	—	30	—	45	ns
t_{DDD}	Write Data Valid to Read Data Delay(1)	—	25	—	30	ns

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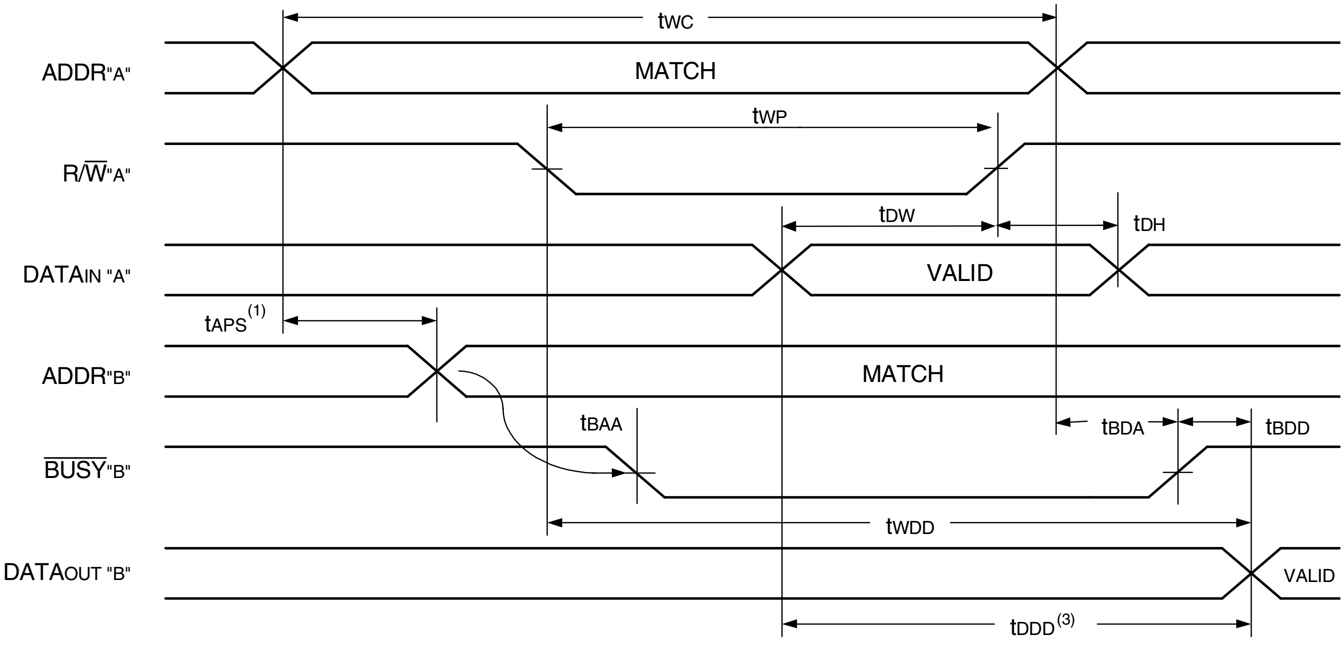
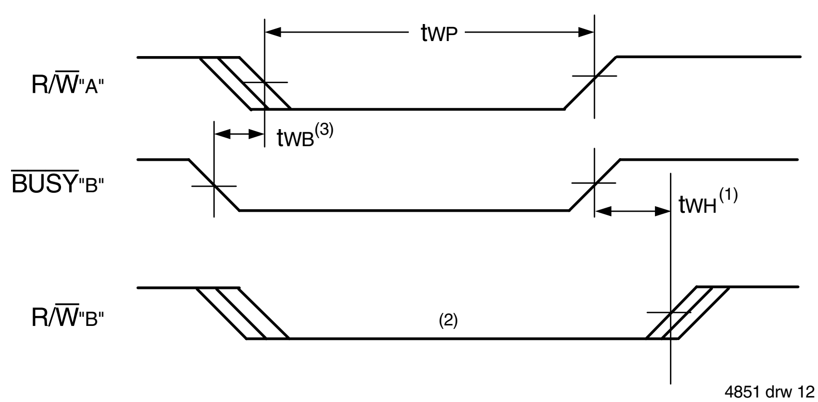
NOTES:
1. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Write with Port-to-Port Read and $\overline{BUSY}$ (M/$\overline{S}$ = V_{IH})".
2. To ensure that the earlier of the two ports wins.
3. t_{BDD} is a calculated parameter and is the greater of 0, t_{WDD} – t_{WP} (actual), or t_{DDD} – t_{DW} (actual).
4. To ensure that the write cycle is inhibited on port "B" during contention on port "A".
5. To ensure that a write cycle is completed on port "B" after contention on port "A".

Timing Waveform of Write with Port-to-Port Read and $\overline{BUSY}$ (M/$\overline{S}$ = V_{IH})(2,4,5)



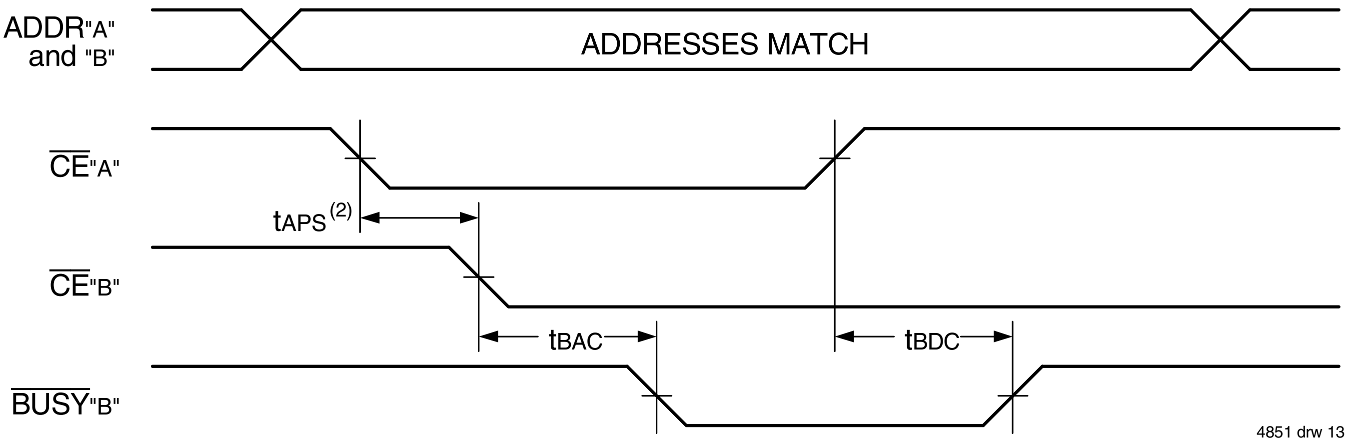
NOTES:
1. To ensure that the earlier of the two ports wins. t_{APS} is ignored for M/$\overline{S}$ = V_{IL} (SLAVE).
2. $\overline{CE}_L$ = $\overline{CE}_R$ = V_{IL}, refer to Truth Table I - Chip Enable.
3. $\overline{OE}$ = V_{IL} for the reading port.
4. If M/$\overline{S}$ = V_{IL} (slave), $\overline{BUSY}$ is an input. Then for this example $\overline{BUSY}$"A" = V_{IH} and $\overline{BUSY}$"B" input is shown above.
5. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from port "A".

Timing Waveform of Write with $\overline{BUSY}$ (M/$\overline{S}$ = V_{IL})

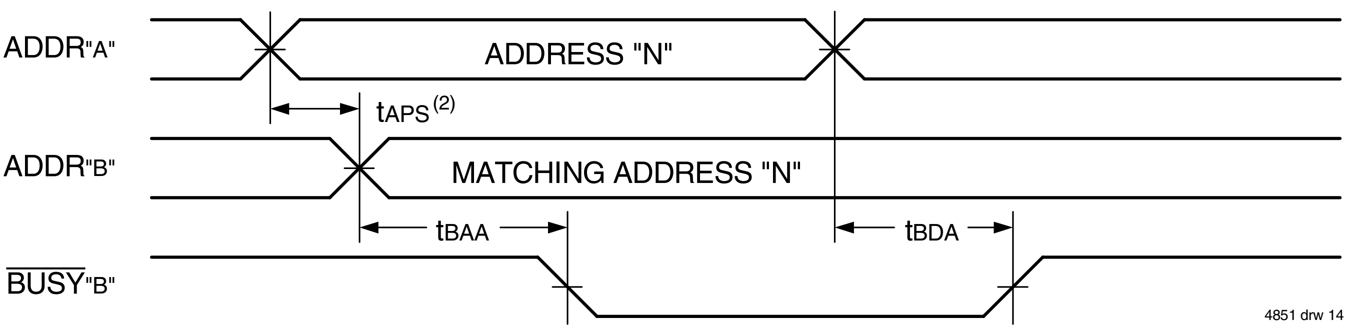


NOTES:
1. t_{WH} must be met for both $\overline{BUSY}$ input (SLAVE) and output (MASTER).
2. $\overline{BUSY}$ is asserted on port "B" blocking R/$\overline{W}$"B", until $\overline{BUSY}$"B" goes HIGH.
3. t_{WB} is only for the 'slave' version.

Waveform of $\overline{BUSY}$ Arbitration Controlled by $\overline{CE}$ Timing (M/$\overline{S}$ = VIH)(1,3)



Waveform of $\overline{BUSY}$ Arbitration Cycle Controlled by Address Match Timing (M/$\overline{S}$ = VIH)(1)



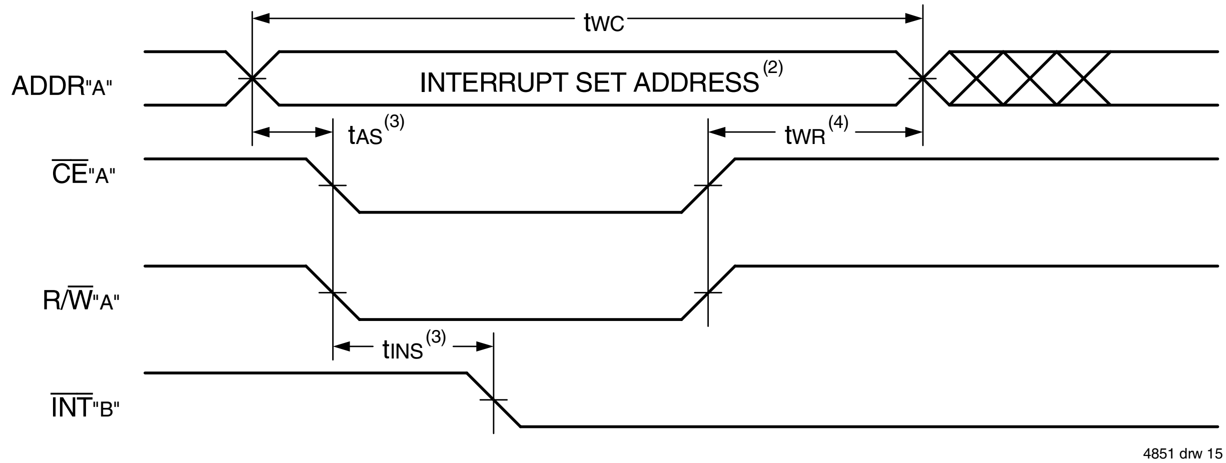
NOTES:
1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from port "A".
2. If tAPS is not satisfied, the $\overline{BUSY}$ signal will be asserted on one side or another but there is no guarantee on which side $\overline{BUSY}$ will be asserted.
3. Refer to Truth Table I - Chip Enable .

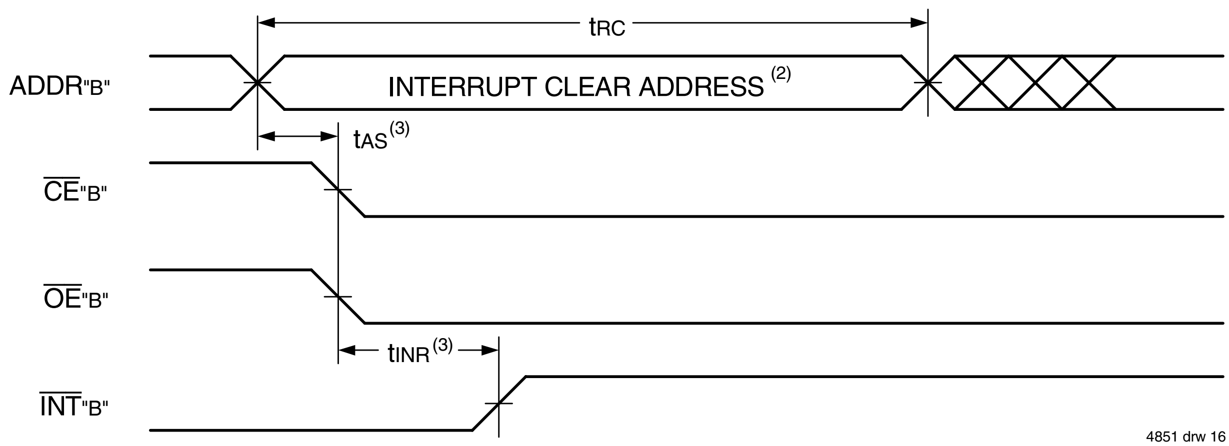
AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range

Symbol	Parameter	70V37L15 Com'l Only Min.	70V37L15 Com'l Only Max.	70V37L20 Com'l & Ind Min.	70V37L20 Com'l & Ind Max.	Unit
INTERRUPT TIMING						
tAS	Address Set-up Time	0	—	0	—	ns
tWR	Write Recovery Time	0	—	0	—	ns
tINS	Interrupt Set Time	—	15	—	20	ns
tINR	Interrupt Reset Time	—	15	—	20	ns

4851 tbl 15

Waveform of Interrupt Timing(1,5)





NOTES:
1. All timing is the same for left and right ports. Port “A” may be either the left or right port. Port “B” is the port opposite from port “A”.
2. Refer to Interrupt Truth Table.
3. Timing depends on which enable signal ($\overline{CE}$ or R/$\overline{W}$) is asserted last.
4. Timing depends on which enable signal ($\overline{CE}$ or R/$\overline{W}$) is de-asserted first.
5. Refer to Truth Table I - Chip Enable.

Truth Table IV — Interrupt Flag(1,4,5)

Left Port					Right Port					Function
R/$\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	A_{14L}-A_{0L}	$\overline{INT}_L$	R/$\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	A_{14R}-A_{0R}	$\overline{INT}_R$	
L	L	X	7FFF	X	X	X	X	X	L(2)	Set Right $\overline{INT}_R$ Flag
X	X	X	X	X	X	L	L	7FFF	H(3)	Reset Right $\overline{INT}_R$ Flag
X	X	X	X	L(3)	L	L	X	7FFE	X	Set Left $\overline{INT}_L$ Flag
X	L	L	7FFE	H(2)	X	X	X	X	X	Reset Left $\overline{INT}_L$ Flag

4851 tbl 16

NOTES:
1. Assumes $\overline{BUSY}_L$ = $\overline{BUSY}_R$ = V_{IH}.
2. If $\overline{BUSY}_L$ = V_{IL}, then no change.
3. If $\overline{BUSY}_R$ = V_{IL}, then no change.
4. $\overline{INT}_L$ and $\overline{INT}_R$ must be initialized at power-up.
5. Refer to Truth Table I - Chip Enable.

Truth Table V — Address $\overline{BUSY}$ Arbitration[4]

Inputs			Outputs		
$\overline{CE}_L$	$\overline{CE}_R$	A_{0L}-A_{14L} A_{0R}-A_{14R}	$\overline{BUSY}_L$[1]	$\overline{BUSY}_R$[1]	Function
X	X	NO MATCH	H	H	Normal
H	X	MATCH	H	H	Normal
X	H	MATCH	H	H	Normal
L	L	MATCH	(2)	(2)	Write Inhibit[3]

4851 tbl 17

NOTES:

1. Pins $\overline{BUSY}_L$ and $\overline{BUSY}_R$ are both outputs when the part is configured as a master. Both are inputs when configured as a slave. $\overline{BUSY}$ outputs on the IDT70V37 are push-pull, not open drain outputs. On slaves the $\overline{BUSY}$ input internally inhibits writes.
2. "L" if the inputs to the opposite port were stable prior to the address and enable inputs of this port. "H" if the inputs to the opposite port became stable after the address and enable inputs of this port. If t_{APS} is not met, either $\overline{BUSY}_L$ or $\overline{BUSY}_R$ = LOW will result. $\overline{BUSY}_L$ and $\overline{BUSY}_R$ outputs can not be LOW simultaneously.
3. Writes to the left port are internally ignored when $\overline{BUSY}_L$ outputs are driving LOW regardless of actual logic level on the pin. Writes to the right port are internally ignored when $\overline{BUSY}_R$ outputs are driving LOW regardless of actual logic level on the pin.
4. Refer to Truth Table I - Chip Enable.

Truth Table VI — Example of Semaphore Procurement Sequence[1,2,3]

Functions	D_0 - D_{17} Left	D_0 - D_{17} Right	Status
No Action	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Right Port Writes "0" to Semaphore	0	1	No change. Right side has no write access to semaphore
Left Port Writes "1" to Semaphore	1	0	Right port obtains semaphore token
Left Port Writes "0" to Semaphore	1	0	No change. Left port has no write access to semaphore
Right Port Writes "1" to Semaphore	0	1	Left port obtains semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free
Right Port Writes "0" to Semaphore	1	0	Right port has semaphore token
Right Port Writes "1" to Semaphore	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free

4851 tbl 18

NOTES:

1. This table denotes a sequence of events for only one of the eight semaphores on the IDT70V37.
2. There are eight semaphore flags written to via I/O_0 and read from all I/O's (I/O_0-I/O_{17}). These eight semaphores are addressed by A_0 - A_2.
3. $\overline{CE}$ = V_{IH}, $\overline{SEM}$ = V_{IL} to access the semaphores. Refer to the Truth Table III - Semaphore Read/Write Control.

Functional Description

The IDT70V37 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The IDT70V37 has an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}_0$ and CE_1 control the on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ = HIGH). When a port is enabled, access to the entire memory array is permitted.

Interrupts

If the user chooses the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag ($\overline{INT}_L$) is asserted when the right port writes to memory location 7FFE (HEX), where a write is defined as $\overline{CE}_R$ = $R/\overline{W}_R$ = V_{IL} per the Truth Table. The left port clears the interrupt through access of address location 7FFE when $\overline{CE}_L$ = $\overline{OE}_L$ = V_{IL}, $R/\overline{W}$ is a "don't care". Likewise, the right port interrupt flag ($\overline{INT}_R$) is asserted when the left port writes to memory location 7FFF (HEX) and to clear the interrupt flag ($\overline{INT}_R$), the right port must read the memory location 7FFF. The message (18 bits) at 7FFE or 7FFF is user-defined since it is an addressable SRAM location. If the interrupt function is not used, address locations 7FFE and 7FFF are not used as mail boxes, but as part of the random access memory. Refer to Truth Table IV for the interrupt operation.

Busy Logic

Busy Logic provides a hardware indication that both ports of the RAM have accessed the same location at the same time. It also allows one of the two accesses to proceed and signals the other side that the RAM is "Busy". The BUSY pin can then be used to stall the access until the operation on the other side is completed. If a write operation has been attempted from the side that receives a BUSY indication, the write signal is gated internally to prevent the write from proceeding.

The use of BUSY logic is not required or desirable for all applications. In some cases it may be useful to logically OR the BUSY outputs together and use any BUSY indication as an interrupt source to flag the event of an illegal or illogical operation. If the write inhibit function of BUSY logic is not desirable, the BUSY logic can be disabled by placing the part in slave mode with the M/S pin. Once in slave mode the BUSY pin operates solely as a write inhibit input pin. Normal operation can be programmed by tying the BUSY pins HIGH. If desired, unintended write operations can be prevented to a port by tying the BUSY pin for that port LOW.

The BUSY outputs on the IDT 70V37 RAM in master mode, are push-pull type outputs and do not require pull up resistors to operate. If these RAMs are being expanded in depth, then the BUSY indication for the resulting array requires the use of an external AND gate.

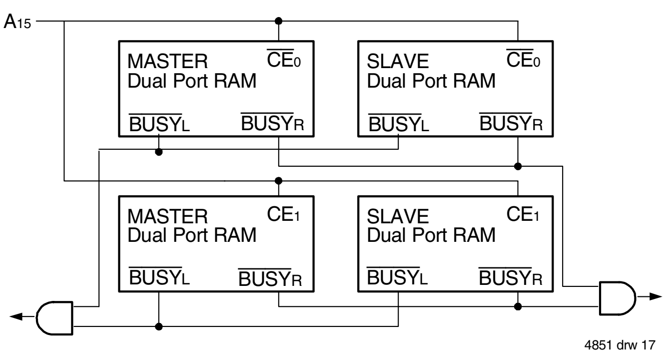


Figure 3. Busy and chip enable routing for both width and depth expansion with IDT70V37 RAMs.

Width Expansion with Busy Logic Master/Slave Arrays

When expanding an IDT70V37 RAM array in width while using BUSY logic, one master part is used to decide which side of the RAMs array will receive a BUSY indication, and to output that indication. Any number of slaves to be addressed in the same address range as the master use the BUSY signal as a write inhibit signal. Thus on the IDT70V37 RAM the BUSY pin is an output if the part is used as a master (M/S pin = V_{IH}), and the BUSY pin is an input if the part used as a slave (M/S pin = V_{IL}) as shown in Figure 3.

If two or more master parts were used when expanding in width, a split decision could result with one master indicating BUSY on one side of the array and another master indicating BUSY on one other side of the array. This would inhibit the write operations from one port for part of a word and inhibit the write operations from the other port for the other part of the word.

The BUSY arbitration on a master is based on the chip enable and address signals only. It ignores whether an access is a read or write. In a master/slave array, both address and chip enable must be valid long enough for a BUSY flag to be output from the master before the actual write pulse can be initiated with the R/W signal. Failure to observe this timing can result in a glitched internal write inhibit signal and corrupted data in the slave.

Semaphores

The IDT70V37 is an extremely fast Dual-Port 32K x 18 CMOS Static RAM with an additional 8 address locations dedicated to binary semaphore flags. These flags allow either processor on the left or right side of the Dual-Port RAM to claim a privilege over the other processor for functions defined by the system designer's software. As an example, the semaphore can be used by one processor to inhibit the other from accessing a portion of the Dual-Port RAM or any other shared resource.

The Dual-Port RAM features a fast access time, with both ports being completely independent of each other. This means that the activity on the left port in no way slows the access time of the right port. Both ports are identical in function to standard CMOS Static RAM and can be read from or written to at the same time with the only possible conflict arising from the simultaneous writing of, or a simultaneous READ/WRITE of, a non-semaphore location. Semaphores are protected against such ambiguous situations and may be used by the system program to avoid any conflicts in the non-semaphore portion of the Dual-Port RAM. These devices have an automatic power-down feature controlled by CE, the Dual-Port RAM enable, and SEM, the semaphore enable. The CE and SEM pins control on-chip power down circuitry that permits the respective port to go into standby mode when not selected. This is the condition which is shown in Truth Table III where CE and SEM are both HIGH.

Systems which can best use the IDT70V37 contain multiple processors or controllers and are typically very high-speed systems which are software controlled or software intensive. These systems can benefit from a performance increase offered by the IDT70V37s hardware semaphores, which provide a lockout mechanism without requiring complex programming.

Software handshaking between processors offers the maximum in system flexibility by permitting shared resources to be allocated in varying configurations. The IDT70V37 does not use its semaphore flags to control any resources through hardware, thus allowing the system designer total flexibility in system architecture.

An advantage of using semaphores rather than the more common methods of hardware arbitration is that wait states are never incurred in either processor. This can prove to be a major advantage in very high-speed systems.

How the Semaphore Flags Work

The semaphore logic is a set of eight latches which are independent of the Dual-Port RAM. These latches can be used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphores provide a hardware assist for a use assignment method called "Token Passing Allocation." In this method, the state of a semaphore latch is used as a token indicating that a shared resource is in use. If the left processor wants to use this resource, it requests the token by setting the latch. This processor then verifies its success in setting the latch by reading it. If it was successful, it proceeds to assume control over the shared resource. If it was not successful in setting the latch, it determines that the right side processor has set the latch first, has the token and is using the shared resource. The left processor can then either repeatedly request that semaphore's status or remove its request for that semaphore to perform another task and occasionally attempt again to gain control of the token via the set and test sequence. Once the right side has relinquished the token, the left side should succeed in gaining control.

The semaphore flags are active LOW. A token is requested by writing a zero into a semaphore latch and is released when the same side writes a one to that latch.

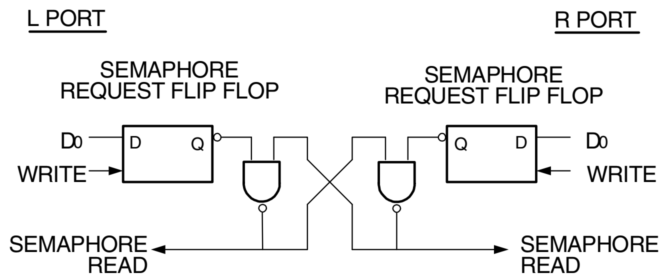
The eight semaphore flags reside within the IDT70V37 in a separate memory space from the Dual-Port RAM. This address space is accessed by placing a low input on the $\overline{SEM}$ pin (which acts as a chip select for the semaphore flags) and using the other control pins (Address, $\overline{CE}$, and R/$\overline{W}$) as they would be used in accessing a standard Static RAM. Each of the flags has a unique address which can be accessed by either side through address pins A_0 – A_2. When accessing the semaphores, none of the other address pins has any effect.

When writing to a semaphore, only data pin D_0 is used. If a low level is written into an unused semaphore location, that flag will be set to a zero on that side and a one on the other side (see Truth Table VI). That semaphore can now only be modified by the side showing the zero. When a one is written into the same location from the same side, the flag will be set to a one for both sides (unless a semaphore request from the other side is pending) and then can be written to by both sides. The fact that the side which is able to write a zero into a semaphore subsequently locks out writes from the other side is what makes semaphore flags useful in interprocessor communications. (A thorough discussion on the use of this feature follows shortly.) A zero written into the same location from the other side will be stored in the semaphore request latch for that side until the semaphore is freed by the first side.

When a semaphore flag is read, its value is spread into all data bits so that a flag that is a one reads as a one in all data bits and a flag containing a zero reads as all zeros. The read value is latched into one side's output register when that side's semaphore select ($\overline{SEM}$) and output enable ($\overline{OE}$) signals go active. This serves to disallow the semaphore from changing state in the middle of a read cycle due to a write cycle from the other side. Because of this latch, a repeated read of a semaphore in a test loop must cause either signal ($\overline{SEM}$ or $\overline{OE}$) to go inactive or the output will never change.

A sequence WRITE/READ must be used by the semaphore in order to guarantee that no system level contention will occur. A processor requests access to shared resources by attempting to write a zero into a semaphore location. If the semaphore is already in use, the semaphore request latch will contain a zero, yet the semaphore flag will appear as one, a fact which the processor will verify by the subsequent read (see Table VI). As an example, assume a processor writes a zero to the left port at a free semaphore location. On a subsequent read, the processor will verify that it has written successfully to that location and will assume control over the resource in question. Meanwhile, if a processor on the right side attempts to write a zero to the same semaphore flag it will fail, as will be verified by the fact that a one will be read from that semaphore on the right side during subsequent read. Had a sequence of READ/WRITE been used instead, system contention problems could have occurred during the gap between the read and write cycles.

It is important to note that a failed semaphore request must be followed by either repeated reads or by writing a one into the same location. The reason for this is easily understood by looking at the simple logic diagram of the semaphore flag in Figure 4. Two semaphore request latches feed into a semaphore flag. Whichever latch is first to present a zero to the semaphore flag will force its side of the semaphore flag LOW and the other side HIGH. This condition will continue until a one is written to the same semaphore request latch. Should the other side's semaphore request latch have been written to a zero in the meantime, the semaphore flag will flip over to the other side as soon as a one is written into the first side's request latch. The second side's flag will now stay LOW until its semaphore request latch is written to a one. From this it is easy to understand that, if a semaphore is requested and the processor which requested it no longer needs the resource, the entire system can hang up until a one is written into that semaphore request latch.



4851 drw 18

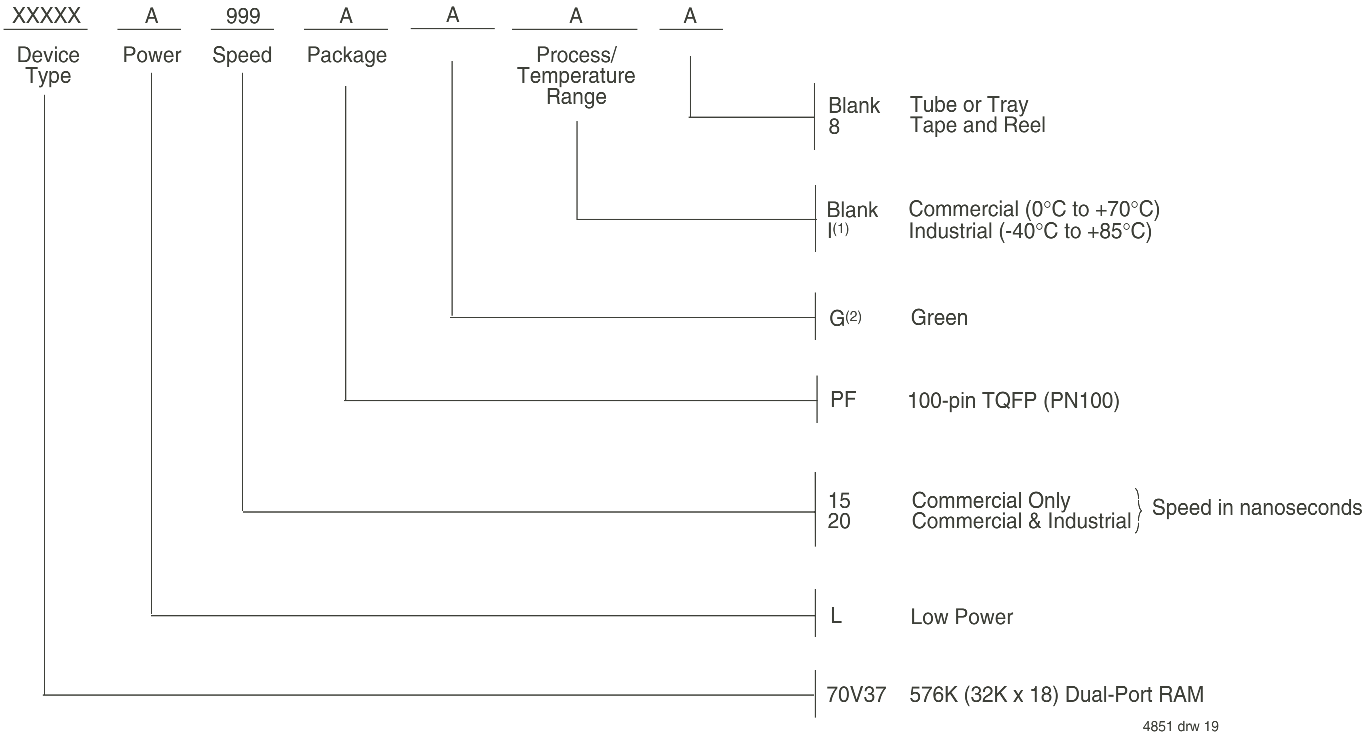
Figure 4. IDT70V37 Semaphore Logic

The critical case of semaphore timing is when both sides request a single token by attempting to write a zero into it at the same time. The semaphore logic is specially designed to resolve this problem. If simultaneous requests are made, the logic guarantees that only one side receives the token. If one side is earlier than the other in making the request, the first side to make the request will receive the token. If both requests arrive at the same time, the assignment will be arbitrarily made to one port or the other.

One caution that should be noted when using semaphores is that semaphores alone do not guarantee that access to a resource is secure. As with any powerful programming technique, if semaphores are misused or misinterpreted, a software error can easily happen.

Initialization of the semaphores is not automatic and must be handled via the initialization program at power-up. Since any semaphore request flag which contains a zero must be reset to a one, all semaphores on both sides should have a one written into them at initialization from both sides to assure that they will be free when needed.

Ordering Information



NOTES:
1. Contact your sales office for Industrial Temperature range in other speeds, packages and powers.
2. Green parts available. For specific speeds, packages and powers contact your sales office.

Datasheet Document History:

08/01/99:		Initial Public Offering
01/02/02:	Page 1 & 17	Replaced IDT logo
	Page 3	Increased storage temperature parameter
		Clarified T_A Parameter
	Page 5	DC Electrical parameters–changed wording from "open" to "disabled"
		Added Truth Table I - Chip Enable as note 5
		Corrected ±200mV to 0mV in notes
	Page 5, 7, 10 & 12	Added Industrial Temperature range for 20ns to DC & AC Electrical Characteristics
06/17/04 :		Removed Preliminary status
	Page 1 & 17	Replaced old ® logo with new TM logo
	Page 2	Added date revision to pin configuration
	Page 2 - 5	Changed naming conventions from V_{CC} to V_{DD} and from GND to V_{SS}
08/15/08:	Page 1	Added green availability to features
	Page 17	Added green indicator to ordering information
	Page 1 & 17	Updated old TM logo with new ® logo
01/19/09:	Page 17	Removed "IDT" from orderable part number
06/18/15:	Page 2	Removed IDT in reference to fabrication
	Page 2	Removed date from the 100-pin TQFP configuration
	Page 2 & 17	The package code PN100-1 changed to PN100 to match standard package codes
	Page 17	Added Tape & Reel indicator to the Ordering Information

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