



#### DMN601K

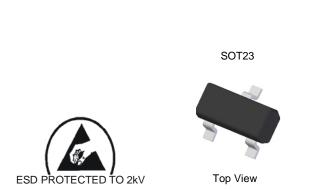
#### N-CHANNEL ENHANCEMENT MODE MOSFET

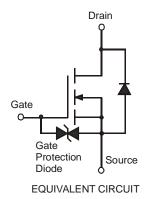
#### **Features**

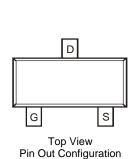
- Low On-Resistance: R<sub>DS(ON)</sub>
- Low Gate Threshold Voltage
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- ESD Protected Up To 2kV
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- Qualified to AEC-Q101 standards for High Reliability

#### **Mechanical Data**

- Case: SOT23
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish Matte Tin annealed over Alloy 42
   leadframe. Solderable per MIL-STD-202, Method 208 (©3)
- Terminal Connections: See Diagram
- Weight: 0.008 grams (approximate)







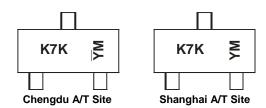
Ordering Information (Note 4)

Part Number	Case	Packaging
DMN601K-7	SOT23	3000/Tape & Reel

Notes:

- 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
- 2. See http://www.diodes.com/quality/lead\_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- 4. For packaging details, go to our website at http://www.diodes.com/products/packages.html.

# **Marking Information**



K7K = Product Type Marking Code

YM = Date Code Marking for SAT (Shanghai Assembly/ Test site)  $\overline{Y}M$  = Date Code Marking for CAT (Chengdu Assembly/ Test site)

Y or  $\overline{Y}$  = Year (ex: A = 2013)

M = Month (ex: 9 = September)

#### Date Code Key

Year	2005	2006	2007	2008	2009	2010	2011	2011	2012	2013	2014	2015	2016	2017
Code	S	Т	U	V	W	Х	Υ	Υ	Z	Α	В	С	D	Е
Month	Jan	Feb	Ma	ar A	Apr	May	Jun	Jul	Aug	Se	р (	Oct	Nov	Dec
Code	1	2	3	3	4	5	6	7	8	9		0	N	D



## **Maximum Ratings** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Units	
Drain-Source Voltage		$V_{DSS}$	60	٧
Gate-Source Voltage		V <sub>GSS</sub>	±20	V
Drain Current (Note 5)	Continuous Pulsed (Note 6)	la la	300 800	mA

## Thermal Characteristics (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Units
Total Power Dissipation (Note 5)	P <sub>D</sub>	350	mW
Thermal Resistance, Junction to Ambient	$R_{ heta JA}$	357	°C/W
Operating and Storage Temperature Range	T <sub>J,</sub> T <sub>STG</sub>	-65 to +150	°C

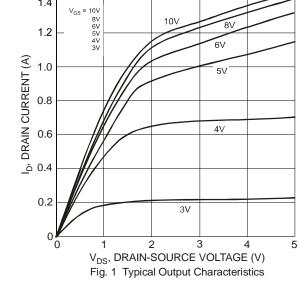
# Electrical Characteristics (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition	
OFF CHARACTERISTICS (Note 7)							
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	60	_	_	V	$V_{GS} = 0V, I_{D} = 10\mu A$	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	_	_	1.0	μA	$V_{DS} = 60V, V_{GS} = 0V$	
Gate-Source Leakage	I <sub>GSS</sub>	_	_	±10	μA	$V_{GS = \pm 20V}, V_{DS} = 0V$	
ON CHARACTERISTICS (Note 7)							
Gate Threshold Voltage	V <sub>GS(th)</sub>	1.0	1.6	2.5	<b>V</b>	$V_{DS} = 10V$ , $I_D = 1mA$	
Static Drain-Source On-Resistance	Б	_	_	2.0	Ω	$V_{GS} = 10V, I_D = 0.5A$	
Static Dialit-Source Off-Resistance	R <sub>DS(ON)</sub>	_	_	3.0		$V_{GS} = 5V, I_D = 0.05A$	
Forward Transfer Admittance	Y <sub>fs</sub>	80	_	_	ms	$V_{DS} = 10V, I_D = 0.2A$	
DYNAMIC CHARACTERISTICS							
Input Capacitance	C <sub>iss</sub>	_	_	50	pF		
Output Capacitance	Coss	_		25	pF	$V_{DS} = 25V, V_{GS} = 0V, f = 1.0MHz$	
Reverse Transfer Capacitance	C <sub>rss</sub>	_	_	5.0	pF		

Notes:

- 5. Device mounted on FR-4 PCB.
- 6. Pulse width ≤10μS, Duty Cycle ≤1%.
  7. Short duration pulse test used to minimize self-heating effect.





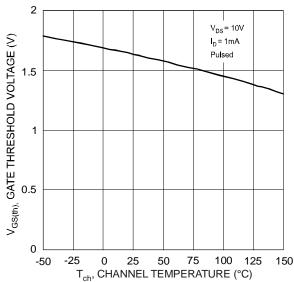


Fig. 3 Gate Threshold Voltage vs. Channel Temperature

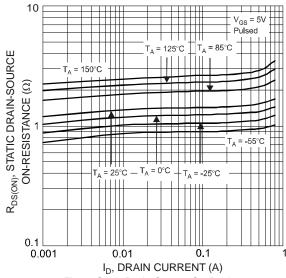
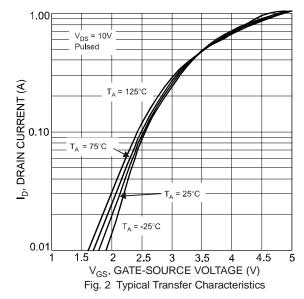


Fig. 5 Static Drain-Source On-Resistance vs. Drain Current



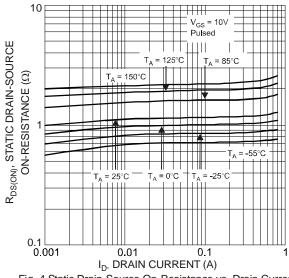


Fig. 4 Static Drain-Source On-Resistance vs. Drain Current

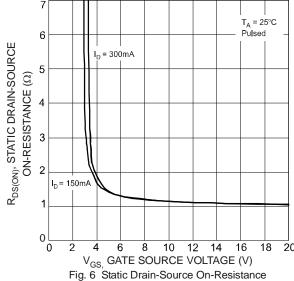
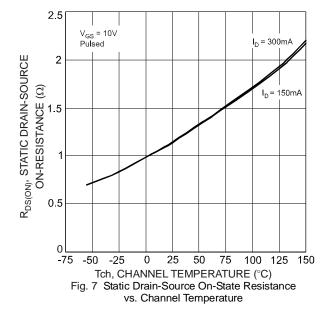
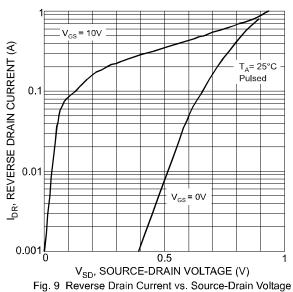
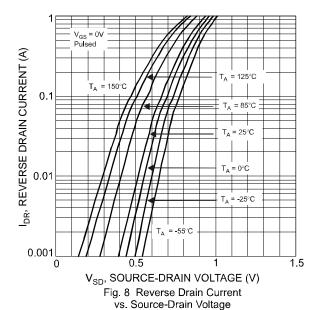


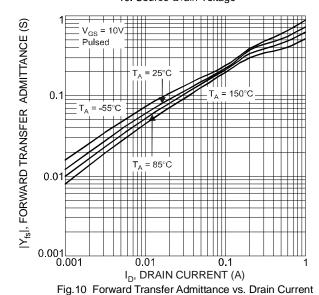
Fig. 6 Static Drain-Source On-Resistance vs. Gate-Source Voltage





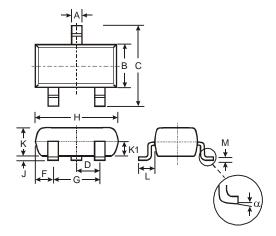






# **Package Outline Dimensions**

Please see AP02002 at http://www.diodes.com/datasheets/ap02002.pdf for latest version.



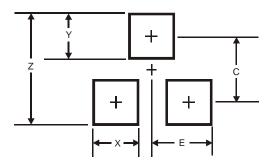
SOT23							
Dim	Min	Max	Тур				
Α	0.37	0.51	0.40				
В	1.20	1.40	1.30				
C	2.30	2.50	2.40				
D	0.89	1.03	0.915				
F	0.45	0.60	0.535				
G	1.78	2.05	1.83				
Н	2.80	3.00	2.90				
7	0.013	0.10	0.05				
K	0.903	1.10	1.00				
K1	-	-	0.400				
L	0.45	0.61	0.55				
M	0.085	0.18	0.11				
α	0°	8°	-				
All Dimensions in mm							

August 2013



### **Suggested Pad Layout**

Please see AP02001 at http://www.diodes.com/datasheets/ap02001.pdf for the latest version.



Dimensions	Value (in mm)
Z	2.9
Х	0.8
Υ	0.9
С	2.0
E	1.35

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