NTY100N10

Preferred Device

Power MOSFET 123 A, 100 V N-Channel Enhancement-Mode TO264 Package

ON Semiconductor®

http://onsemi.com

123 A, 100 V
9 mΩ @ V_{GS} = 10 V (Typ)

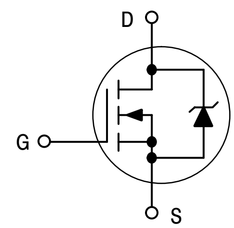
Features

- Source−to−Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Avalanche Energy Specified
- IDSS and $R_{DS(on)}$ Specified at Elevated Temperature
- Pb−Free Package is Available*

Applications

- PWM Motor Control
- Power Supplies
- Converters

N−Channel



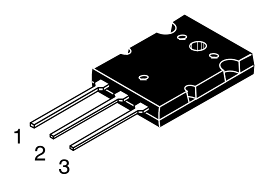
MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain−Source Voltage	V_{DSS}	100	V
Drain−Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	100	V
Gate−Source Voltage − Continuous − Non−Repetitive (t_p ≤ 10 ms)	V_{GS} V_{GSM}	± 20 ± 40	V V
Drain Current (Note 1) − Continuous @ T_C = 25°C − Pulsed	I_D I_{DM}	123 369	A A
Total Power Dissipation (Note 1) Derate above 25°C	P_D	313 2.5	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to 150	°C
Single Pulse Drain−to−Source Avalanche Energy − Starting T_J = 25°C (V_{DD} = 80 Vdc, V_{GS} = 10 Vdc, Peak I_L = 100 Apk, L = 0.1 mH, R_G = 25 Ω)	E_{AS}	500	mJ
Thermal Resistance − Junction to Case − Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	0.4 25	°C/W
Maximum Lead Temperature for Soldering Purposes, 0.125 in from case for 10 seconds	T_L	260	°C

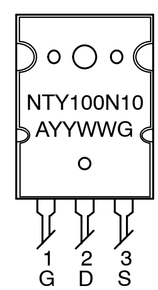
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Pulse Test: Pulse Width = 10 μs, Duty−Cycle = 2%.

MARKING DIAGRAM & PIN ASSIGNMENT



TO−264
CASE 340G
STYLE 1



A = Assembly Location
YY = Year
WW = Work Week
G = Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping
NTY100N10	TO−264	25 Units/Rail
NTY100N10G	TO−264 (Pb−Free)	25 Units/Rail

Preferred devices are recommended choices for future use and best overall value.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

March, 2006 − Rev. 2
Publication Order Number:
NTY100N10/D

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain−Source Breakdown Voltage (V_{GS} = 0, I_D = 250 μA) (Positive Temperature Coefficient)		$V_{(BR)DSS}$	 100 –	 – 144	 – –	 Vdc mV/°C
Zero Gate Voltage Drain Current (V_{GS} = 0 Vdc, V_{DS} = 100 Vdc, T_J = 25°C) (V_{GS} = 0 Vdc, V_{DS} = 100 Vdc, T_J = 150°C)		I_{DSS}	 – –	 – –	 10 100	μAdc
Gate−Body Leakage Current (V_{GS} = ±20 Vdc, V_{DS} = 0)		I_{GSS}	–	–	 100	nAdc
ON CHARACTERISTICS (Note 2)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc) (Negative Temperature Coefficient)		$V_{GS(th)}$	 2.0 –	 3.1 10.6	 4.0 –	 Vdc mV/°C
Static Drain−Source On−State Resistance (V_{GS} = 10 Vdc, I_D = 50 Adc) (V_{GS} = 10 Vdc, I_D = 50 Adc, 150°C)		$R_{DS(on)}$	 – –	 0.009 0.019	 0.010 0.021	Ω
Drain−Source On−Voltage (V_{GS} = 10 Vdc, I_D = 100 Adc)		$V_{DS(on)}$	–	0.8	1.0	Vdc
Forward Transconductance (V_{DS} = 6 Vdc, I_D = 50 Adc)		g_{FS}	–	73	–	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1 MHz)	C_{iss}	–	7225	10110	pF
Output Capacitance		C_{oss}	–	1800	2540	
Reverse Transfer Capacitance		C_{rss}	–	270	540	
SWITCHING CHARACTERISTICS (Notes 2, 3)						
Turn−On Delay Time	(V_{DD} = 50 Vdc, I_D = 100 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	–	30	55	ns
Rise Time		t_r	–	150	265	
Turn−Off Delay Time		$t_{d(off)}$	–	340	595	
Fall Time		t_f	–	250	435	
Total Gate Charge	(V_{DS} = 80 Vdc, I_D = 100 Adc, V_{GS} = 10 Vdc)	Q_T	–	200	350	nC
Gate−Source Charge		Q_1	–	40	–	
		Q_2	–	100	–	
		Q_3	–	86	–	
BODY−DRAIN DIODE RATINGS (Note 2)						
Forward On−Voltage (I_S = 100 Adc, V_{GS} = 0 Vdc) (I_S = 100 Adc, V_{GS} = 0 Vdc, T_J = 150°C)		V_{SD}	 – –	 1.02 0.94	 1.1 –	Vdc
Reverse Recovery Time (I_S = 100 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)		t_{rr}	–	210	–	ns
		t_a	–	155	–	
		t_b	–	55	–	
Reverse Recovery Stored Charge		Q_{RR}	–	1.08	–	μC

2. Indicates Pulse Test: Pulse Width ≤300 μs max, Duty Cycle = 2%.
3. Switching characteristics are independent of operating junction temperature.

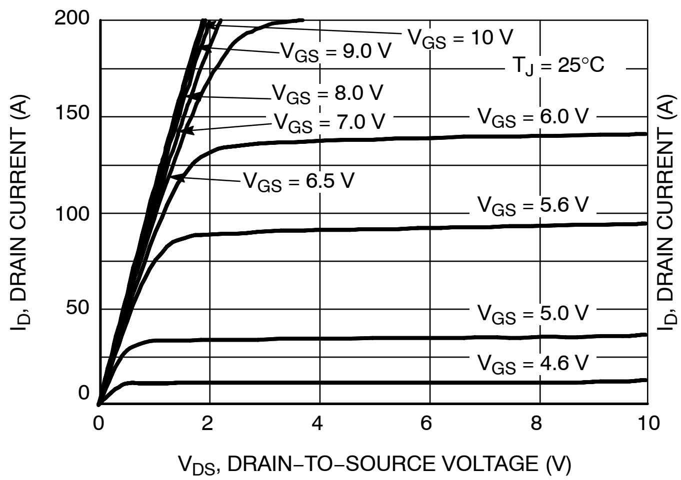


Figure 1. On−Region Characteristics

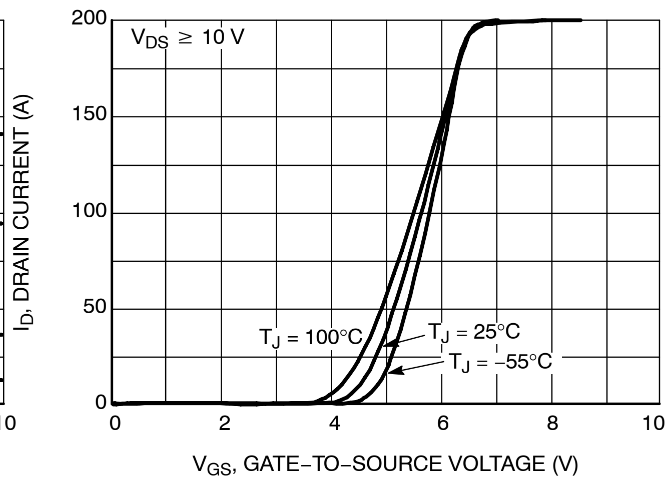


Figure 2. On−Region Characteristics

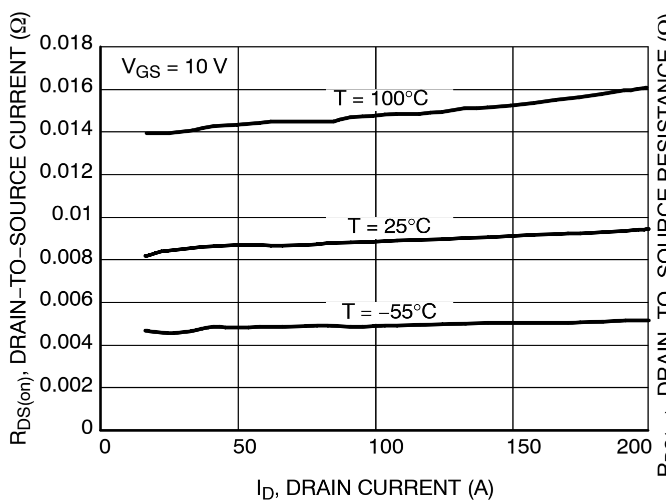


Figure 3. On−Resistance versus Drain Current and Temperature

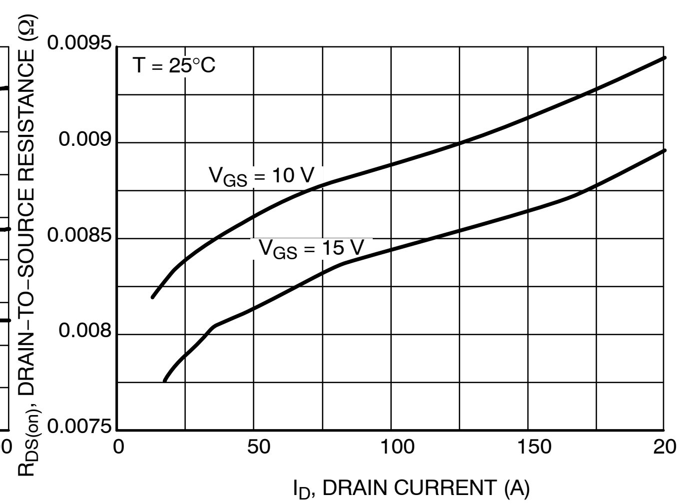


Figure 4. On−Resistance versus Drain Current and Gate Voltage

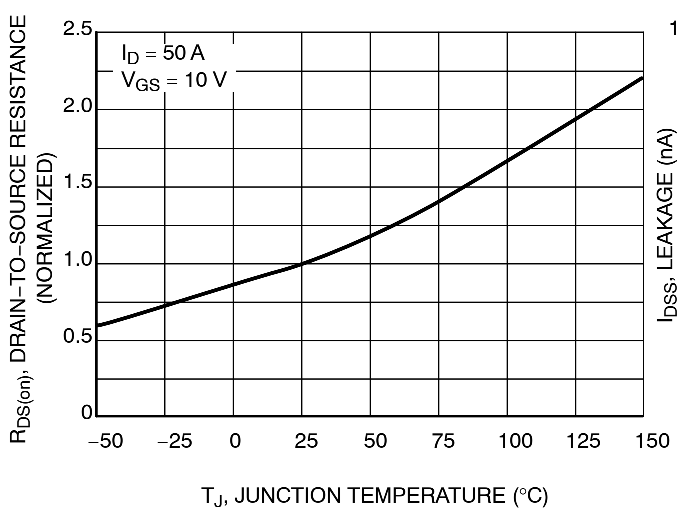


Figure 5. On−Resistance Variation with Temperature

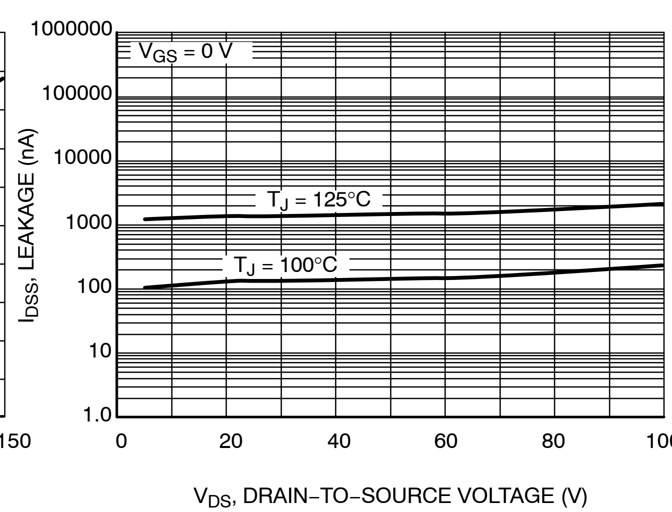


Figure 6. Drain−to−Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain−gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn−on and turn−off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\ C_{iss}\ \text{In}\ [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G\ C_{iss}\ \text{In}\ (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off−state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on−state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

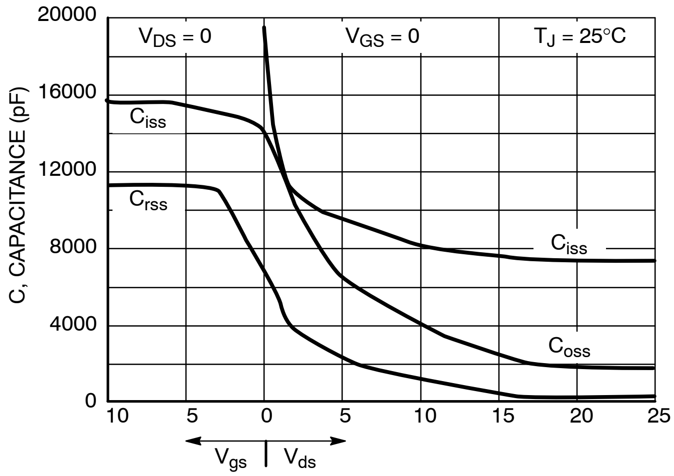


Figure 7. Capacitance Variation

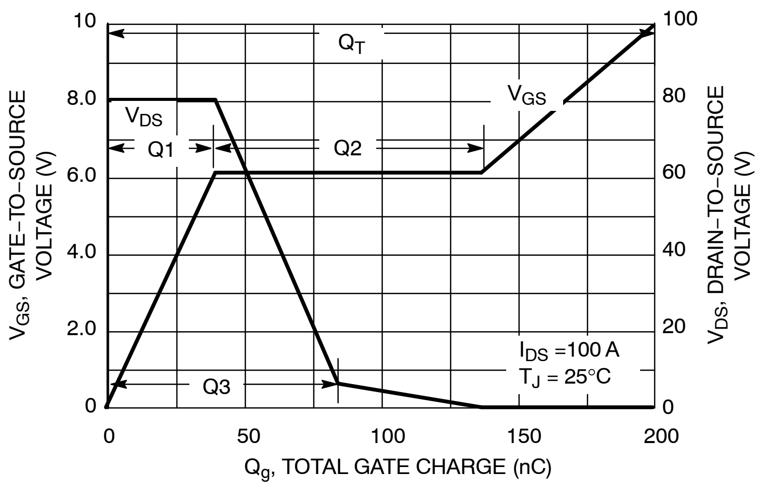


Figure 8. Gate−to−Source and Drain−to−Source Voltage versus Total Charge

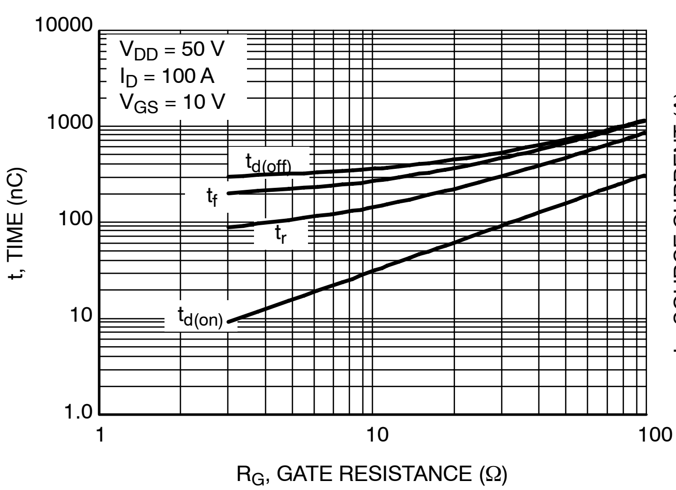


Figure 9. Resistive Switching Time Variation versus Gate Resistance

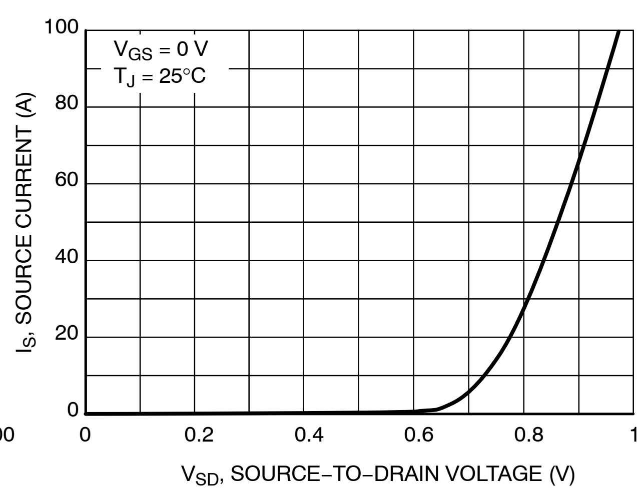


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain−to−source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, "Transient Thermal Resistance−General Data and Its Use."

Switching between the off−state and the on−state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A Power MOSFET designated E−FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non−linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E−FETs can withstand the stress of drain−to−source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

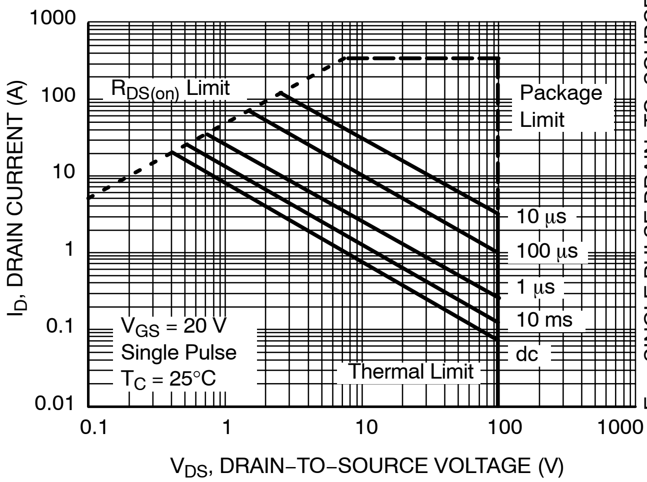


Figure 11. Maximum Rated Forward Bias Safe Operating Area

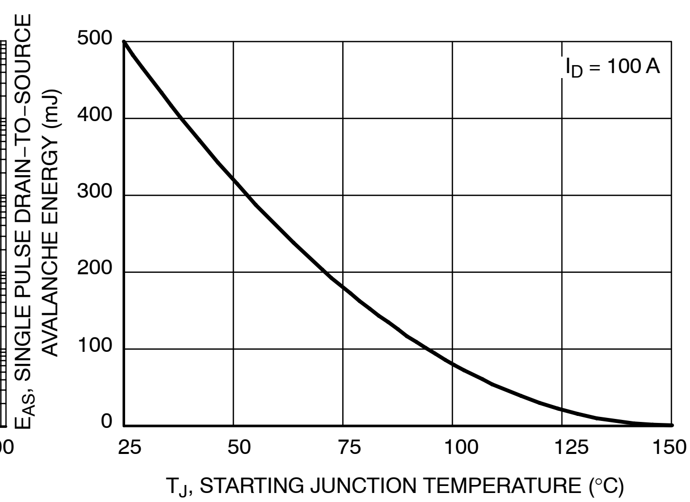


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

SAFE OPERATING AREA

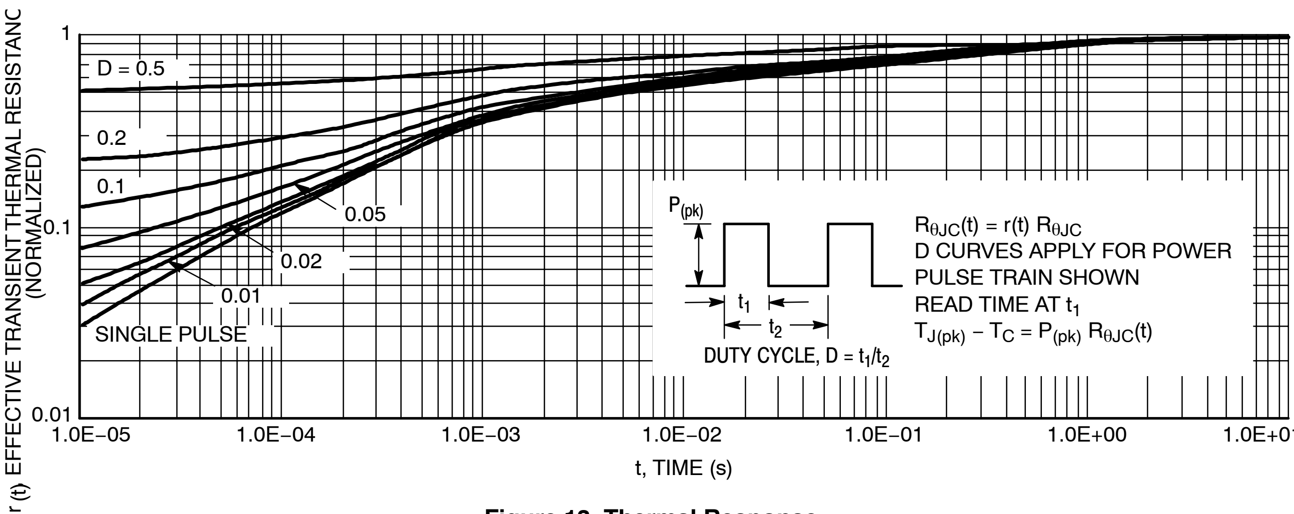


Figure 13. Thermal Response

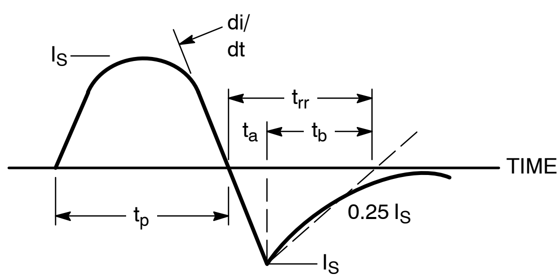
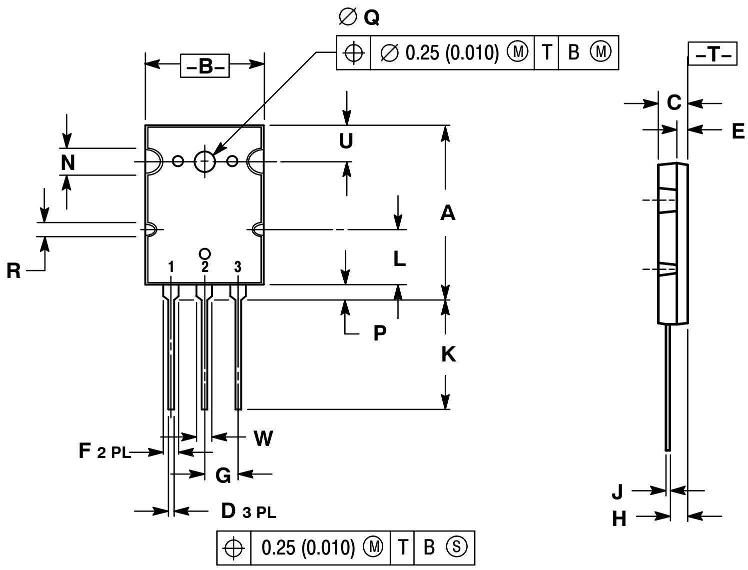


Figure 14. Diode Reverse Recovery Waveform

PACKAGE DIMENSIONS

TO−3BPL (TO−264)
CASE 340G−02
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS		INCHES	
DIM	**MIN**	**MAX**	**MIN**	**MAX**
A	28.0	29.0	1.102	1.142
B	19.3	20.3	0.760	0.800
C	4.7	5.3	0.185	0.209
D	0.93	1.48	0.037	0.058
E	1.9	2.1	0.075	0.083
F	2.2	2.4	0.087	0.102
G	5.45 BSC		0.215 BSC	
H	2.6	3.0	0.102	0.118
J	0.43	0.78	0.017	0.031
K	17.6	18.8	0.693	0.740
L	11.2 REF		0.411 REF	
N	4.35 REF		0.172 REF	
P	2.2	2.6	0.087	0.102
Q	3.1	3.5	0.122	0.137
R	2.25 REF		0.089 REF	
U	6.3 REF		0.248 REF	
W	2.8	3.2	0.110	0.125

STYLE 1:
PIN 1. GATE
2. DRAIN
3. SOURCE

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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