

IP4773CZ14

VGA Interface with integrated buffer, ESD protection and termination resistor

Rev. 01 — 24 February 2009

Product data sheet

1. General description

The IP4773CZ14 is a VGA or DVI-I interface intended to be connected between a video transmitter such as a PC graphics card and a VGA or DVI-I receiver, such as a PC monitor. The IP4773CZ14 has ESD protection for the DDC lines, ESD protection plus buffering for the h-sync and v-sync lines and high-level ESD protection diodes for the R, G, B video signal lines.

The synchronizing signals are buffered by non-inverting buffers which can accept TTL-level input. The buffers convert TTL-level input to CMOS-level output which swings between $V_{CC(SYNC)}$ and GND.

An external termination resistor can be added to achieve the desired termination, which is typically required for the h-sync and v-sync lines of the video interface.

The IP4773CZ14 has a typical output resistance (R_O) of 10 Ω .

2. Features

- Integrated high-level ESD protection, buffering, sync-signal impedance matching
- All pin connections have integrated rail-to-rail clamping diodes providing downstream ESD protection of ± 8 kV according to IEC 61000-4-2, level 4
- Drivers for h-sync and v-sync lines
- Line capacitance < 4 pF per channel

3. Applications

Buffer and terminating channels, reduce EMI and RFI, and provide downstream ESD protection for:

- VGA interfaces including DDC channels
- Desktop and notebook PCs, LCD TVs and PC monitors
- Graphics cards
- Set-top boxes
- Game consoles
- DVD players

4. Ordering information

Table 1. Ordering information

Type number	Package		Version
	Name	Description	
IP4773CZ14	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1

5. Functional diagram

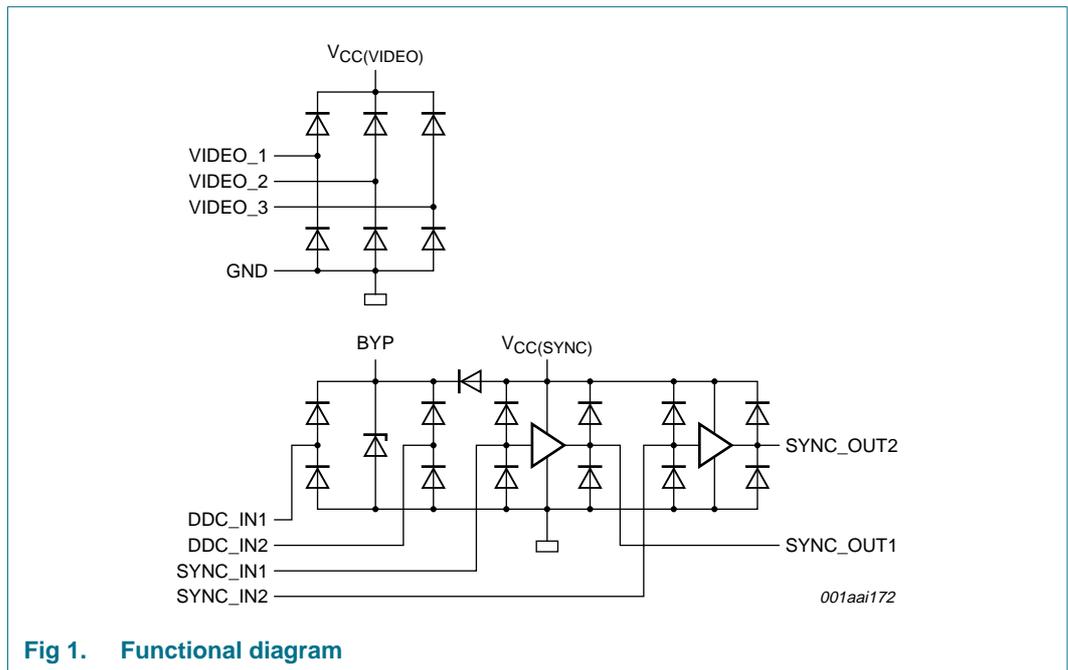


Fig 1. Functional diagram

6. Pinning information

6.1 Pinning

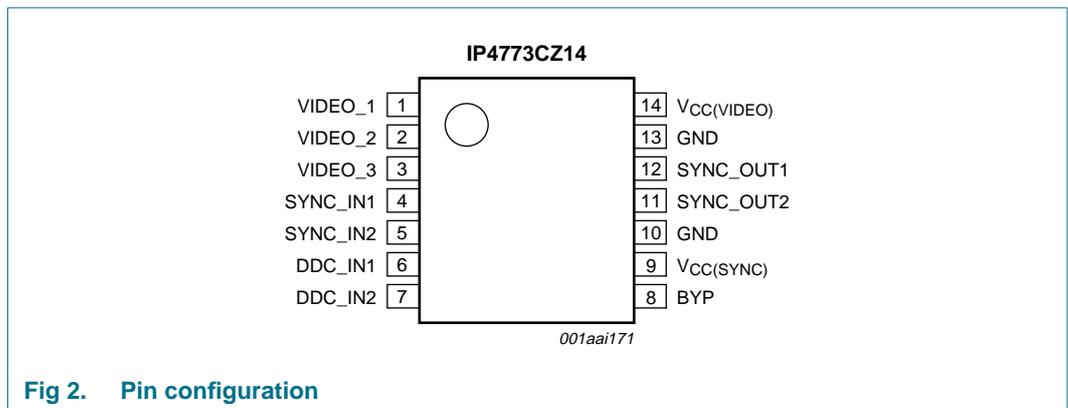


Fig 2. Pin configuration

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
VIDEO_1	1	ESD protection for video channel 1
VIDEO_2	2	ESD protection for video channel 2
VIDEO_3	3	ESD protection for video channel 3
SYNC_IN1	4	sync signal input 1
SYNC_IN2	5	sync signal input 2
DDC_IN1	6	DDC signal input 1
DDC_IN2	7	DDC signal input 2
BYP	8	for connecting a 100 nF bypass capacitor to increase ESD clamping performance of the DDC outputs
V _{CC(SYNC)}	9	supply voltage for sync buffer
GND	10	ground
SYNC_OUT2	11	sync signal output 2
SYNC_OUT1	12	sync signal output 1
GND	13	ground
V _{CC(VIDEO)}	14	supply voltage for video protection circuit

7. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC(VIDEO)}	video supply voltage		GND – 0.5	5.5	V
V _{CC(SYNC)}	synchronization supply voltage		3.0	5.5	V
V _I	input voltage	pins VIDEO_1, VIDEO_2, VIDEO_3	GND – 0.5	V _{CC(VIDEO)}	V
		pins SYNC_IN1, SYNC_IN2, DDC_IN1, DDC_IN2	GND – 0.5	V _{CC(SYNC)}	V
V _{ESD}	electrostatic discharge voltage	IEC 61000-4-2, level 4, contact	[1] –8	+8	kV
P _{tot}	total power dissipation	T _{amb} = 25 °C; f _{sync} = 100 kHz, C _L = 6 nF, R _L = 10 kΩ	-	50	mW
T _{stg}	storage temperature		–55	+125	°C

- [1] Pins BYP, V_{CC(VIDEO)} and V_{CC(SYNC)} must be bypassed to GND via a low-impedance ground plane with 100 nF, low inductance, chip ceramic capacitor at each supply pin. ESD pulse is applied between pins (VIDEO_1, VIDEO_2, VIDEO_3, SYNC_OUT1, SYNC_OUT2) and GND.

8. Characteristics

Table 4. Characteristics
T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Analog video (RGB)						
I _{CC(VIDEO)}	supply current on pin V _{CC(VIDEO)}	V _{CC(VIDEO)} = 5.0 V; static input signals	-	-	10	μA
C _{ch}	channel capacitance	V _{CC(VIDEO)} = 5.0 V; f = 1 MHz; V _I = 2.5 V (p-p); V _{bias} = 2.5 V	[1]	-	4	pF
I _I	input current	V _{CC(VIDEO)} = 5.0 V; V _I = V _{CC(VIDEO)} or GND	-	-	±1	μA
V _{Fd}	diode forward voltage	I _F = 1 mA	-	0.7	-	V
DDC						
C _{ch}	channel capacitance	f = 1 MHz; V _I = 2.5 V (p-p); V _{bias} = 2.5 V	[1]	-	4	pF
I _I	input current	V _I = 5.0 V	-	-	±1	μA
V _{Fd}	diode forward voltage	I _F = 1 mA	-	0.7	-	V
Sync buffer						
V _{CC(SYNC)}	synchronization supply voltage		3.0	5.0	5.5	V
I _{CC(SYNC)}	supply current on pin V _{CC(SYNC)}	V _{CC(SYNC)} = 5.0 V; static input signals	[2]	-	10	μA
C _{ch}	channel capacitance	V _{CC(SYNC)} = 5.0 V; f = 1 MHz; V _{bias} = 1.65 V	[1]	-	4	pF
I _I	input current	V _{CC(SYNC)} = 5.0 V; V _I = V _{CC(SYNC)} or GND	-	-	±1	μA
V _{Fd}	diode forward voltage	I _F = 1 mA	-	0.7	-	V
V _{IH}	HIGH-level input voltage	V _{CC(SYNC)} = 5.0 V	[3]	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC(SYNC)} = 5.0 V	[3]	-	0.6	V
V _{OH}	HIGH-level output voltage	V _{CC(SYNC)} = 5.0 V; I _{OH} = 24 mA	[3]	2.0	-	V
V _{OL}	LOW-level output voltage	V _{CC(SYNC)} = 5.0 V; I _{OL} = 24 mA	[3]	-	0.8	V
R _O	output resistance		[3]	-	10	Ω
t _{PLH}	LOW to HIGH propagation delay	V _{CC(SYNC)} = 5.0 V; C _L = 50 pF; t _{r(i)} and t _{f(i)} ≤ 5 ns	[1]	-	12	ns
t _{PHL}	HIGH to LOW propagation delay	V _{CC(SYNC)} = 5.0 V; C _L = 50 pF; t _{r(i)} and t _{f(i)} ≤ 5 ns	[1]	-	12	ns
t _{r(o)}	output rise time	V _{CC(SYNC)} = 5.0 V; C _L = 50 pF; t _{r(i)} and t _{f(i)} ≤ 5 ns	-	4	-	ns
t _{f(o)}	output fall time	V _{CC(SYNC)} = 5.0 V; C _L = 50 pF; t _{r(i)} and t _{f(i)} ≤ 5 ns	-	4	-	ns

[1] Guaranteed by design and characterization.

[2] Sync buffer outputs unloaded.

[3] Applies only to the Sync buffer; note that R_O = R_{buffer}.

9. Application information

9.1 Connections

The IP4773CZ14 should be placed as close as possible to the VGA or DVI-I interface connector. The ESD-protected channels on pins VIDEO_1, VIDEO_2 and VIDEO_3 can be connected in any order to R, G, B signals. The sync buffers are equivalent and can be connected to either h-sync or v-sync signals.

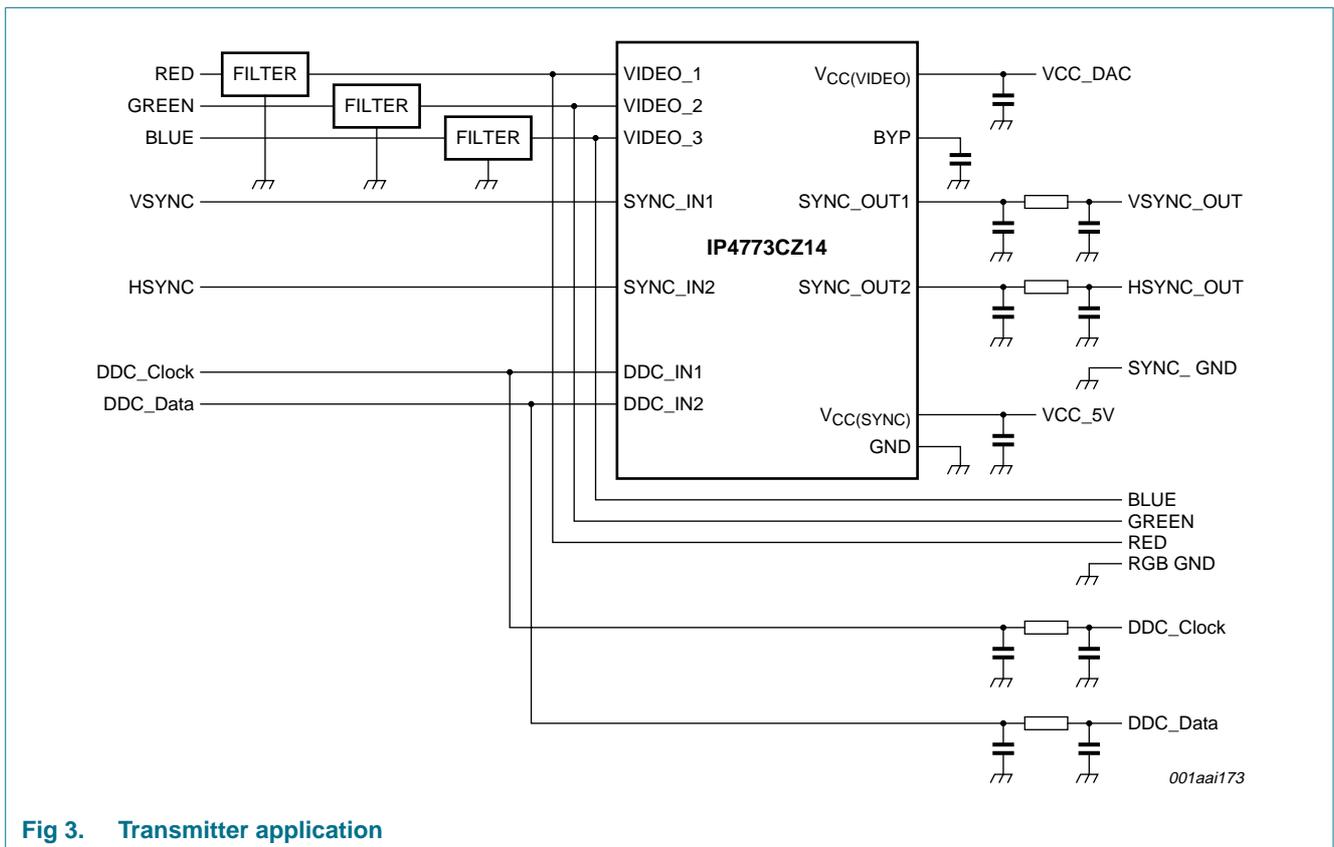


Fig 3. Transmitter application

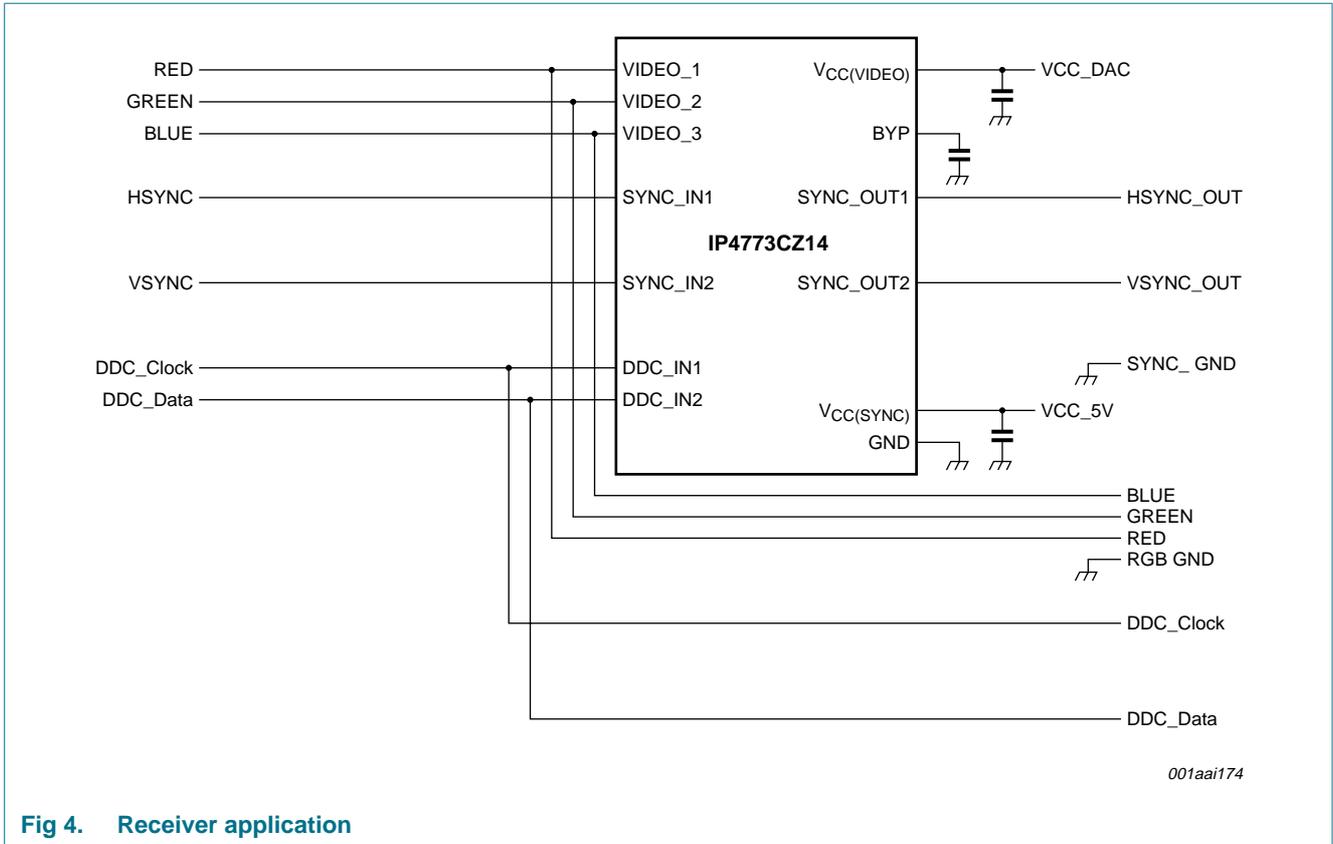


Fig 4. Receiver application

The receiver application simplifies VGA input circuit applications.

10. Package outline

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1

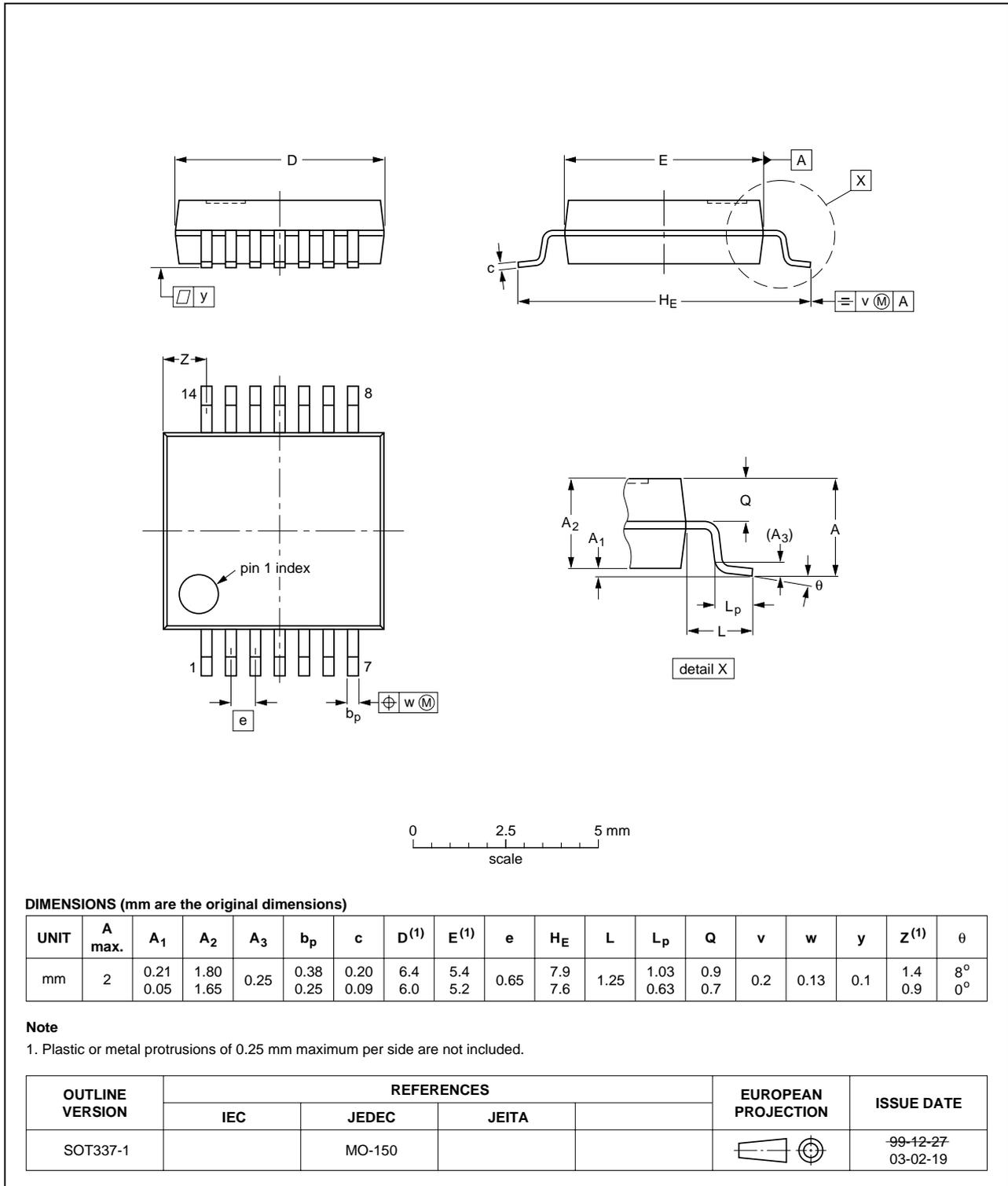


Fig 5. Package outline SOT337-1 (SSOP14)

11. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

11.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

11.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

11.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

11.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 6](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 5](#) and [6](#)

Table 5. SnPb eutectic process (from J-STD-020C)

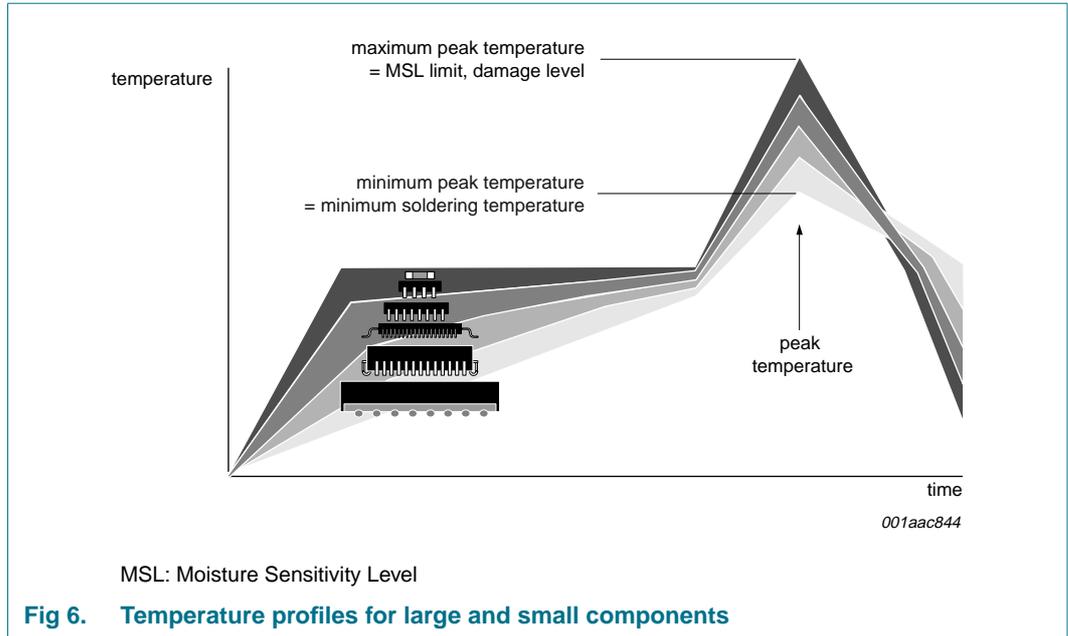
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm ³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 6. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm ³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 6](#).



For further information on temperature profiles, refer to Application Note AN10365 “Surface mount reflow soldering description”.

12. Abbreviations

Table 7. Abbreviations

Acronym	Description
DDC	Display Data Channel
DVI-I	Digital Visual Interface Integrated (Analog and Digital)
EMI	ElectroMagnetic Interference
ESD	ElectroStatic Discharge
RGB	Red, Green, Blue
RFI	Radio Frequency Interference
TTL	Transistor-Transistor Logic
VGA	Video Graphics Array

13. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
IP4773CZ14_1	20090224	Product data sheet	-	-

14. Legal information

14.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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