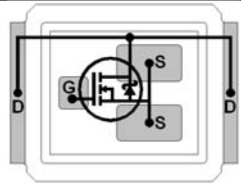
International Rectifier

IRF6609

HEXFET® Power MOSFET

V_{DSS}	$R_{DS(on)}$ max	Qg
20V	2.0mΩ@V_{GS} = 10V	46nC
	2.6mΩ@V_{GS} = 4.5V	

- Low Conduction Losses
- Low Switching Losses
- Ideal Synchronous Rectifier MOSFET
- Low Profile (<0.7 mm)
- Dual Sided Cooling Compatible
- Compatible with existing Surface Mount Techniques



MT


DirectFET™ ISOMETRIC

Applicable DirectFET Outline and Substrate Outline (see p.8,9 for details)

SQ	SX	ST		MQ	MX	MT				

Description

The IRF6609 combines the latest HEXFET® Power MOSFET Silicon technology with the advanced DirectFET™ packaging to achieve the lowest on-state resistance in a package that has the footprint of an SO-8 and only 0.7 mm profile. The DirectFET package is compatible with existing layout geometries used in power applications, PCB assembly equipment and vapor phase, infra-red or convection soldering techniques, when application note AN-1035 is followed regarding the manufacturing methods and processes. The DirectFET package allows dual sided cooling to maximize thermal transfer in power systems, IMPROVING previous best thermal resistance by 80%.

The IRF6609 balances both low resistance and low charge along with ultra low package inductance to reduce both conduction and switching losses. The reduced total losses make this product ideal for high efficiency DC-DC converters that power the latest generation of processors operating at higher frequencies. The IRF6609 has been optimized for parameters that are critical in synchronous buck operating from 12 volt buss converters including Rds(on), gate charge and Cdv/dt-induced turn on immunity. The IRF6609 offers particularly low Rds(on) and high Cdv/dt immunity for synchronous FET applications.

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{DS}	Drain-to-Source Voltage	20	V
V_{GS}	Gate-to-Source Voltage	±20	
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V ⑦	150	A
I_D @ T_A = 25°C	Continuous Drain Current, V_{GS} @ 10V ④	31	
I_D @ T_A = 70°C	Continuous Drain Current, V_{GS} @ 10V ④	25	
I_{DM}	Pulsed Drain Current ①	250	
P_D @T_C = 25°C	Power Dissipation ⑦	89	W
P_D @T_A = 25°C	Power Dissipation ④	1.8	
P_D @T_A = 70°C	Power Dissipation ④	2.8	
	Linear Derating Factor	0.022	W/°C
T_J T_{STG}	Operating Junction and Storage Temperature Range	-40 to + 150	°C

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JA}$	Junction-to-Ambient ④⑧	–––	45	°C/W
$R_{\theta JA}$	Junction-to-Ambient ⑤⑧	12.5	–––	
$R_{\theta JA}$	Junction-to-Ambient ⑥⑧	20	–––	
$R_{\theta JC}$	Junction-to-Case ⑦⑧	–––	1.4	
$R_{\theta J\text{-}PCB}$	Junction-to-PCB Mounted	1.0	–––	

Notes ① through ⑧ are on page 10

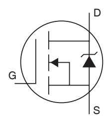
Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	20	—	—	V	V_{GS} = 0V, I_D = 250μA
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	15	—	mV/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	1.6	2.0	mΩ	V_{GS} = 10V, I_D = 31A ③
		—	2.0	2.6		V_{GS} = 4.5V, I_D = 25A ③
$V_{GS(th)}$	Gate Threshold Voltage	1.55	—	2.45	V	V_{DS} = V_{GS}, I_D = 250μA
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	-6.1	—	mV/°C	
I_{DSS}	Drain-to-Source Leakage Current	—	—	1.0	μA	V_{DS} = 16V, V_{GS} = 0V
		—	—	150		V_{DS} = 16V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS} = -20V
gfs	Forward Transconductance	91	—	—	S	V_{DS} = 10V, I_D = 25A
Q_g	Total Gate Charge	—	46	69		
Q_{gs1}	Pre-Vth Gate-to-Source Charge	—	15	—		V_{DS} = 10V
Q_{gs2}	Post-Vth Gate-to-Source Charge	—	4.7	—	nC	V_{GS} = 4.5V
Q_{gd}	Gate-to-Drain Charge	—	15	—		I_D = 17A
Q_{godr}	Gate Charge Overdrive	—	11	—		See Fig. 16
Q_{sw}	Switch Charge (Q_{gs2} + Q_{gd})	—	20	—		
Q_{oss}	Output Charge	—	26	—	nC	V_{DS} = 10V, V_{GS} = 0V
$t_{d(on)}$	Turn-On Delay Time	—	24	—		V_{DD} = 16V, V_{GS} = 4.5V ③
t_r	Rise Time	—	95	—		I_D = 25A
$t_{d(off)}$	Turn-Off Delay Time	—	26	—	ns	Clamped Inductive Load
t_f	Fall Time	—	9.8	—		
C_{iss}	Input Capacitance	—	6290	—		V_{GS} = 0V
C_{oss}	Output Capacitance	—	1850	—	pF	V_{DS} = 10V
C_{rss}	Reverse Transfer Capacitance	—	860	—		f = 1.0MHz

Avalanche Characteristics

	Parameter	Typ.	Max.	Units
$E_{AS\ (Thermally\ limited)}$	Single Pulse Avalanche Energy ②	—	240	mJ
I_{AR}	Avalanche Current ①	—	See Fig. 12, 13, 18a, 18b,	A
E_{AR}	Repetitive Avalanche Energy ①	—		mJ

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	89	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	250		
V_{SD}	Diode Forward Voltage	—	0.80	1.2	V	T_J = 25°C, I_S = 25A, V_{GS} = 0V ③
t_{rr}	Reverse Recovery Time	—	32	48	ns	T_J = 25°C, I_F = 25A
Q_{rr}	Reverse Recovery Charge	—	26	39	nC	di/dt = 100A/μs ③

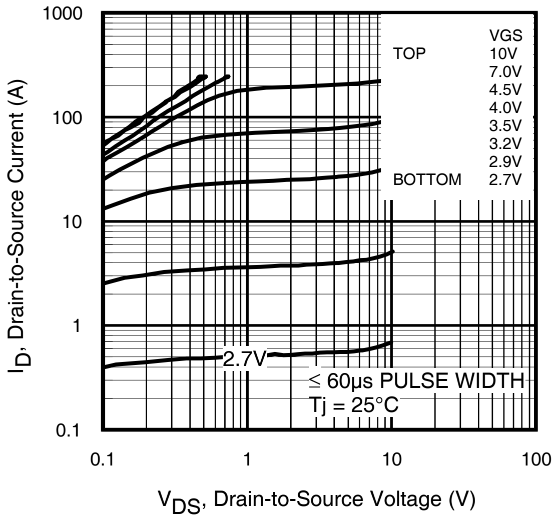


Fig 1. Typical Output Characteristics

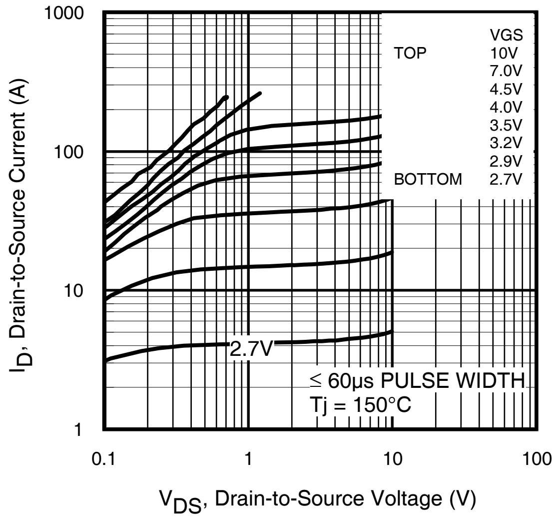


Fig 2. Typical Output Characteristics

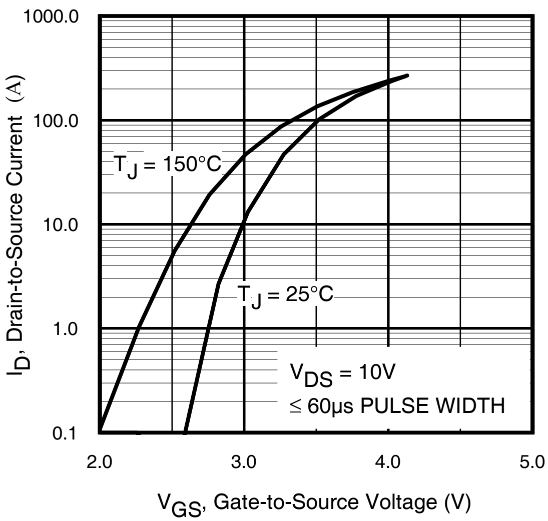


Fig 3. Typical Transfer Characteristics

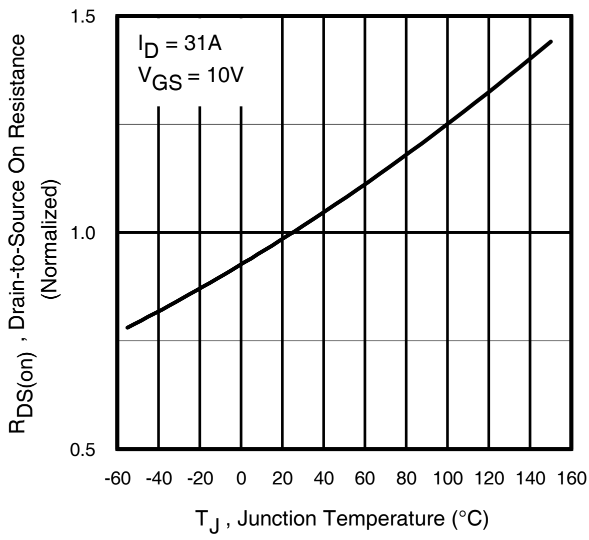


Fig 4. Normalized On-Resistance vs. Temperature

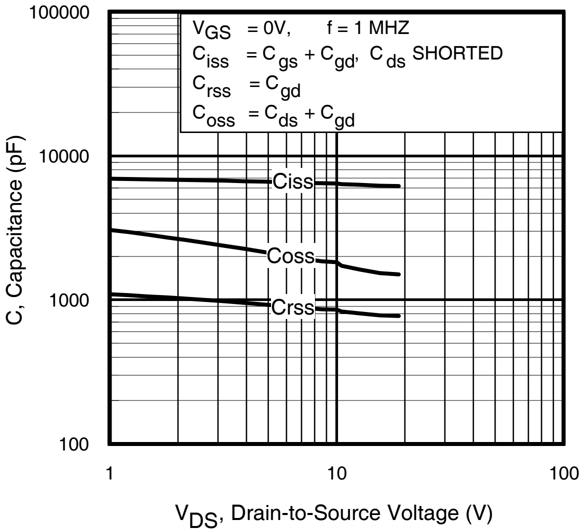


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

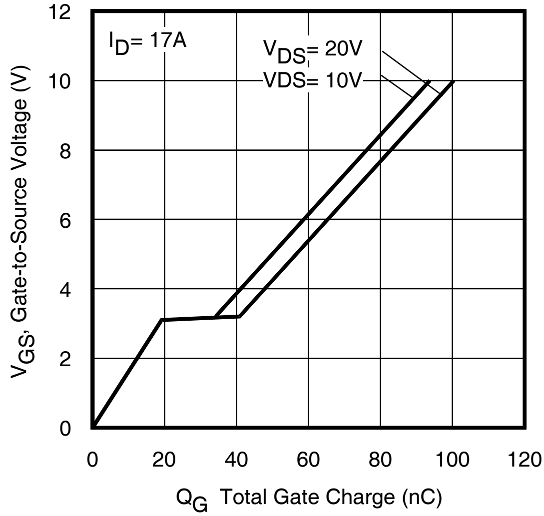


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

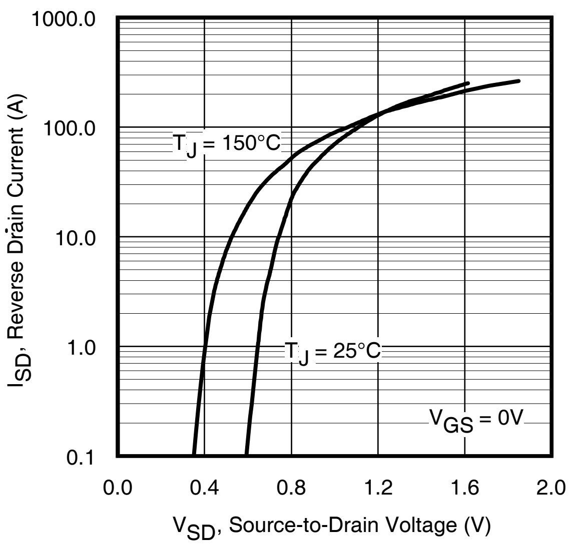


Fig 7. Typical Source-Drain Diode Forward Voltage

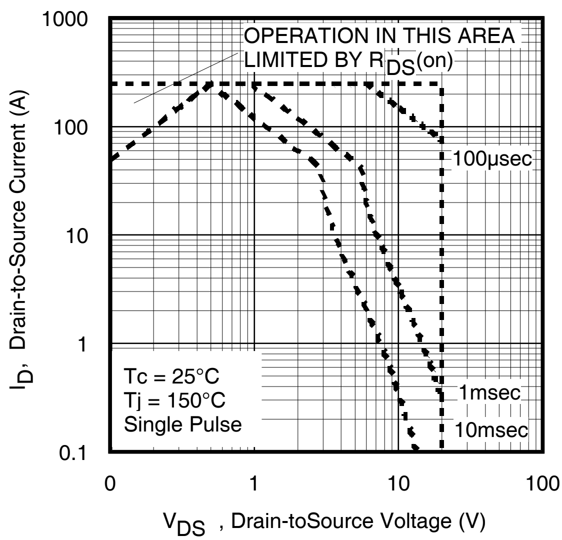


Fig 8. Maximum Safe Operating Area

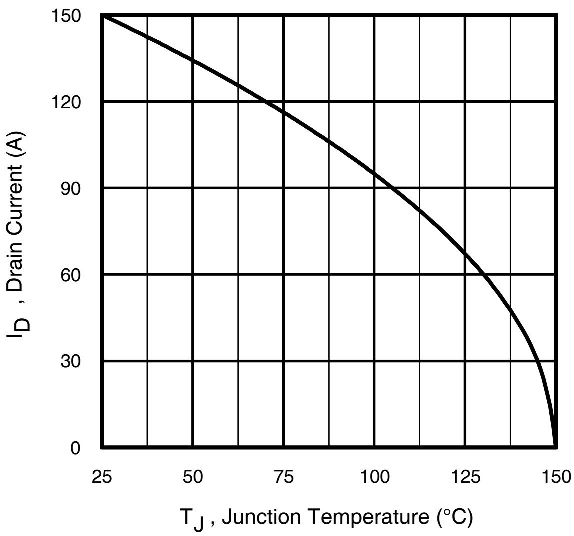


Fig 9. Maximum Drain Current vs. Case Temperature

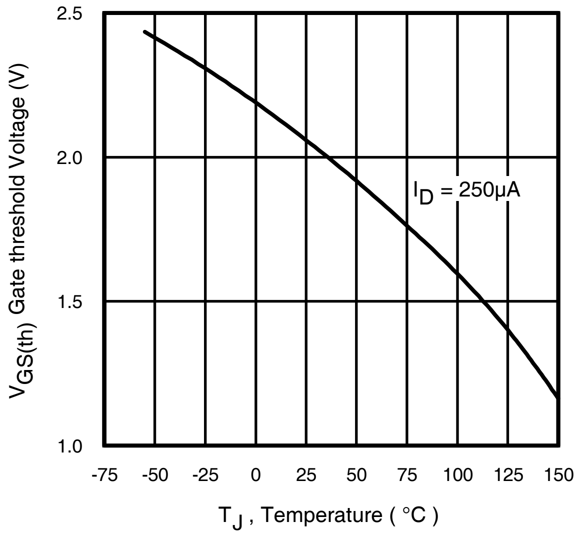
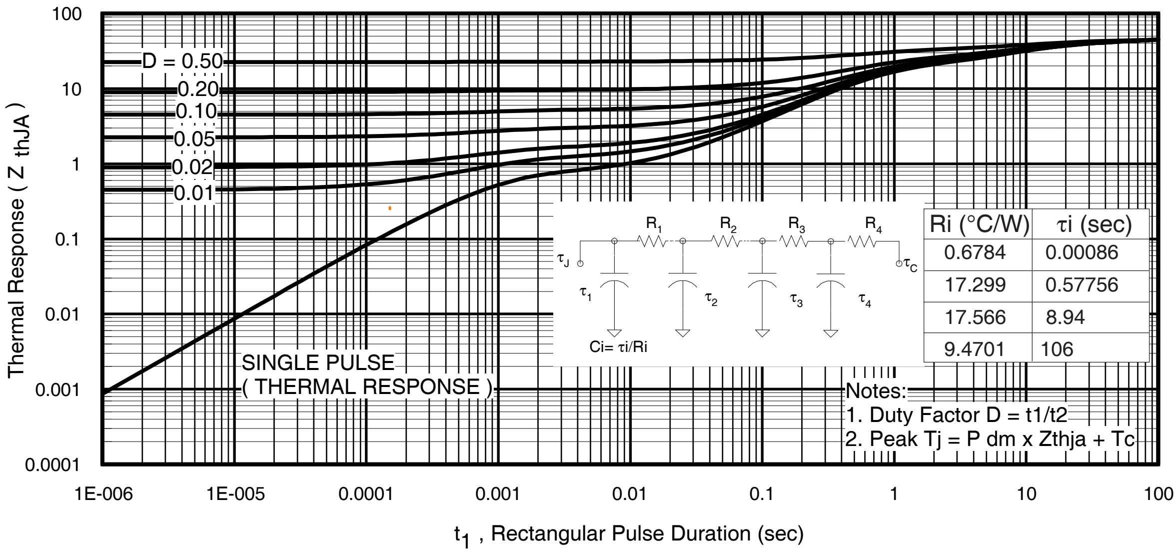


Fig 10. Threshold Voltage vs. Temperature



Ri (°C/W)	τi (sec)
0.6784	0.00086
17.299	0.57756
17.566	8.94
9.4701	106

Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

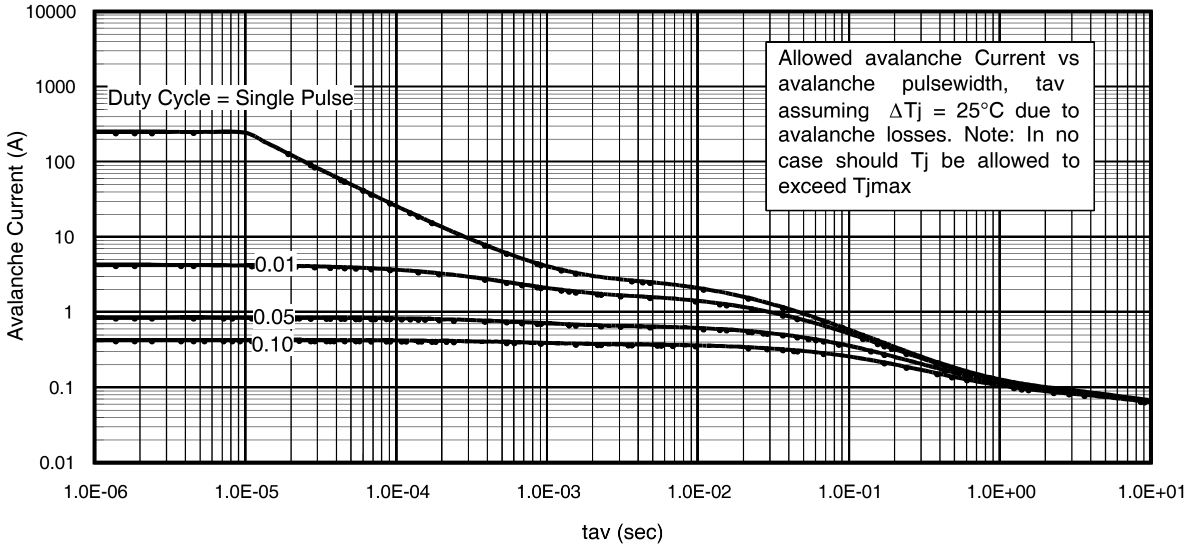


Fig 12. Typical Avalanche Current vs.Pulsewidth

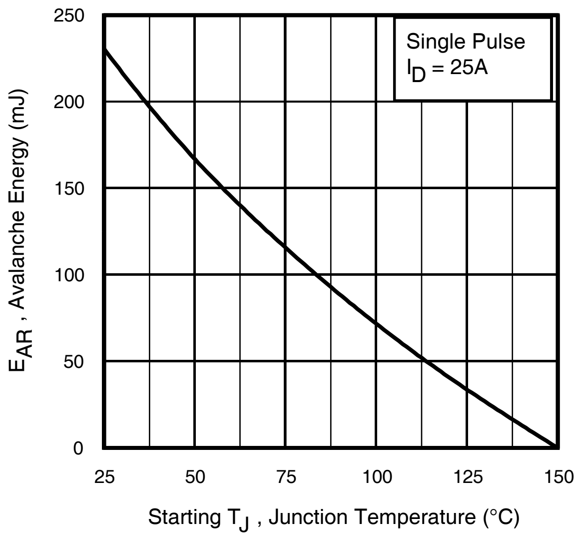


Fig 13. Maximum Avalanche Energy vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 12, 13:
(For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption:
   Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax}. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 16a, 16b.
4. $P_{D\ (ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 12, 13).
   t_{av} = Average time in avalanche.
   D = Duty cycle in avalanche = $t_{av} \cdot f$
   $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see figure 11)

$$P_{D\ (ave)} = 1/2\ (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$
$$E_{AS\ (AR)} = P_{D\ (ave)} \cdot t_{av}$$

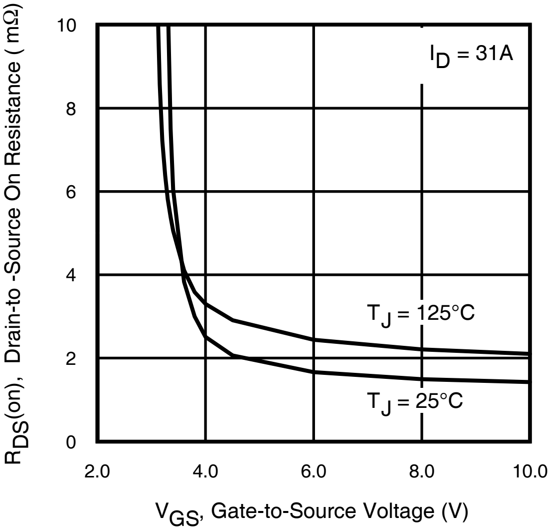


Fig 14. On-Resistance Vs. Gate Voltage

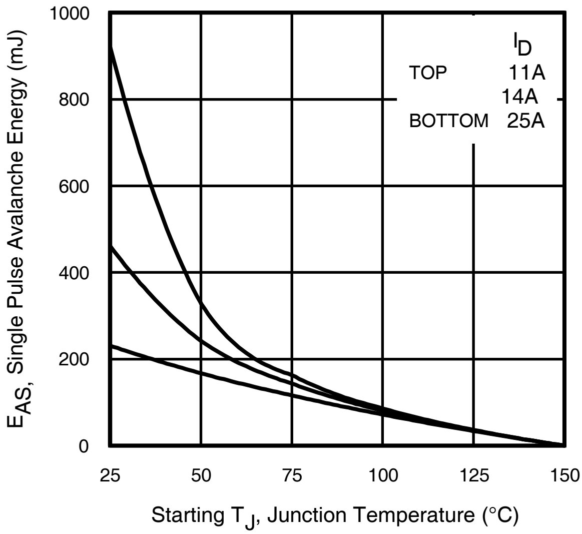


Fig 15. Maximum Avalanche Energy Vs. Drain Current

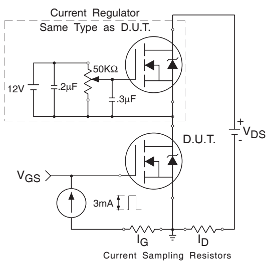


Fig 16a. Gate Charge Test Circuit

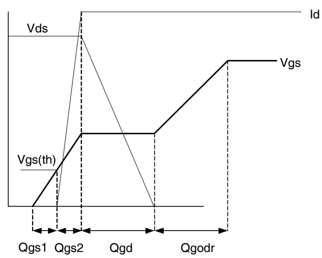


Fig 16b. Gate Charge Waveform

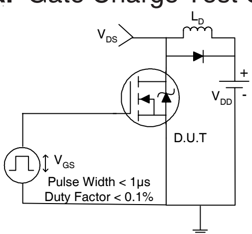


Fig 17a. Switching Time Test Circuit

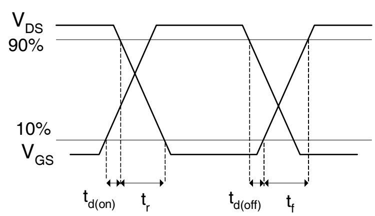


Fig 17b. Switching Time Waveforms

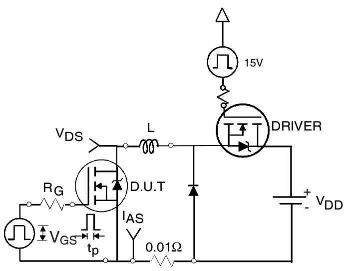


Fig 18a. Unclamped Inductive Test Circuit

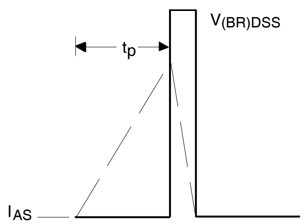


Fig 18b. Unclamped Inductive Waveforms

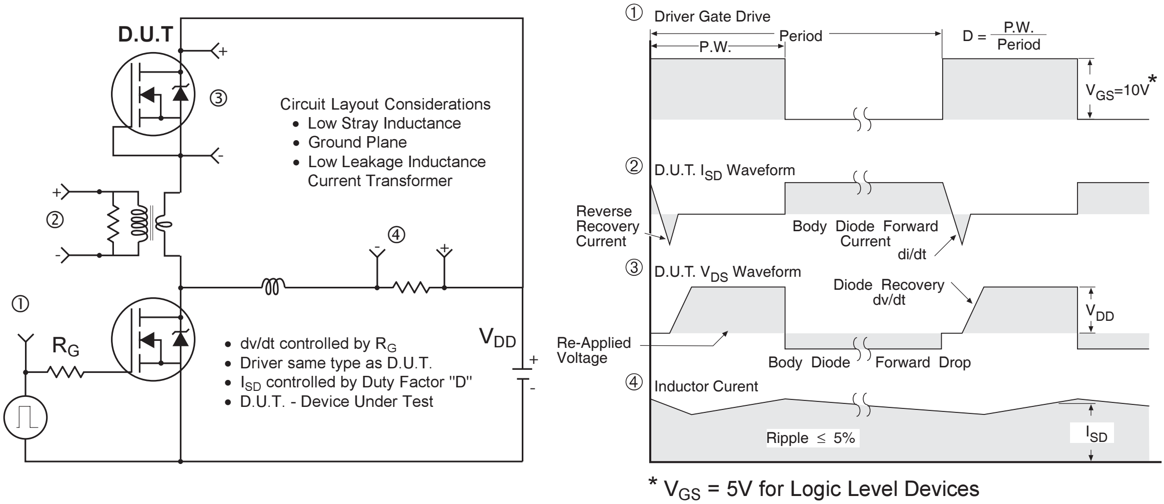
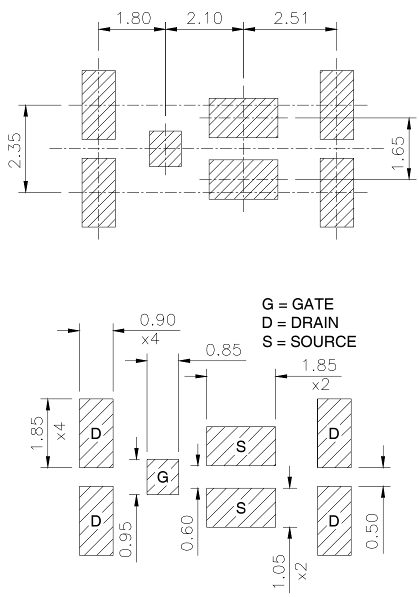


Fig 19. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

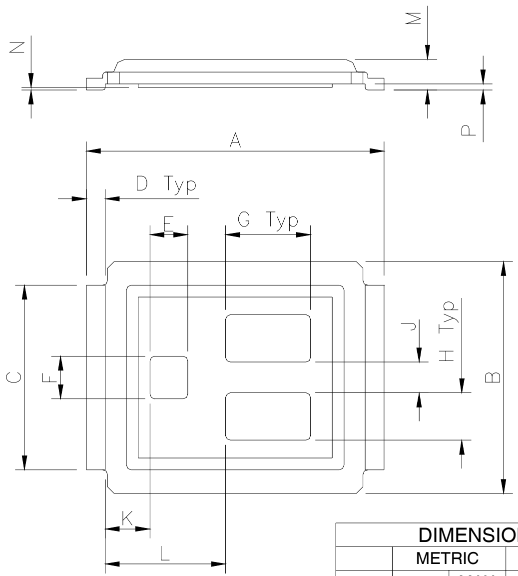
DirectFET™ Substrate and PCB Layout, MT Outline (Medium Size Can, T-Designation).

Please see DirectFET application note AN-1035 for all details regarding the assembly of DirectFET. This includes all recommendations for stencil and substrate designs.



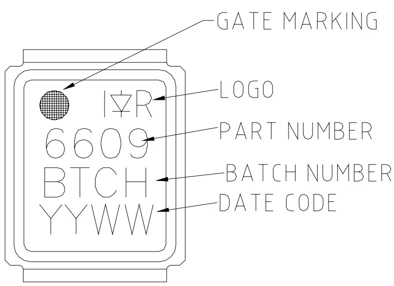
DirectFET™ Outline Dimension, MT Outline (Medium Size Can, T-Designation).

Please see DirectFET application note AN-1035 for all details regarding the assembly of DirectFET. This includes all recommendations for stencil and substrate designs.

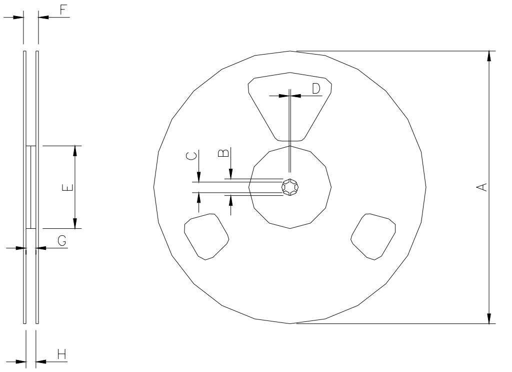


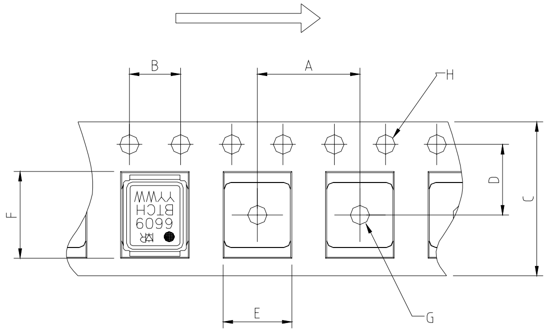
DIMENSIONS				
	METRIC		IMPERIAL	
CODE	MIN	MAX	MIN	MAX
A	6.25	6.35	0.246	0.250
B	4.80	5.05	0.189	0.199
C	3.85	3.95	0.152	0.156
D	0.35	0.45	0.014	0.018
E	0.78	0.82	0.031	0.032
F	0.88	0.92	0.035	0.036
G	1.78	1.82	0.070	0.072
H	0.98	1.02	0.039	0.040
J	0.63	0.67	0.025	0.026
K	0.88	1.01	0.035	0.039
L	2.46	2.63	0.097	0.104
M	0.59	0.70	0.023	0.028
N	0.03	0.08	0.001	0.003
P	0.08	0.17	0.003	0.007

DirectFET™ Part Marking



DirectFET™ Tape & Reel Dimension (Showing component orientation).





NOTE: Controlling dimensions in mm
Std reel quantity is 4800 parts. (ordered as IRF6609). For 1000 parts on 7" reel, order IRF6609TR1

REEL DIMENSIONS								
	STANDARD OPTION **(QTY 4800)**				TR1 OPTION **(QTY 1000)**			
	METRIC		IMPERIAL		METRIC		IMPERIAL	
CODE	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	330.0	N.C	12.992	N.C	177.77	N.C	6.9	N.C
B	20.2	N.C	0.795	N.C	19.06	N.C	0.75	N.C
C	12.8	13.2	0.504	0.520	13.5	12.8	0.53	0.50
D	1.5	N.C	0.059	N.C	1.5	N.C	0.059	N.C
E	100.0	N.C	3.937	N.C	58.72	N.C	2.31	N.C
F	N.C	18.4	N.C	0.724	N.C	13.50	N.C	0.53
G	12.4	14.4	0.488	0.567	11.9	12.01	0.47	N.C
H	11.9	15.4	0.469	0.606	11.9	12.01	0.47	N.C

NOTE: CONTROLLING DIMENSIONS IN MM

DIMENSIONS				
	METRIC		IMPERIAL	
CODE	MIN	MAX	MIN	MAX
A	7.90	8.10	0.311	0.319
B	3.90	4.10	0.154	0.161
C	11.90	12.30	0.469	0.484
D	5.45	5.55	0.215	0.219
E	5.10	5.30	0.201	0.209
F	6.50	6.70	0.256	0.264
G	1.50	N.C	0.059	N.C
H	1.50	1.60	0.059	0.063

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.
② Starting T_J = 25°C, L = 0.75mH, R_G = 25Ω, I_{AS} = 25A.
③ Pulse width ≤ 400µs; duty cycle ≤ 2%.
④ Surface mounted on 1 in. square Cu board.
⑤ Used double sided cooling , mounting pad.
⑥ Mounted on minimum footprint full size board with metalized back and with small clip heatsink.
⑦ T_C measured with thermal couple mounted to top (Drain) of part.
⑧ R_θ is measured at T_J of approximately 90°C.

Data and specifications subject to change without notice.
This product has been designed and qualified for the Consumer market.
Qualification Standards can be found on IR's Web site.

International
IOR Rectifier

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TAC Fax: (310) 252-7903
Visit us at www.irf.com for sales contact information.10/05

Note: For the most current drawings please refer to the IR website at:
http://www.irf.com/package/