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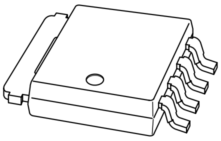


BUK9Y53-100B

N-channel TrenchMOS logic level FET

Rev. 01 — 30 August 2007 **Product data sheet**

1. Product profile

1.1 General description

N-channel enhancement mode power Field-Effect Transistor (FET) in a plastic package using NXP High-Performance Automotive (HPA) TrenchMOS technology.

1.2 Features

- Very low on-state resistance
- 175 °C rated
- Q101 compliant
- Logic level compatible

1.3 Applications

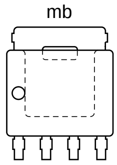
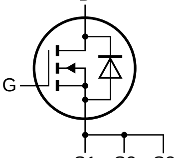
- Automotive systems
- Motors, lamps and solenoids
- General purpose power switching
- 12 V, 24 V and 42 V loads

1.4 Quick reference data

- $E_{DS(AL)S} \leq 85$ mJ
- $I_D \leq 23$ A
- $R_{DSon} = 45$ mΩ (typ)
- $P_{tot} \leq 75$ W

2. Pinning information

Table 1. Pinning

Pin	Description	Simplified outline	Symbol
1, 2, 3	source (S)	 SOT669 (LFPAK)	
4	gate (G)		
mb	mounting base; connected to drain (D)		

3. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
BUK9Y53-100B	LFPAK	plastic single-ended surface-mounted package (LFPAK); 4 leads	SOT669

4. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	100	V
V_{DGR}	drain-gate voltage (DC)	R_{GS} = 20 kΩ	-	100	V
V_{GS}	gate-source voltage		-	±15	V
I_D	drain current	T_{mb} = 25 °C; V_{GS} = 5 V; see Figure 2 and 3	-	23	A
		T_{mb} = 100 °C; V_{GS} = 5 V; see Figure 2	-	16	A
I_{DM}	peak drain current	T_{mb} = 25 °C; pulsed; t_p ≤ 10 µs; see Figure 3	-	94	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; see Figure 1	-	75	W
T_{stg}	storage temperature		–55	+175	°C
T_j	junction temperature		–55	+175	°C
Source-drain diode					
I_{DR}	reverse drain current	T_{mb} = 25 °C	-	23	A
I_{DRM}	peak reverse drain current	T_{mb} = 25 °C; pulsed; t_p ≤ 10 µs	-	94	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	unclamped inductive load; I_D = 23 A; V_{DS} ≤ 100 V; V_{GS} = 5 V; R_{GS} = 50 Ω; starting at T_j = 25 °C	-	85	mJ
$E_{DS(AL)R}$	repetitive drain-source avalanche energy		-	[1]	-

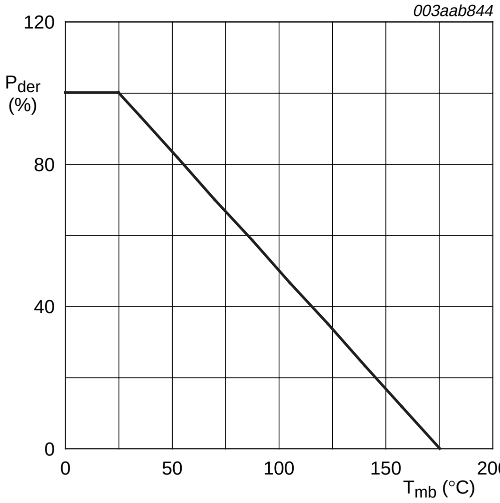
[1] Conditions:

a) Maximum value not quoted. Repetitive rating defined in Figure 16.

b) Single-pulse avalanche rating limited by $T_{j(max)}$ of 175 °C.

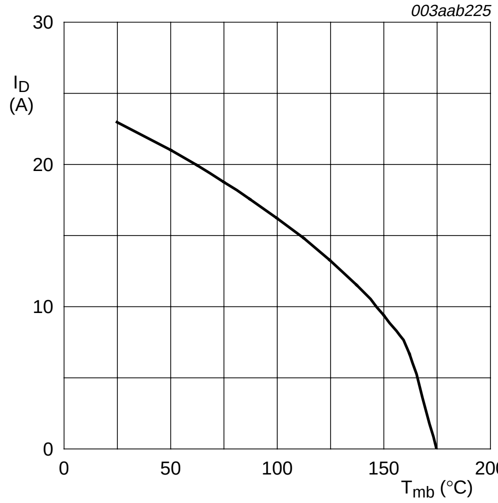
c) Repetitive avalanche rating limited by $T_{j(avg)}$ of 170 °C.

d) Refer to application note *AN10273* for further information.



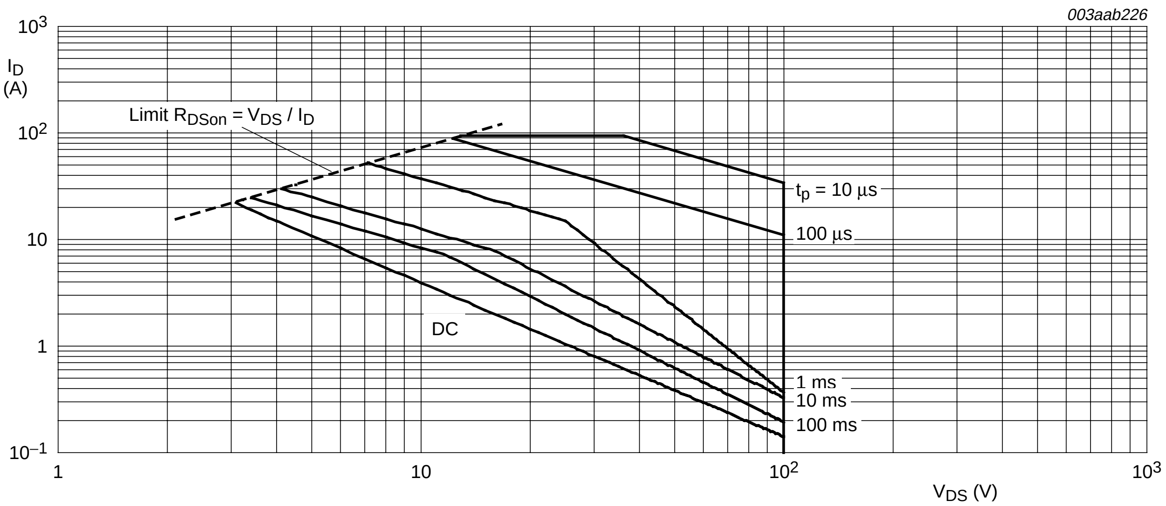
$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\ \%$$

Fig 1. Normalized total power dissipation as a function of mounting base temperature



$V_{GS} \geq 5$ V

Fig 2. Continuous drain current as a function of mounting base temperature



T_{mb} = 25 °C; I_{DM} is single pulse.

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	-	2	K/W

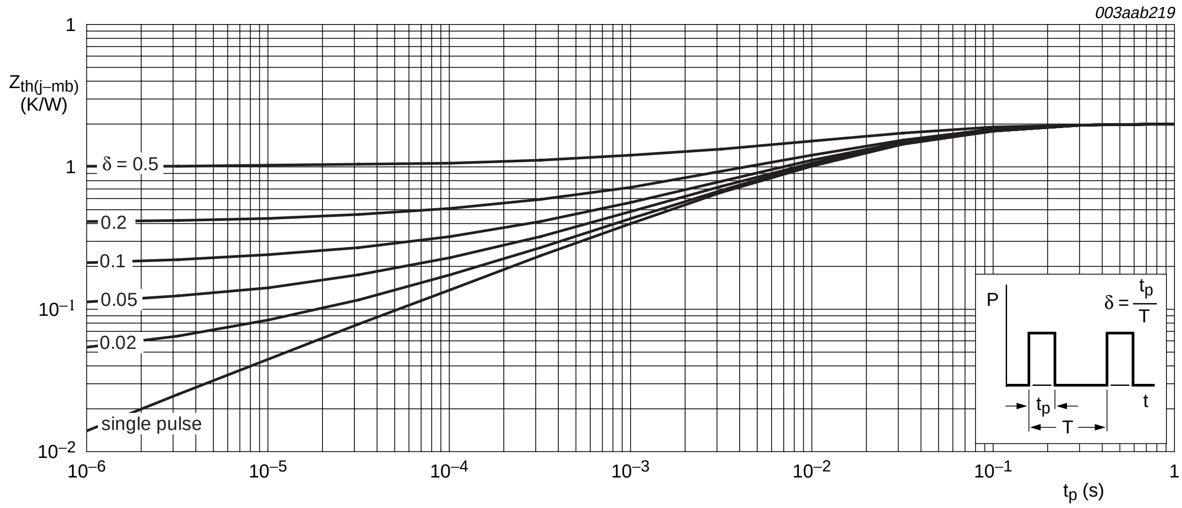


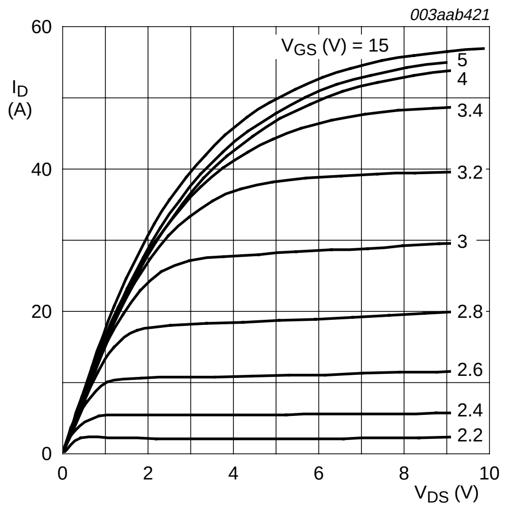
Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

Table 5: Characteristics

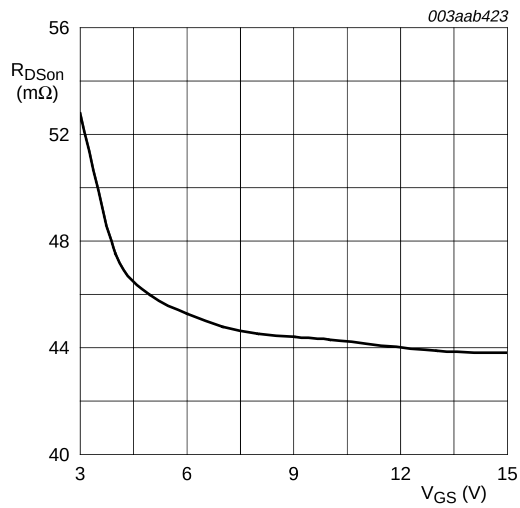
T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 0.25 mA; V_{GS} = 0 V				
		T_j = 25 °C	100	-	-	V
		T_j = –55 °C	89	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; see Figure 9 and 10				
		T_j = 25 °C	1.1	1.5	2	V
		T_j = 175 °C	0.5	-	-	V
		T_j = –55 °C	-	-	2.3	V
I_{DSS}	drain leakage current	V_{DS} = 100 V; V_{GS} = 0 V				
		T_j = 25 °C	-	0.02	1	µA
		T_j = 175 °C	-	-	500	µA
I_{GSS}	gate leakage current	V_{GS} = ±15 V; V_{DS} = 0 V	-	2	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 5 V; I_D = 10 A; see Figure 6 and 8				
		T_j = 25 °C	-	45	53	mΩ
		T_j = 175 °C	-	-	132	mΩ
		V_{GS} = 4.5 V; I_D = 10 A	-	-	59	mΩ
		V_{GS} = 10 V; I_D = 10 A	-	41	49	mΩ
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	I_D = 15 A; V_{DS} = 80 V; V_{GS} = 5 V; see Figure 14	-	18	-	nC
Q_{GS}	gate-source charge		-	4.1	-	nC
Q_{GD}	gate-drain charge		-	8	-	nC
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz; see Figure 12	-	1600	2130	pF
C_{oss}	output capacitance		-	141	170	pF
C_{rss}	reverse transfer capacitance		-	60	82	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 30 V; R_L = 2.5 Ω; V_{GS} = 5 V; R_G = 10 Ω	-	18	-	ns
t_r	rise time		-	26	-	ns
$t_{d(off)}$	turn-off delay time		-	52	-	ns
t_f	fall time		-	16	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	I_S = 25 A; V_{GS} = 0 V; see Figure 15	-	0.85	1.2	V
t_{rr}	reverse recovery time	I_S = 20 A; dI_S/dt = –100 A/µs; V_{GS} = 0 V; V_R = 30 V	-	71	-	ns
Q_r	recovered charge		-	83	-	nC



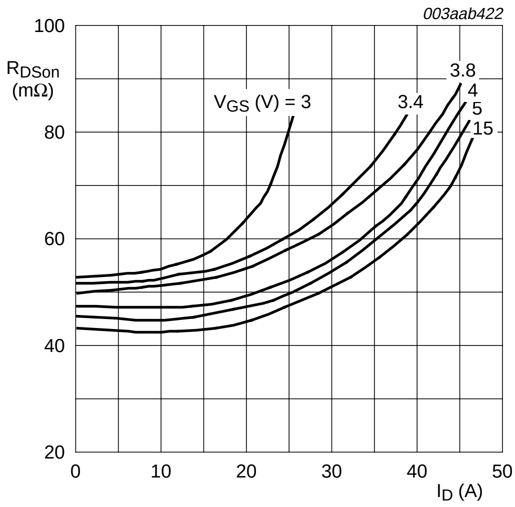
T_j = 25 °C

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



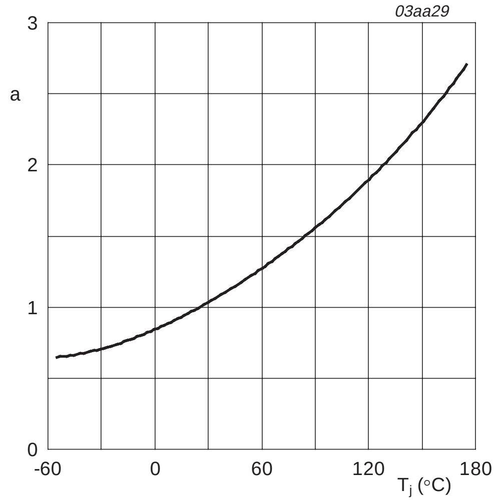
T_j = 25 °C; I_D = 20 A

Fig 6. Drain-source on-state resistance as a function of gate-source voltage; typical values



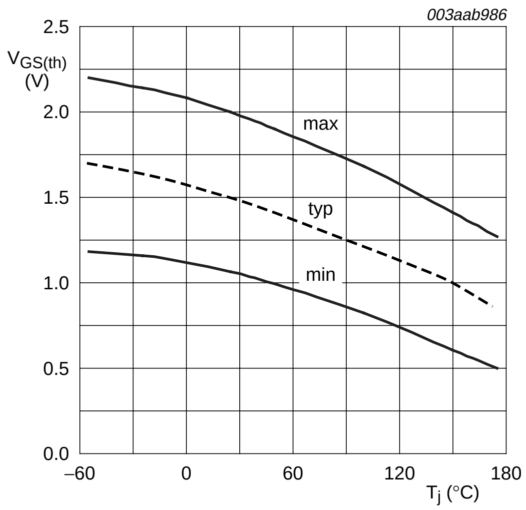
T_j = 25 °C

Fig 7. Drain-source on-state resistance as a function of drain current; typical values



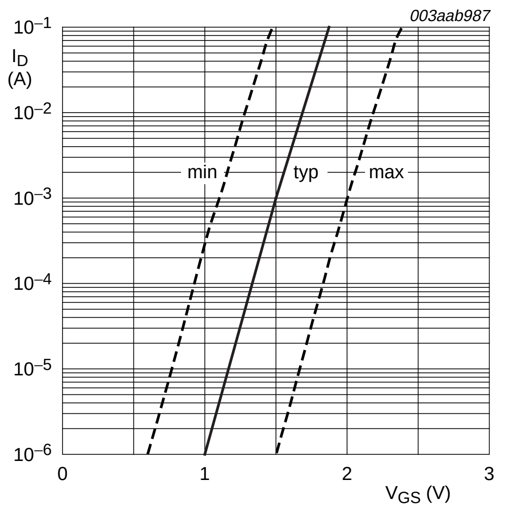
$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature



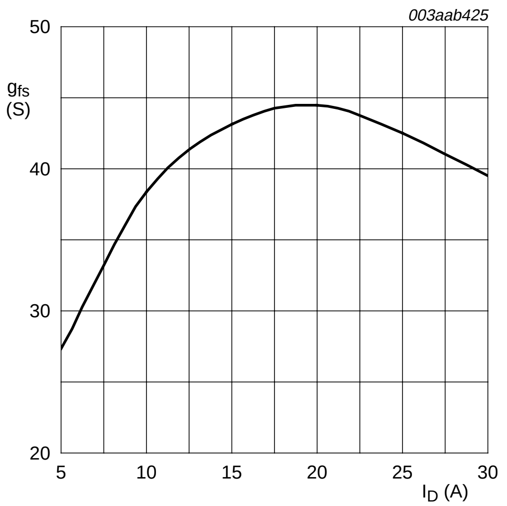
I_D = 1 mA; V_{DS} = V_{GS}

Fig 9. Gate-source threshold voltage as a function of junction temperature



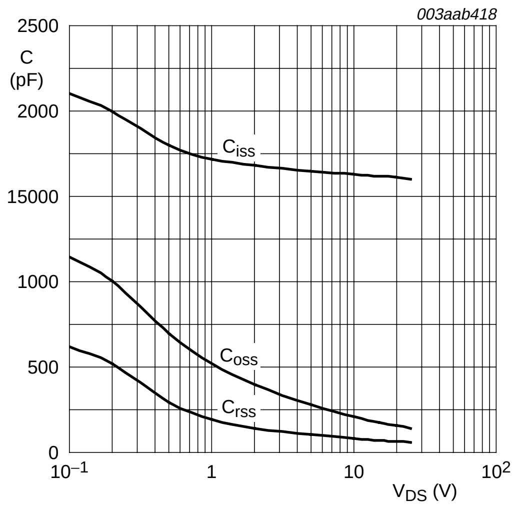
T_j = 25 °C; V_{DS} = V_{GS}

Fig 10. Sub-threshold drain current as a function of gate-source voltage



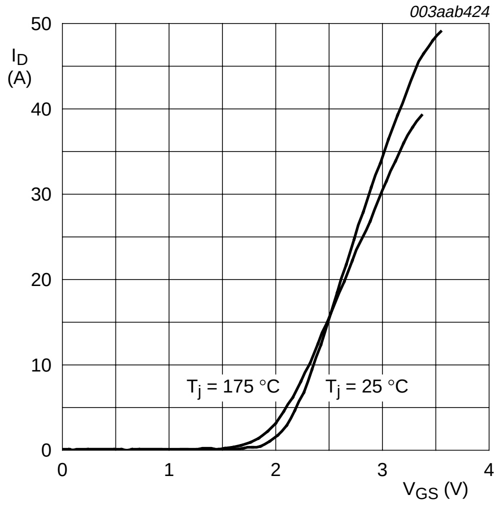
T_j = 25 °C; V_{DS} = 25 V

Fig 11. Forward transconductance as a function of drain current; typical values



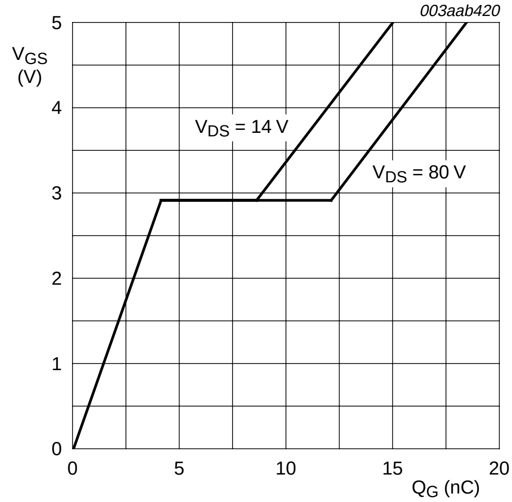
V_{GS} = 0 V; f = 1 MHz

Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



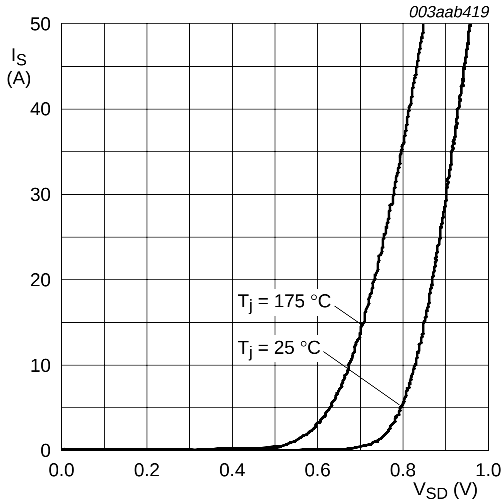
V_{DS} = 25 V

Fig 13. Transfer characteristics: drain current as a function of gate-source voltage; typical values



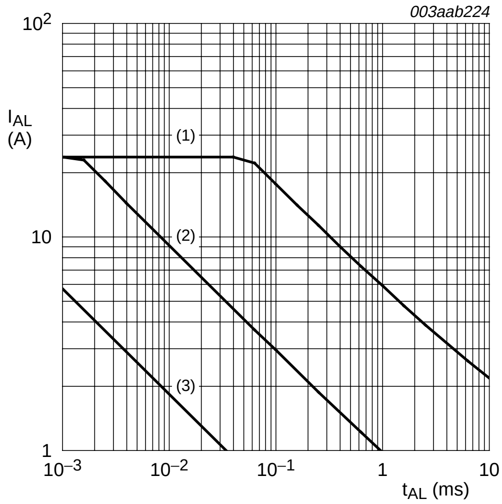
T_j = 25 °C; I_D = 10 A

Fig 14. Gate-source voltage as a function of gate charge; typical values



V_{GS} = 0 V

Fig 15. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values



See Table note 1 of Table 3 Limiting values.

(1) Single-pulse; T_j = 25 °C.

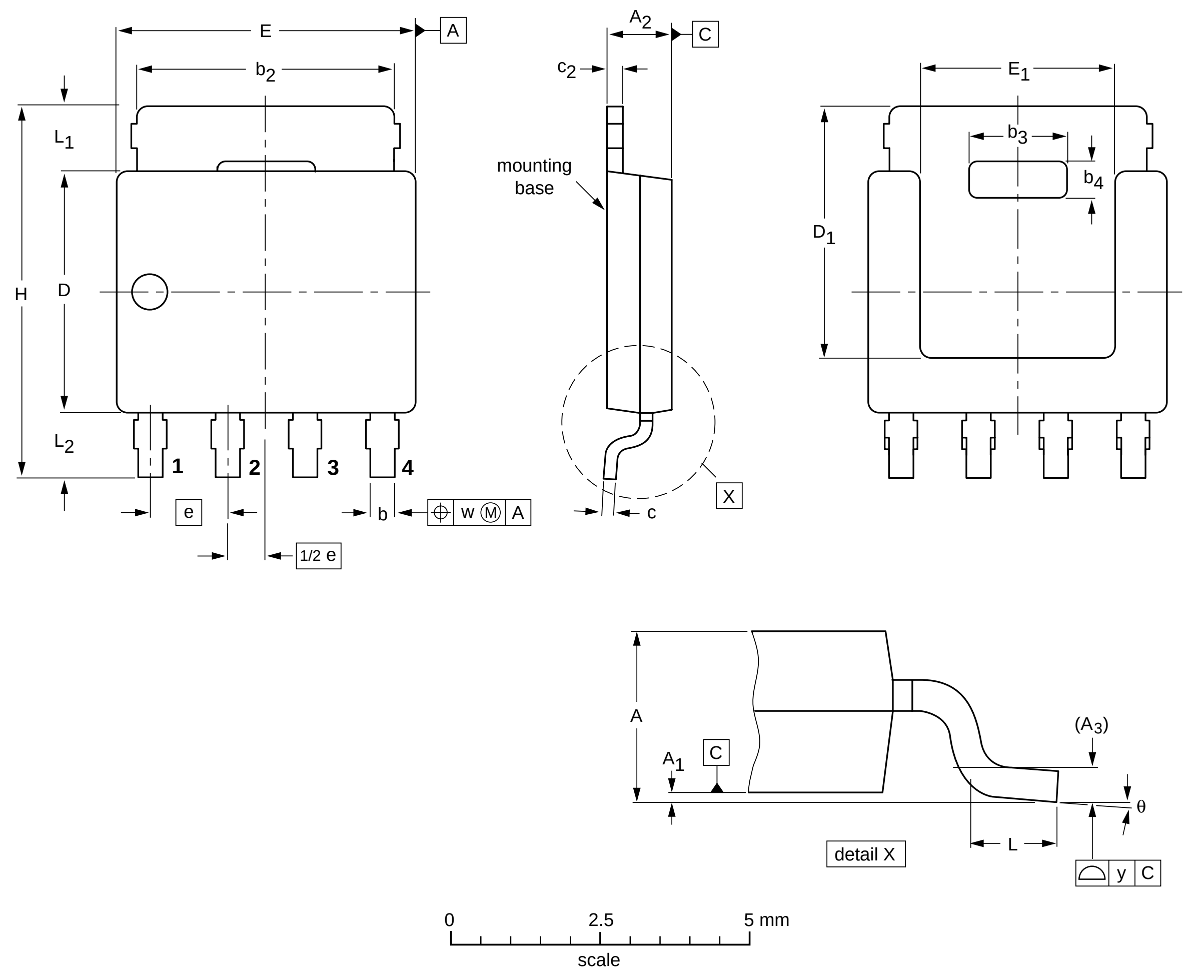
(2) Single-pulse; T_j = 150 °C.

(3) Repetitive.

Fig 16. Single-pulse and repetitive avalanche rating; avalanche current as a function of avalanche time

7. Package outline

Plastic single-ended surface-mounted package (LFPAK); 4 leads **SOT669**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	A_2	A_3	b	b_2	b_3	b_4	c	c_2	D(1)	D_1(1) max	E(1)	E_1(1)	e	H	L	L_1	L_2	w	y	θ
mm	1.20 1.01	0.15 0.00	1.10 0.95	0.25	0.50 0.35	4.41 3.62	2.2 2.0	0.9 0.7	0.25 0.19	0.30 0.24	4.10 3.80	4.20	5.0 4.8	3.3 3.1	1.27	6.2 5.8	0.85 0.40	1.3 0.8	1.3 0.8	0.25	0.1	8° 0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT669		MO-235				~~04-10-13~~ 06-03-16

Fig 17. Package outline SOT669 (LFPAK)

8. Revision history

Table 6. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK9Y53-100B_01	20070830	Product data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term ‘short data sheet’ is explained in section “Definitions”.

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11. Contents

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