74AUP2G126

Low-power dual buffer/line driver; 3-state

Rev. 10 — 28 October 2016 Product data sheet

1. General description

The 74AUP2G126 provides the dual non-inverting buffer/line driver with 3-state output. The 3-state output is controlled by the output enable input (nOE). A LOW level at pin nOE causes the output to assume a high-impedance OFF-state. This device has the input-disable feature, which allows floating input signals. The inputs are disabled when the output enable input nOE is LOW.

Schmitt trigger action at all inputs makes the circuit tolerant to slower input rise and fall times across the entire V_{CC} range from 0.8 V to 3.6 V. This device ensures a very low static and dynamic power consumption across the entire V_{CC} range from 0.8 V to 3.6 V.

This device is fully specified for partial power-down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing a damaging backflow current through the device when it is powered down.

2. Features and benefits

- Wide supply voltage range from 0.8 V to 3.6 V
- High noise immunity
- Complies with JEDEC standards:
  - JESD8-12 (0.8 V to 1.3 V)
  - JESD8-11 (0.9 V to 1.65 V)
  - JESD8-7 (1.2 V to 1.95 V)
  - JESD8-5 (1.8 V to 2.7 V)
  - JESD8-B (2.7 V to 3.6 V)
- ESD protection:
  - HBM JESD22-A114F Class 3A exceeds 5000 V
  - MM JESD22-A115-A exceeds 200 V
  - CDM JESD22-C101E exceeds 1000 V
- Low static power consumption; I_{CC} = 0.9 μA (maximum)
- Latch-up performance exceeds 100 mA per JESD78 Class II
- Inputs accept voltages up to 3.6 V
- Low noise overshoot and undershoot < 10 % of V_{CC}
- Input-disable feature allows floating input conditions
- I_{OFF} circuitry provides partial Power-down mode operation
- Multiple package options
- Specified from –40 °C to +85 °C and –40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74AUP2G126DC	–40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1
74AUP2G126GT	–40 °C to +125 °C	XSON8	plastic extremely thin small outline package; no leads; 8 terminals; body 1 × 1.95 × 0.5 mm	SOT833-1
74AUP2G126GF	–40 °C to +125 °C	XSON8	extremely thin small outline package; no leads; 8 terminals; body 1.35 × 1 × 0.5 mm	SOT1089
74AUP2G126GD	–40 °C to +125 °C	XSON8	plastic extremely thin small outline package; no leads; 8 terminals; body 3 × 2 × 0.5 mm	SOT996-2
74AUP2G126GM	–40 °C to +125 °C	XQFN8	plastic, extremely thin quad flat package; no leads; 8 terminals; body 1.6 × 1.6 × 0.5 mm	SOT902-2
74AUP2G126GN	–40 °C to +125 °C	XSON8	extremely thin small outline package; no leads; 8 terminals; body 1.2 × 1.0 × 0.35 mm	SOT1116
74AUP2G126GS	–40 °C to +125 °C	XSON8	extremely thin small outline package; no leads; 8 terminals; body 1.35 × 1.0 × 0.35 mm	SOT1203
74AUP2G126GX[1]	–40 °C to +125 °C	X2SON8	plastic thermal enhanced extremely thin small outline package; no leads; 8 terminals; body 1.35 × 0.8 × 0.35 mm	SOT1233

[1] Type number 74AUP2G126GX is in development.

4. Marking

Table 2. Marking codes

Type number	Marking code[1]
74AUP2G126DC	p26
74AUP2G126GT	p26
74AUP2G126GF	pN
74AUP2G126GD	p26
74AUP2G126GM	p26
74AUP2G126GN	pN
74AUP2G126GS	pN
74AUP2G126GX	pN

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

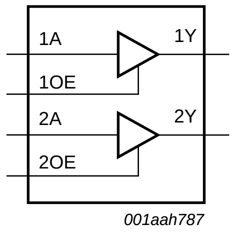


Fig 1. Logic symbol

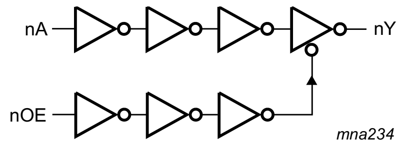


Fig 2. Logic diagram (one gate)

6. Pinning information

6.1 Pinning

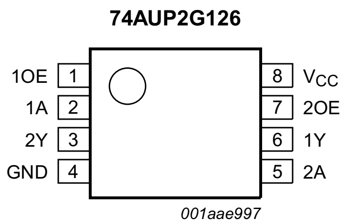


Fig 3. Pin configuration SOT765-1

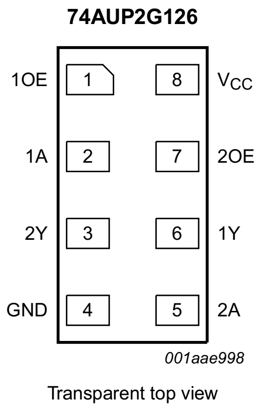


Fig 4. Pin configuration SOT833-1, SOT1089, SOT1116 and SOT1203

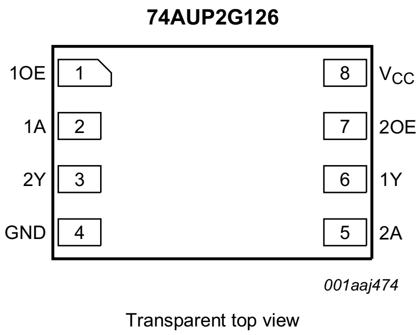


Fig 5. Pin configuration SOT996-2

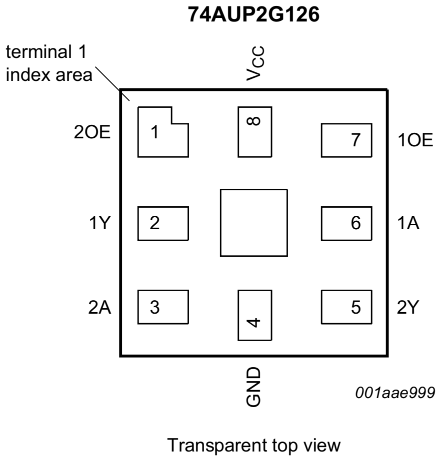


Fig 6. Pin configuration SOT902-2

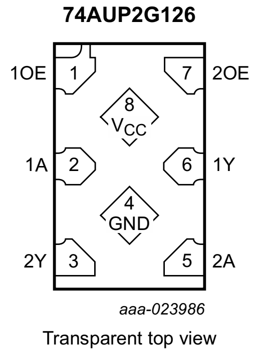


Fig 7. Pin configuration SOT1233

6.2 Pin description

Table 3. Pin description

Symbol	Pin		Description
	SOT765-1, SOT833-1, SOT1089, SOT996-2, SOT1116, SOT1203 and SOT1233	SOT902-2	
1OE, 2OE	1, 7	7, 1	output enable input (active HIGH)
1A, 2A	2, 5	6, 3	data input
1Y, 2Y	6, 3	2, 5	data output
GND	4	4	ground (0 V)
V_{CC}	8	8	supply voltage

7. Functional description

Table 4. Function table[1]

Input		Output
nOE	nA	nY
H	L	L
H	H	H
L	X	Z

[1] H = HIGH voltage level; L = LOW voltage level; X = don’t care; Z = high-impedance OFF-state.

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		–0.5	+4.6	V
I_{IK}	input clamping current	$V_I < 0$ V	–50	-	mA
V_I	input voltage	[1]	–0.5	+4.6	V
I_{OK}	output clamping current	$V_O < 0$ V	–50	-	mA
V_O	output voltage	Active mode and Power-down mode [1]	–0.5	+4.6	V
I_O	output current	$V_O = 0$ V to V_{CC}	-	±20	mA
I_{CC}	supply current		-	50	mA
I_{GND}	ground current		–50	-	mA
T_{stg}	storage temperature		–65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +125 °C [2]	-	250	mW

[1] The minimum input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For VSSOP8 packages: above 110 °C the value of P_{tot} derates linearly with 8.0 mW/K.
For XSON8 and XQFN8 packages: above 118 °C the value of P_{tot} derates linearly with 7.8 mW/K.
For X2SON8 package: above 118 °C the value of P_{tot} derates linearly with 7.7 mW/K.

9. Recommended operating conditions

Table 6. Operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		0.8	3.6	V
V_I	input voltage		0	3.6	V
V_O	output voltage	Active mode	0	V_{CC}	V
		Power-down mode; $V_{CC} = 0$ V	0	3.6	V
T_{amb}	ambient temperature		–40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 0.8$ V to 3.6 V	0	200	ns/V

10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 0.8 V	0.70 × V_{CC}	-	-	V
		V_{CC} = 0.9 V to 1.95 V	0.65 × V_{CC}	-	-	V
		V_{CC} = 2.3 V to 2.7 V	1.6	-	-	V
		V_{CC} = 3.0 V to 3.6 V	2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 0.8 V	-	-	0.30 × V_{CC}	V
		V_{CC} = 0.9 V to 1.95 V	-	-	0.35 × V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V	-	-	0.7	V
		V_{CC} = 3.0 V to 3.6 V	-	-	0.9	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = −20 μA; V_{CC} = 0.8 V to 3.6 V	V_{CC} − 0.1	-	-	V
		I_O = −1.1 mA; V_{CC} = 1.1 V	0.75 × V_{CC}	-	-	V
		I_O = −1.7 mA; V_{CC} = 1.4 V	1.11	-	-	V
		I_O = −1.9 mA; V_{CC} = 1.65 V	1.32	-	-	V
		I_O = −2.3 mA; V_{CC} = 2.3 V	2.05	-	-	V
		I_O = −3.1 mA; V_{CC} = 2.3 V	1.9	-	-	V
		I_O = −2.7 mA; V_{CC} = 3.0 V	2.72	-	-	V
		I_O = −4.0 mA; V_{CC} = 3.0 V	2.6	-	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = 20 μA; V_{CC} = 0.8 V to 3.6 V	-	-	0.1	V
		I_O = 1.1 mA; V_{CC} = 1.1 V	-	-	0.3 × V_{CC}	V
		I_O = 1.7 mA; V_{CC} = 1.4 V	-	-	0.31	V
		I_O = 1.9 mA; V_{CC} = 1.65 V	-	-	0.31	V
		I_O = 2.3 mA; V_{CC} = 2.3 V	-	-	0.31	V
		I_O = 3.1 mA; V_{CC} = 2.3 V	-	-	0.44	V
		I_O = 2.7 mA; V_{CC} = 3.0 V	-	-	0.31	V
		I_O = 4.0 mA; V_{CC} = 3.0 V	-	-	0.44	V
I_I	input leakage current	V_I = GND to 3.6 V; V_{CC} = 0 V to 3.6 V	-	-	±0.1	μA
I_{OZ}	OFF-state output current	V_I = V_{IH} or V_{IL}; V_O = 0 V to 3.6 V; V_{CC} = 0 V to 3.6 V	-	-	±0.1	μA
I_{OFF}	power-off leakage current	V_I or V_O = 0 V to 3.6 V; V_{CC} = 0 V	-	-	±0.2	μA
ΔI_{OFF}	additional power-off leakage current	V_I or V_O = 0 V to 3.6 V; V_{CC} = 0 V to 0.2 V	-	-	±0.2	μA
I_{CC}	supply current	V_I = GND or V_{CC}; I_O = 0 A; V_{CC} = 0.8 V to 3.6 V	-	-	0.5	μA

Table 7. Static characteristics *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
ΔI_{CC}	additional supply current	data input; $V_I = V_{CC} - 0.6$ V; $I_O = 0$ A; $V_{CC} = 3.3$ V	[1]	-	-	40	µA
		nOE input; $V_I = V_{CC} - 0.6$ V; $I_O = 0$ A; $V_{CC} = 3.3$ V	[1]	-	-	110	µA
		all inputs; V_I = GND to 3.6 V; nOE = GND; V_{CC} = 0.8 V to 3.6 V	[2]	-	-	1	µA
C_I	input capacitance	V_I = GND or V_{CC}; V_{CC} = 0 V to 3.6 V		-	0.9	-	pF
C_O	output capacitance	output enabled; V_O = GND; V_{CC} = 0 V		-	1.7	-	pF
		output disabled; V_O = GND or V_{CC}; V_{CC} = 0 V to 3.6 V		-	1.5	-	pF
T_{amb} = –40 °C to +85 °C							
V_{IH}	HIGH-level input voltage	V_{CC} = 0.8 V		$0.70 \times V_{CC}$	-	-	V
		V_{CC} = 0.9 V to 1.95 V		$0.65 \times V_{CC}$	-	-	V
		V_{CC} = 2.3 V to 2.7 V		1.6	-	-	V
		V_{CC} = 3.0 V to 3.6 V		2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 0.8 V		-	-	$0.30 \times V_{CC}$	V
		V_{CC} = 0.9 V to 1.95 V		-	-	$0.35 \times V_{CC}$	V
		V_{CC} = 2.3 V to 2.7 V		-	-	0.7	V
		V_{CC} = 3.0 V to 3.6 V		-	-	0.9	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		I_O = –20 µA; V_{CC} = 0.8 V to 3.6 V		$V_{CC} - 0.1$	-	-	V
		I_O = –1.1 mA; V_{CC} = 1.1 V		$0.7 \times V_{CC}$	-	-	V
		I_O = –1.7 mA; V_{CC} = 1.4 V		1.03	-	-	V
		I_O = –1.9 mA; V_{CC} = 1.65 V		1.30	-	-	V
		I_O = –2.3 mA; V_{CC} = 2.3 V		1.97	-	-	V
		I_O = –3.1 mA; V_{CC} = 2.3 V		1.85	-	-	V
		I_O = –2.7 mA; V_{CC} = 3.0 V		2.67	-	-	V
		I_O = –4.0 mA; V_{CC} = 3.0 V		2.55	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		I_O = 20 µA; V_{CC} = 0.8 V to 3.6 V		-	-	0.1	V
		I_O = 1.1 mA; V_{CC} = 1.1 V		-	-	$0.3 \times V_{CC}$	V
		I_O = 1.7 mA; V_{CC} = 1.4 V		-	-	0.37	V
		I_O = 1.9 mA; V_{CC} = 1.65 V		-	-	0.35	V
		I_O = 2.3 mA; V_{CC} = 2.3 V		-	-	0.33	V
		I_O = 3.1 mA; V_{CC} = 2.3 V		-	-	0.45	V
		I_O = 2.7 mA; V_{CC} = 3.0 V		-	-	0.33	V
		I_O = 4.0 mA; V_{CC} = 3.0 V		-	-	0.45	V
I_I	input leakage current	V_I = GND to 3.6 V; V_{CC} = 0 V to 3.6 V		-	-	±0.5	µA
I_{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL}; V_O = 0 V to 3.6 V; V_{CC} = 0 V to 3.6 V		-	-	±0.5	µA
I_{OFF}	power-off leakage current	V_I or V_O = 0 V to 3.6 V; V_{CC} = 0 V		-	-	±0.5	µA

Table 7. Static characteristics *...continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
ΔI_{OFF}	additional power-off leakage current	V_I or V_O = 0 V to 3.6 V; V_{CC} = 0 V to 0.2 V		-	-	±0.6	μA
I_{CC}	supply current	V_I = GND or V_{CC}; I_O = 0 A; V_{CC} = 0.8 V to 3.6 V		-	-	0.9	μA
ΔI_{CC}	additional supply current	data input; $V_I = V_{CC} - 0.6$ V; I_O = 0 A; V_{CC} = 3.3 V	[1]	-	-	50	μA
		nOE input; $V_I = V_{CC} - 0.6$ V; I_O = 0 A; V_{CC} = 3.3 V	[1]	-	-	120	μA
		all inputs; V_I = GND to 3.6 V; nOE = GND; V_{CC} = 0.8 V to 3.6 V	[2]	-	-	1	μA
T_{amb} = –40 °C to +125 °C							
V_{IH}	HIGH-level input voltage	V_{CC} = 0.8 V		$0.75 \times V_{CC}$	-	-	V
		V_{CC} = 0.9 V to 1.95 V		$0.70 \times V_{CC}$	-	-	V
		V_{CC} = 2.3 V to 2.7 V		1.6	-	-	V
		V_{CC} = 3.0 V to 3.6 V		2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 0.8 V		-	-	$0.25 \times V_{CC}$	V
		V_{CC} = 0.9 V to 1.95 V		-	-	$0.30 \times V_{CC}$	V
		V_{CC} = 2.3 V to 2.7 V		-	-	0.7	V
		V_{CC} = 3.0 V to 3.6 V		-	-	0.9	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		I_O = –20 μA; V_{CC} = 0.8 V to 3.6 V		$V_{CC} - 0.11$	-	-	V
		I_O = –1.1 mA; V_{CC} = 1.1 V		$0.6 \times V_{CC}$	-	-	V
		I_O = –1.7 mA; V_{CC} = 1.4 V		0.93	-	-	V
		I_O = –1.9 mA; V_{CC} = 1.65 V		1.17	-	-	V
		I_O = –2.3 mA; V_{CC} = 2.3 V		1.77	-	-	V
		I_O = –3.1 mA; V_{CC} = 2.3 V		1.67	-	-	V
		I_O = –2.7 mA; V_{CC} = 3.0 V		2.40	-	-	V
		I_O = –4.0 mA; V_{CC} = 3.0 V		2.30	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		I_O = 20 μA; V_{CC} = 0.8 V to 3.6 V		-	-	0.11	V
		I_O = 1.1 mA; V_{CC} = 1.1 V		-	-	$0.33 \times V_{CC}$	V
		I_O = 1.7 mA; V_{CC} = 1.4 V		-	-	0.41	V
		I_O = 1.9 mA; V_{CC} = 1.65 V		-	-	0.39	V
		I_O = 2.3 mA; V_{CC} = 2.3 V		-	-	0.36	V
		I_O = 3.1 mA; V_{CC} = 2.3 V		-	-	0.50	V
		I_O = 2.7 mA; V_{CC} = 3.0 V		-	-	0.36	V
		I_O = 4.0 mA; V_{CC} = 3.0 V		-	-	0.50	V
I_I	input leakage current	V_I = GND to 3.6 V; V_{CC} = 0 V to 3.6 V		-	-	±0.75	μA
I_{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL}; V_O = 0 V to 3.6 V; V_{CC} = 0 V to 3.6 V		-	-	±0.75	μA
I_{OFF}	power-off leakage current	V_I or V_O = 0 V to 3.6 V; V_{CC} = 0 V		-	-	±0.75	μA

Table 7. Static characteristics *...continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
ΔI_{OFF}	additional power-off leakage current	V_I or V_O = 0 V to 3.6 V; V_{CC} = 0 V to 0.2 V		-	-	±0.75	µA
I_{CC}	supply current	V_I = GND or V_{CC}; I_O = 0 A; V_{CC} = 0.8 V to 3.6 V		-	-	1.4	µA
ΔI_{CC}	additional supply current	data input; $V_I = V_{CC} - 0.6$ V; I_O = 0 A; V_{CC} = 3.3 V	[1]	-	-	75	µA
		nOE input; $V_I = V_{CC} - 0.6$ V; I_O = 0 A; V_{CC} = 3.3 V	[1]	-	-	180	µA
		all inputs; V_I = GND to 3.6 V; nOE = GND; V_{CC} = 0.8 V to 3.6 V	[2]	-	-	1	µA

[1] One input at V_{CC} – 0.6 V, other input at V_{CC} or GND.

[2] To show I_{CC} remains very low when the input-disable feature is enabled.

11. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 10.

Symbol	Parameter	Conditions		25 °C			–40 °C to +125 °C			Unit
				Min	Typ[1]	Max	Min	Max (85 °C)	Max (125 °C)	
C_L = 5 pF										
t_{pd}	propagation delay	nA to nY; see Figure 8	[2]							
		V_{CC} = 0.8 V		-	20.6	-	-	-	-	ns
		V_{CC} = 1.1 V to 1.3 V		2.8	5.5	10.5	2.5	11.7	12.9	ns
		V_{CC} = 1.4 V to 1.6 V		2.2	3.9	6.1	2.0	7.3	8.1	ns
		V_{CC} = 1.65 V to 1.95 V		1.9	3.2	4.1	1.7	6.1	6.7	ns
		V_{CC} = 2.3 V to 2.7 V		1.6	2.6	3.6	1.4	4.3	4.9	ns
		V_{CC} = 3.0 V to 3.6 V		1.4	2.4	3.1	1.2	3.9	4.4	ns
t_{en}	enable time	nOE to nY; see Figure 9	[3]							
		V_{CC} = 0.8 V		-	71.6	-	-	-	-	ns
		V_{CC} = 1.1 V to 1.3 V		2.8	6.2	12.4	2.6	13.6	13.6	ns
		V_{CC} = 1.4 V to 1.6 V		2.3	4.2	6.9	2.2	7.4	7.7	ns
		V_{CC} = 1.65 V to 1.95 V		1.9	3.3	5.3	1.7	5.9	6.2	ns
		V_{CC} = 2.3 V to 2.7 V		1.5	2.4	3.6	1.4	3.8	4.1	ns
		V_{CC} = 3.0 V to 3.6 V		1.3	2.0	2.9	1.2	3.2	3.4	ns
t_{dis}	disable time	nOE to nY; see Figure 9	[4]							
		V_{CC} = 0.8 V		-	10.3	-	-	-	-	ns
		V_{CC} = 1.1 V to 1.3 V		2.6	4.2	6.2	2.9	6.4	6.5	ns
		V_{CC} = 1.4 V to 1.6 V		2.1	3.2	4.4	2.2	4.6	4.7	ns
		V_{CC} = 1.65 V to 1.95 V		2.1	3.1	4.4	1.7	4.6	4.8	ns
		V_{CC} = 2.3 V to 2.7 V		1.7	2.4	3.2	1.4	3.4	3.6	ns
		V_{CC} = 3.0 V to 3.6 V		2.1	2.8	3.6	1.2	3.7	3.8	ns

Table 8. Dynamic characteristics *...continued*

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 10.

Symbol	Parameter	Conditions		25 °C			–40 °C to +125 °C			Unit
				Min	Typ[1]	Max	Min	Max (85 °C)	Max (125 °C)	
C_L = 10 pF										
t_{pd}	propagation delay	nA to nY; see Figure 8	[2]							
		V_{CC} = 0.8 V		-	24.0	-	-	-	-	ns
		V_{CC} = 1.1 V to 1.3 V		3.2	6.4	12.3	3.0	13.8	15.2	ns
		V_{CC} = 1.4 V to 1.6 V		2.1	4.5	7.3	1.9	8.5	9.4	ns
		V_{CC} = 1.65 V to 1.95 V		1.9	3.8	5.5	1.7	6.8	7.6	ns
		V_{CC} = 2.3 V to 2.7 V		2.1	3.2	4.2	1.6	5.3	5.9	ns
		V_{CC} = 3.0 V to 3.6 V		1.8	3.0	3.8	1.6	4.6	5.2	ns
t_{en}	enable time	nOE to nY; see Figure 9	[3]							
		V_{CC} = 0.8 V		-	75.3	-	-	-	-	ns
		V_{CC} = 1.1 V to 1.3 V		3.2	7.1	14.1	3.0	15.4	15.4	ns
		V_{CC} = 1.4 V to 1.6 V		2.2	4.8	8.0	2.1	8.3	8.6	ns
		V_{CC} = 1.65 V to 1.95 V		1.8	3.9	5.9	1.7	6.5	6.8	ns
		V_{CC} = 2.3 V to 2.7 V		1.5	2.9	4.2	1.4	4.5	4.8	ns
		V_{CC} = 3.0 V to 3.6 V		1.4	2.6	3.6	1.3	3.8	4.0	ns
t_{dis}	disable time	nOE to nY; see Figure 9	[4]							
		V_{CC} = 0.8 V		-	12.2	-	-	-	-	ns
		V_{CC} = 1.1 V to 1.3 V		3.5	5.3	7.6	3.3	7.9	7.9	ns
		V_{CC} = 1.4 V to 1.6 V		2.2	4.1	5.6	2.1	5.7	5.9	ns
		V_{CC} = 1.65 V to 1.95 V		2.4	4.2	5.7	1.7	5.8	6.0	ns
		V_{CC} = 2.3 V to 2.7 V		1.9	3.2	4.1	1.4	4.3	4.5	ns
		V_{CC} = 3.0 V to 3.6 V		2.4	4.1	5.0	1.3	5.2	5.3	ns
C_L = 15 pF										
t_{pd}	propagation delay	nA to nY; see Figure 8	[2]							
		V_{CC} = 0.8 V		-	27.4	-	-	-	-	ns
		V_{CC} = 1.1 V to 1.3 V		3.6	7.2	14.1	3.3	15.8	17.5	ns
		V_{CC} = 1.4 V to 1.6 V		3.0	5.1	8.1	2.5	9.8	10.9	ns
		V_{CC} = 1.65 V to 1.95 V		2.2	4.3	6.3	2.0	7.9	8.8	ns
		V_{CC} = 2.3 V to 2.7 V		2.0	3.7	4.9	1.8	6.0	6.7	ns
		V_{CC} = 3.0 V to 3.6 V		2.0	3.5	4.4	1.8	5.4	6.1	ns
t_{en}	enable time	nOE to nY; see Figure 9	[3]							
		V_{CC} = 0.8 V		-	79.2	-	-	-	-	ns
		V_{CC} = 1.1 V to 1.3 V		3.6	7.8	15.8	3.3	17.1	17.1	ns
		V_{CC} = 1.4 V to 1.6 V		3.0	5.4	8.8	2.9	9.4	9.7	ns
		V_{CC} = 1.65 V to 1.95 V		2.1	4.3	6.7	2.0	7.3	7.7	ns
		V_{CC} = 2.3 V to 2.7 V		1.8	3.4	4.8	1.7	5.2	5.6	ns
		V_{CC} = 3.0 V to 3.6 V		1.6	3.1	4.1	1.5	4.5	4.7	ns

Table 8. Dynamic characteristics *...continued*

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 10.

Symbol	Parameter	Conditions	25 °C			−40 °C to +125 °C			Unit
			Min	Typ[1]	Max	Min	Max (85 °C)	Max (125 °C)	
t_{dis}	disable time	nOE to nY; see Figure 9 [4]							
		V_{CC} = 0.8 V	-	14.9	-	-	-	-	ns
		V_{CC} = 1.1 V to 1.3 V	4.3	6.4	8.5	3.7	9.3	9.4	ns
		V_{CC} = 1.4 V to 1.6 V	3.0	5.0	6.6	2.5	6.9	7.0	ns
		V_{CC} = 1.65 V to 1.95 V	3.1	5.4	6.6	2.0	7.4	7.5	ns
		V_{CC} = 2.3 V to 2.7 V	2.4	4.0	5.0	1.7	5.1	5.5	ns
		V_{CC} = 3.0 V to 3.6 V	3.2	5.3	6.2	1.5	6.7	6.9	ns
C_L = 30 pF									
t_{pd}	propagation delay	nA to nY; see Figure 8 [2]							
		V_{CC} = 0.8 V	-	37.4	-	-	-	-	ns
		V_{CC} = 1.1 V to 1.3 V	4.8	9.5	18.7	4.4	21.4	24.0	ns
		V_{CC} = 1.4 V to 1.6 V	4.0	6.7	10.8	3.0	13.0	14.5	ns
		V_{CC} = 1.65 V to 1.95 V	2.9	5.6	8.4	2.6	10.3	11.5	ns
		V_{CC} = 2.3 V to 2.7 V	2.7	4.8	6.3	2.5	7.8	8.7	ns
		V_{CC} = 3.0 V to 3.6 V	2.7	4.6	5.8	2.5	7.0	8.3	ns
t_{en}	enable time	nOE to nY; see Figure 9 [3]							
		V_{CC} = 0.8 V	-	90.6	-	-	-	-	ns
		V_{CC} = 1.1 V to 1.3 V	4.7	10.0	20.4	4.3	22.0	22.0	ns
		V_{CC} = 1.4 V to 1.6 V	3.0	6.9	11.3	3.7	12.0	12.5	ns
		V_{CC} = 1.65 V to 1.95 V	2.6	5.6	8.6	3.2	9.5	10.1	ns
		V_{CC} = 2.3 V to 2.7 V	2.3	4.5	6.3	2.9	6.8	7.3	ns
		V_{CC} = 3.0 V to 3.6 V	2.2	4.2	5.8	2.7	6.4	6.7	ns
t_{dis}	disable time	nOE to nY; see Figure 9 [4]							
		V_{CC} = 0.8 V	-	51.6	-	-	-	-	ns
		V_{CC} = 1.1 V to 1.3 V	6.0	9.8	13.6	4.7	14.3	14.4	ns
		V_{CC} = 1.4 V to 1.6 V	4.5	7.7	10.5	3.0	10.7	11.0	ns
		V_{CC} = 1.65 V to 1.95 V	5.2	8.8	11.4	2.6	11.5	11.6	ns
		V_{CC} = 2.3 V to 2.7 V	3.9	6.4	7.4	2.3	9.0	10.2	ns
		V_{CC} = 3.0 V to 3.6 V	5.5	9.0	10.7	2.2	10.8	12.0	ns

Table 8. Dynamic characteristics *...continued*

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 10.

Symbol	Parameter	Conditions	25 °C			−40 °C to +125 °C			Unit
			Min	Typ[1]	Max	Min	Max (85 °C)	Max (125 °C)	
C_L = 5 pF, 10 pF, 15 pF and 30 pF									
C_{PD}	power dissipation capacitance	output enabled; f_i = 1 MHz; V_I = GND to V_{CC} [5]							
		V_{CC} = 0.8 V	-	2.7	-	-	-	-	pF
		V_{CC} = 1.1 V to 1.3 V	-	2.8	-	-	-	-	pF
		V_{CC} = 1.4 V to 1.6 V	-	2.9	-	-	-	-	pF
		V_{CC} = 1.65 V to 1.95 V	-	3.0	-	-	-	-	pF
		V_{CC} = 2.3 V to 2.7 V	-	3.6	-	-	-	-	pF
		V_{CC} = 3.0 V to 3.6 V	-	4.2	-	-	-	-	pF

[1] All typical values are measured at nominal V_{CC}.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] t_{en} is the same as t_{PZH} and t_{PZL}.

[4] t_{dis} is the same as t_{PHZ} and t_{PLZ}.

[5] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

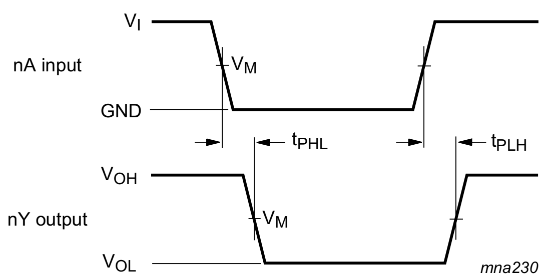
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

12. Waveforms



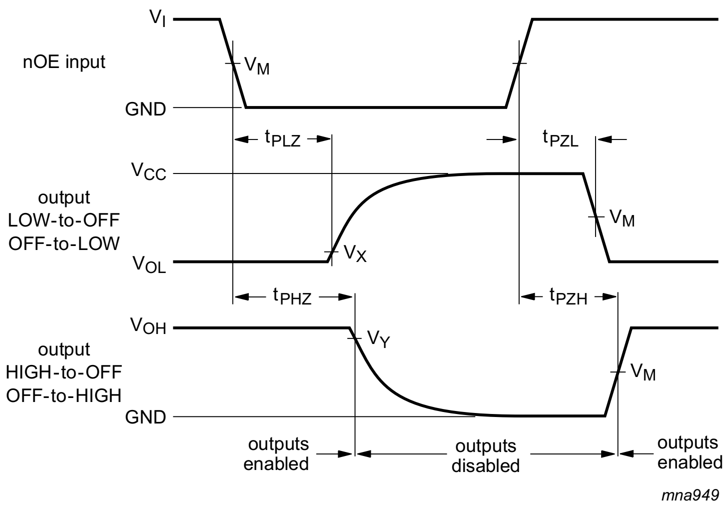
Measurement points are given in Table 9.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 8. The data input (nA) to output (nY) propagation delays

Table 9. Measurement points

Supply voltage	Output	Input		
V_{CC}	V_M	V_M	V_I	$t_r = t_f$
0.8 V to 3.6 V	0.5 × V_{CC}	0.5 × V_{CC}	V_{CC}	≤ 3.0 ns



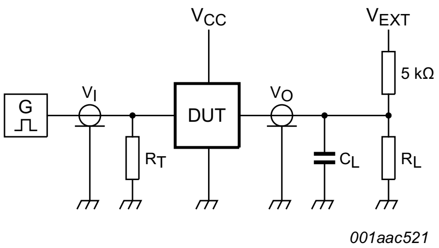
Measurement points are given in Table 10.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 9. Enable and disable times

Table 10. Measurement points

Supply voltage	Input	Output		
V_{CC}	V_M	V_M	V_X	V_Y
0.8 V to 1.6 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	V_{OL} + 0.1 V	V_{OH} − 0.1 V
1.65 V to 2.7 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	V_{OL} + 0.15 V	V_{OH} − 0.15 V
3.0 V to 3.6 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	V_{OL} + 0.3 V	V_{OH} − 0.3 V



Test data is given in Table 11.

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Fig 10. Test circuit for measuring switching times

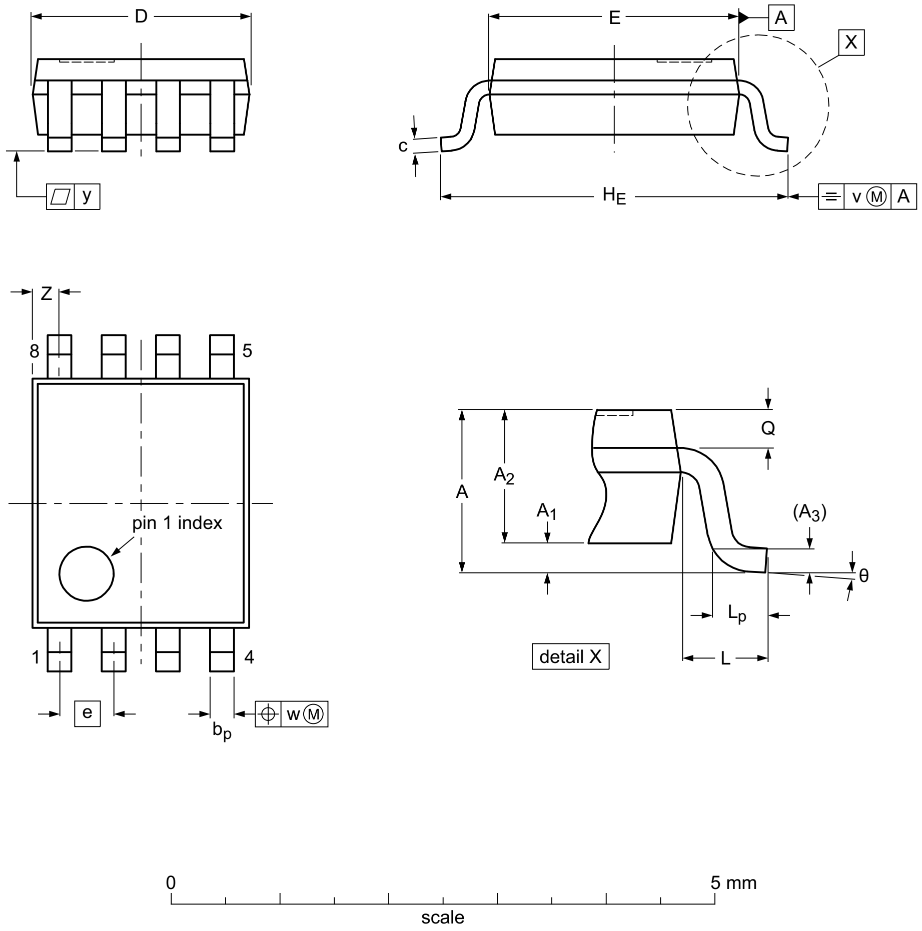
Table 11. Test data

Supply voltage	Load		V_{EXT}		
V_{CC}	C_L	R_L [1]	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
0.8 V to 3.6 V	5 pF, 10 pF, 15 pF and 30 pF	5 kΩ or 1 MΩ	open	GND	2 × V_{CC}

[1] For measuring enable and disable times R_L = 5 kΩ.
For measuring propagation delays, set-up and hold times and pulse width R_L = 1 MΩ.

13. Package outline

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm **SOT765-1**



Dimensions (mm are the original dimensions)

Unit		A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	max		0.15	0.85		0.27	0.23	2.1	2.4		3.2		0.40	0.21				0.4	8°
	nom	1			0.12					0.5		0.4			0.2	0.08	0.1		
	min		0.00	0.60		0.17	0.08	1.9	2.2		3.0		0.15	0.19				0.1	0°

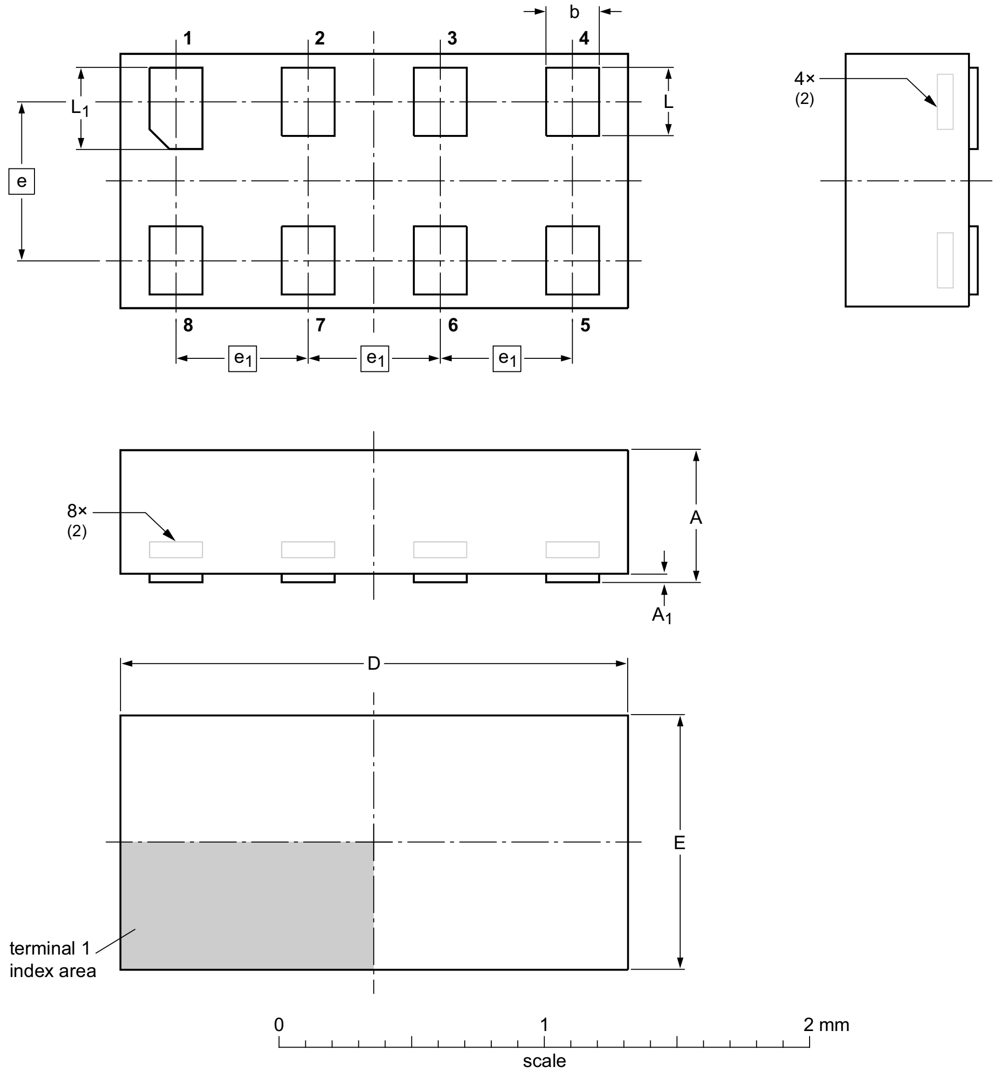
Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

sot765-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT765-1		MO-187				~~07-06-02~~ 16-05-31

Fig 11. Package outline SOT765-1 (VSSOP8)

XSON8: plastic extremely thin small outline package; no leads; 8 terminals; body 1 x 1.95 x 0.5 mm **SOT833-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max	A_1 max	b	D	E	e	e_1	L	L_1
mm	0.5	0.04	0.25 0.17	2.0 1.9	1.05 0.95	0.6	0.5	0.35 0.27	0.40 0.32

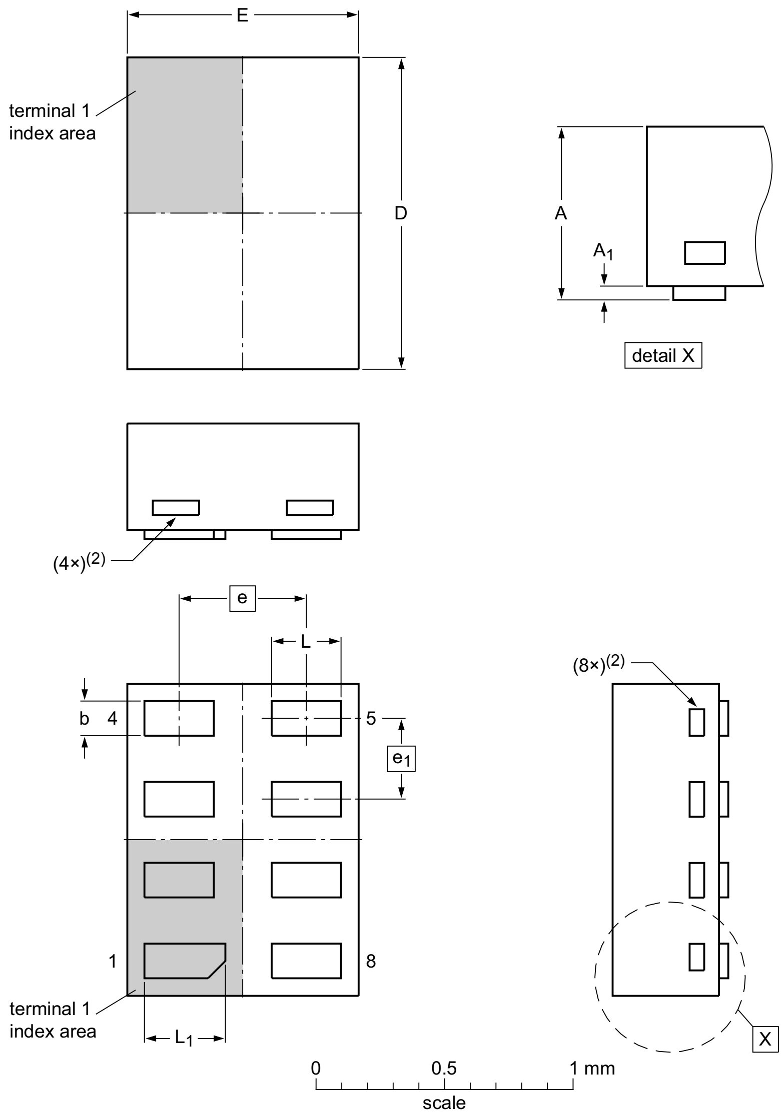
Notes

1. Including plating thickness.
2. Can be visible in some manufacturing processes.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT833-1	- - -	MO-252	- - -			~~07-11-14~~ 07-12-07

Fig 12. Package outline SOT833-1 (XSON8)

XSON8: extremely thin small outline package; no leads; 8 terminals; body 1.35 x 1 x 0.5 mm **SOT1089**



Dimensions

Unit		A(1)	A_1	b	D	E	e	e_1	L	L_1
	max	0.5	0.04	0.20	1.40	1.05			0.35	0.40
mm	nom			0.15	1.35	1.00	0.55	0.35	0.30	0.35
	min			0.12	1.30	0.95			0.27	0.32

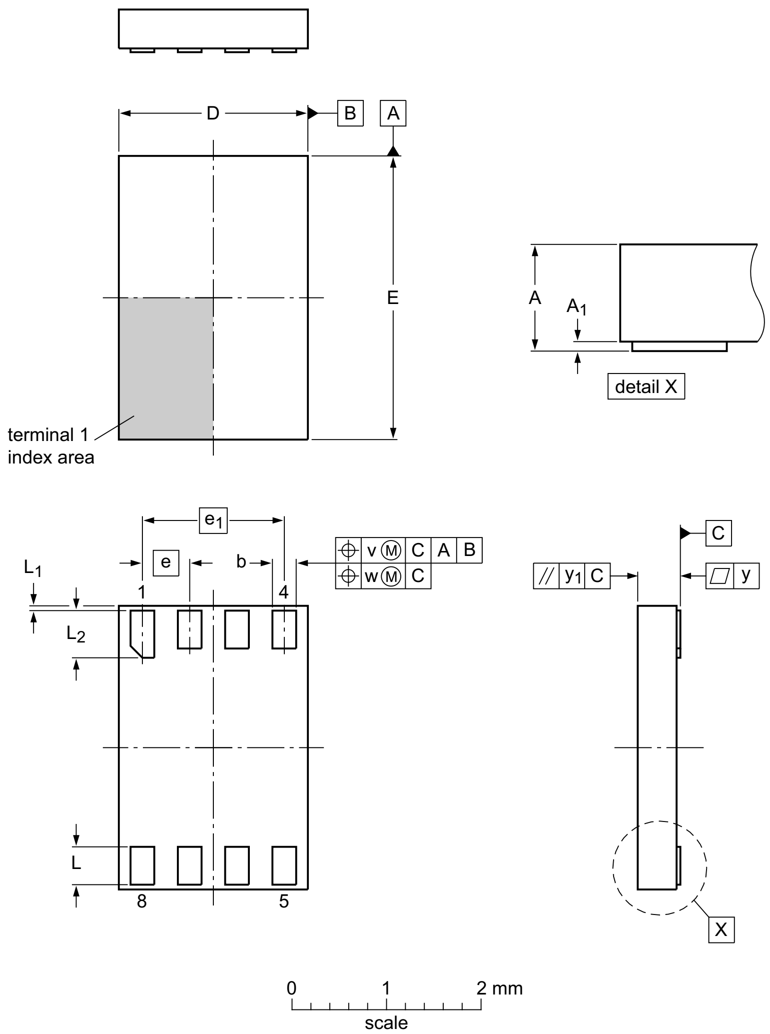
Note
1. Including plating thickness.
2. Visible depending upon used manufacturing technology.

sot1089_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1089		MO-252				~~10-04-09~~ 10-04-12

Fig 13. Package outline SOT1089 (XSON8)

XSON8: plastic extremely thin small outline package; no leads;
8 terminals; body 3 x 2 x 0.5 mm **SOT996-2**



Dimensions (mm are the original dimensions)

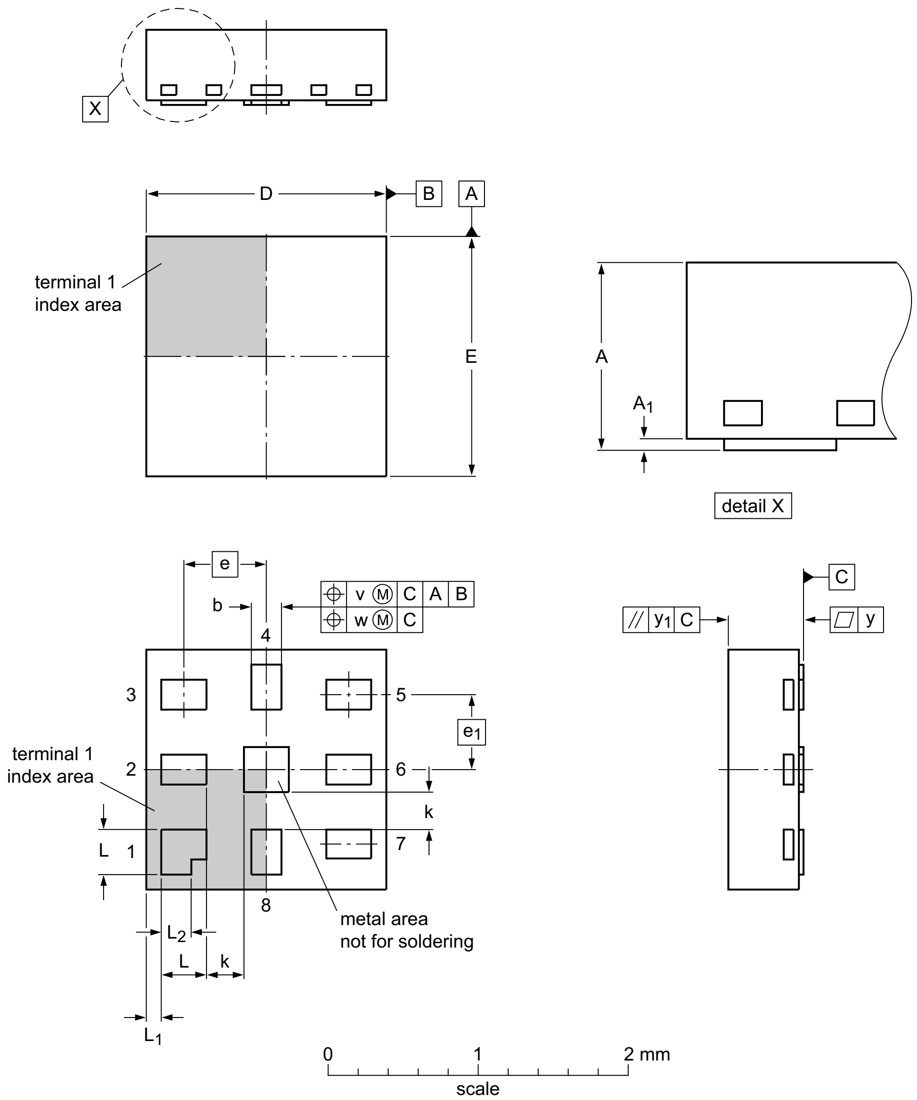
Unit[1]		A	A_1	b	D	E	e	e_1	L	L_1	L_2	v	w	y	y_1
	max		0.05	0.35	2.1	3.1			0.5	0.15	0.6				
mm	nom	0.5					0.5	1.5				0.1	0.05	0.05	0.1
	min		0.00	0.15	1.9	2.9			0.3	0.05	0.4				

sot996-2_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT996-2						~~07-12-21~~ 12-11-20

Fig 14. Package outline SOT996-2 (XSON8)

XQFN8: plastic, extremely thin quad flat package; no leads; 8 terminals; body 1.6 x 1.6 x 0.5 mm **SOT902-2**



Dimensions

Unit[(1)]		A	A_1	b	D	E	e	e_1	k	L	L_1	L_2	v	w	y	y_1
mm	max	0.5	0.05	0.25	1.65	1.65				0.35	0.15	0.25				
	nom			0.20	1.60	1.60	0.55	0.5		0.30	0.10	0.20	0.1	0.05	0.05	0.05
	min		0.00	0.15	1.55	1.55			0.2	0.25	0.05	0.15				

Note

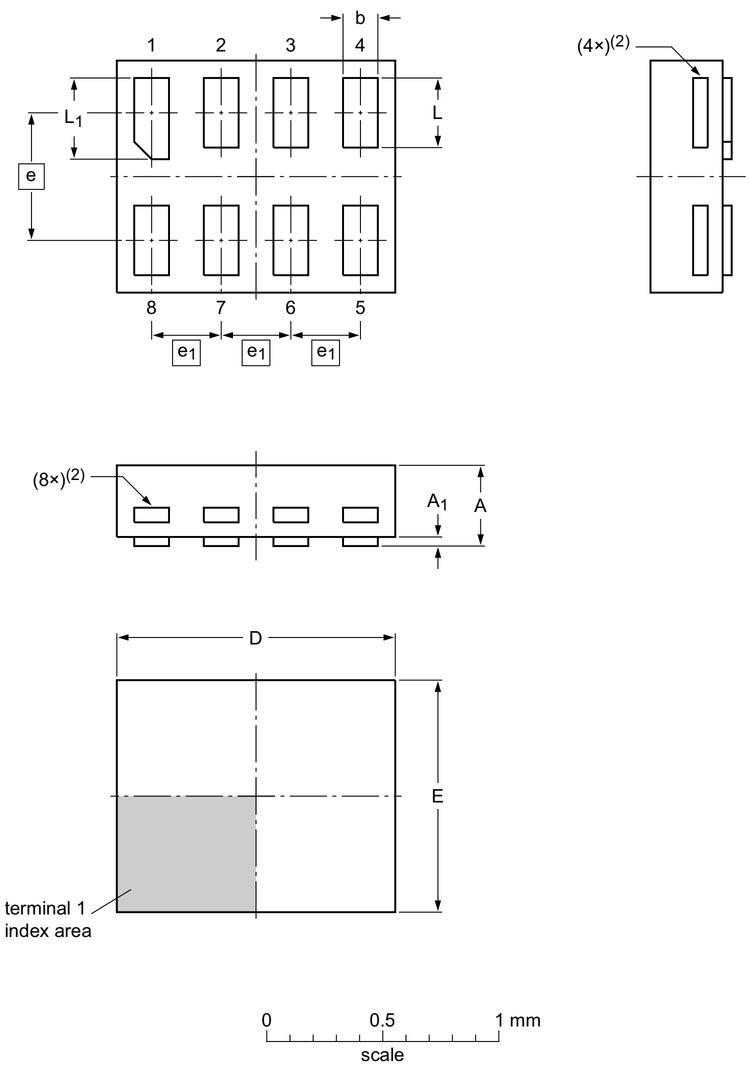
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot902-2_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT902-2	- - -	MO-255	- - -			~~16-07-12~~ 16-07-14

Fig 15. Package outline SOT902-2 (XQFN8)

XSON8: extremely thin small outline package; no leads; 8 terminals; body 1.2 x 1.0 x 0.35 mm **SOT1116**



Dimensions

Unit		A(1)	A_1	b	D	E	e	e_1	L	L_1
mm	max	0.35	0.04	0.20	1.25	1.05			0.35	0.40
	nom			0.15	1.20	1.00	0.55	0.3	0.30	0.35
	min			0.12	1.15	0.95			0.27	0.32

Note

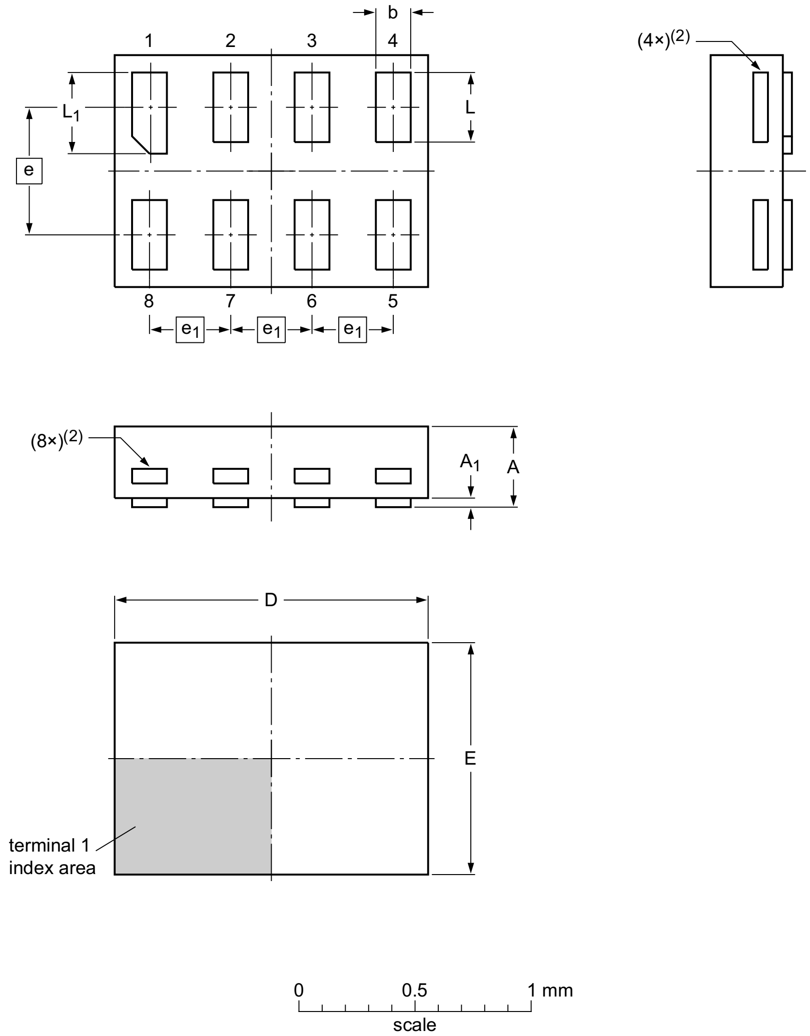
1. Including plating thickness.
2. Visible depending upon used manufacturing technology.

sot1116_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1116						~~10-04-02~~ 10-04-07

Fig 16. Package outline SOT1116 (XSON8)

XSON8: extremely thin small outline package; no leads;
8 terminals; body 1.35 x 1.0 x 0.35 mm **SOT1203**



Dimensions

Unit		$A^{(1)}$	A_1	b	D	E	e	e_1	L	L_1
	max	0.35	0.04	0.20	1.40	1.05			0.35	0.40
mm	nom			0.15	1.35	1.00	0.55	0.35	0.30	0.35
	min			0.12	1.30	0.95			0.27	0.32

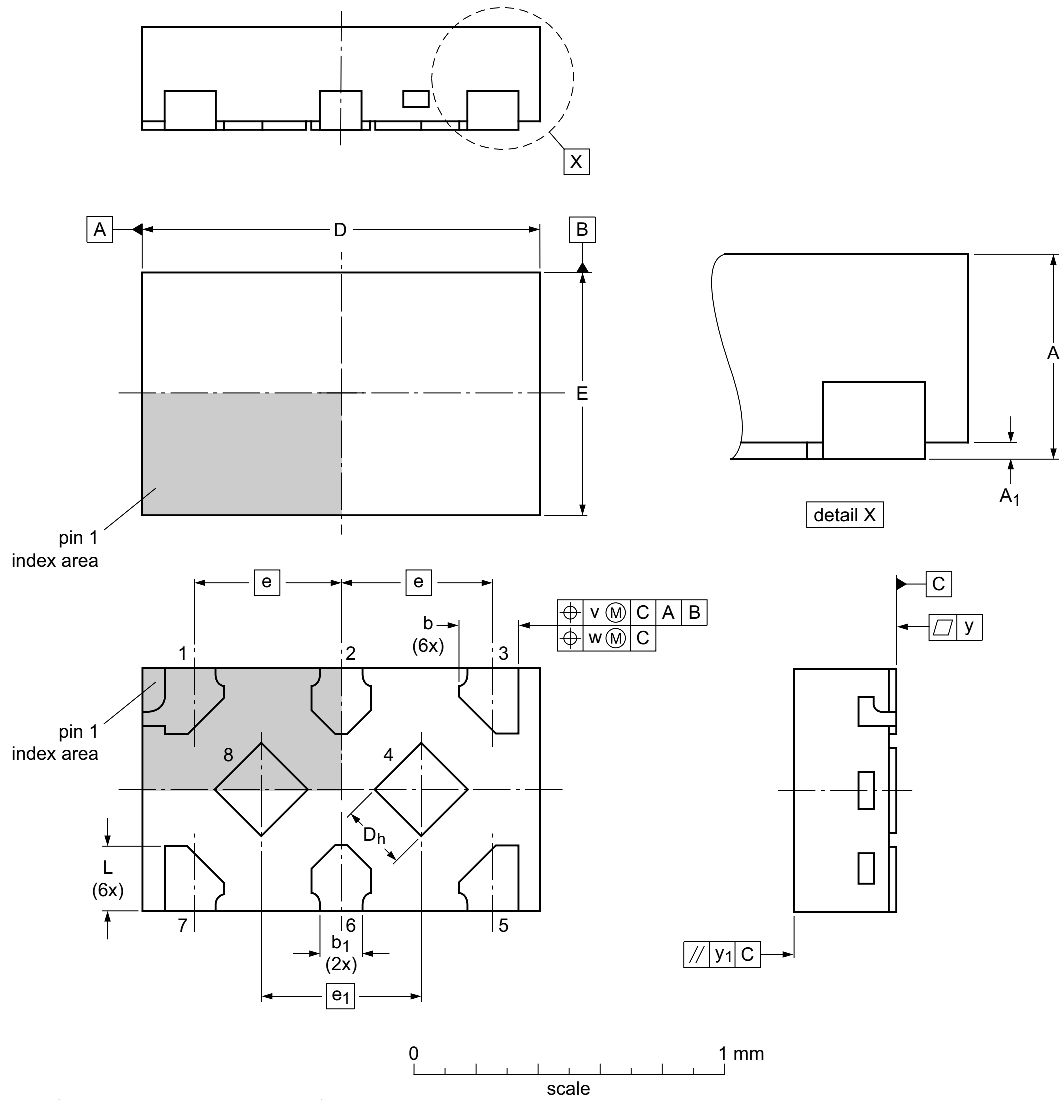
Note
1. Including plating thickness.
2. Visible depending upon used manufacturing technology.

sot1203_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1203						~~10-04-02~~ 10-04-06

Fig 17. Package outline SOT1203 (XSON8)

X2SON8: plastic thermal enhanced extremely thin small outline package; no leads; 8 terminals; body 1.35 x 0.8 x 0.35 mm **SOT1233**



Dimensions (mm are the original dimensions)

Unit		A	A_1	b	b_1	D	D_h	E	e	e_1	L	v	w	y	y_1
	max	0.35	0.04	0.25		1.40	0.27	0.85			0.27				
mm	nom	0.32		0.20	0.15	1.35	0.22	0.80	0.5	0.54	0.22	0.1	0.05	0.05	0.05
	min	0.30	0.00	0.15	(ref)	1.30	0.17	0.75			0.17				

sot1233_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1233		---				~~15-04-30~~ 16-04-21

Fig 18. Package outline SOT1233 (X2SON8)

14. Abbreviations

Table 12. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

15. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AUP2G126 v.10	20161028	Product data sheet	-	74AUP2G126 v.9
Modifications:	• Added type number 74AUP2G126GX (SOT1233/X2SON8)			
74AUP2G126 v.9	20130211	Product data sheet	-	74AUP2G126 v.8
Modifications:	• For type number 74AUP2G126GD XSON8U has changed to XSON8.			
74AUP2G126 v.8	20120606	Product data sheet	-	74AUP2G126 v.7
74AUP2G126 v.7	20111201	Product data sheet	-	74AUP2G126 v.6
74AUP2G126 v.6	20100621	Product data sheet	-	74AUP2G126 v.5
74AUP2G126 v.5	20090202	Product data sheet	-	74AUP2G126 v.4
74AUP2G126 v.4	20090114	Product data sheet	-	74AUP2G126 v.3
74AUP2G126 v.3	20080409	Product data sheet	-	74AUP2G126 v.2
74AUP2G126 v.2	20070515	Product data sheet	-	74AUP2G126 v.1
74AUP2G126 v.1	20061009	Product data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

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17. Contact information

For more information, please visit: **http://www.nexperia.com**

For sales office addresses, please send an email to: **salesaddresses@nexperia.com**

18. Contents

For more information, please visit: http://www.nexperia.com
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