

PCIe® 3.0 Clock Generator with 4 HCSL Outputs

Product Features

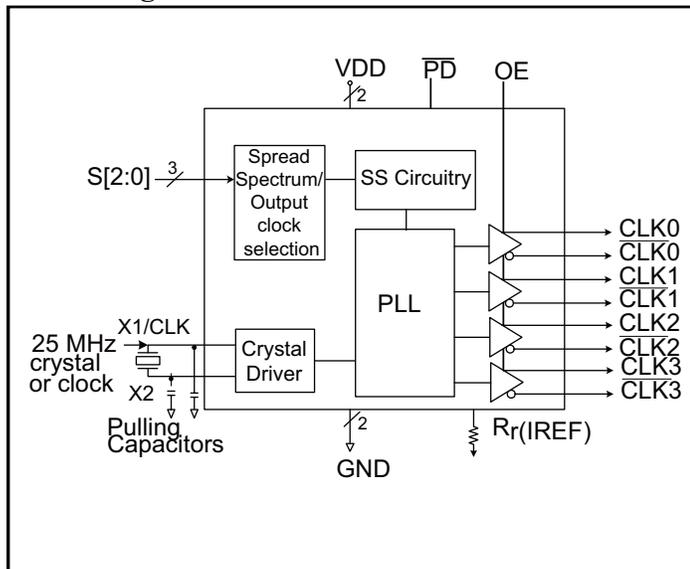
- PCIe® 3.0 compliant
→PCIe 3.0 Phase jitter: 0.48ps RMS (High Freq. Typ.)
- LVDS compatible outputs
- Supply voltage of 3.3V ±5%
- 25MHz crystal or clock input frequency
- HCSL outputs, 0.7V Current mode differential pair
- Jitter 40ps cycle-to-cycle (typ)
- Spread of -0.5%, -1.0%, -1.5%, and no spread
- Industrial temperature range
- Spread Bypass option available
- Spread and frequency selection via external pins
- Packaging: (Pb-free and Green)
→20-pin, 173-mil wide TSSOP

Description

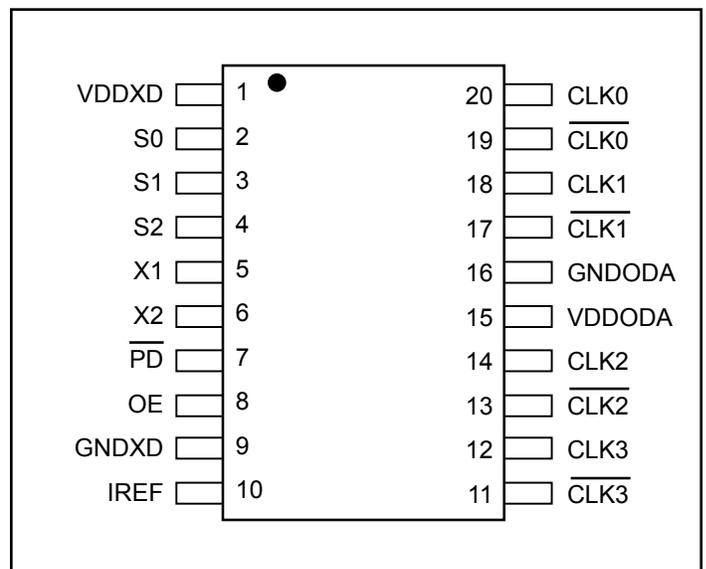
The PI6C557-05B is a spread spectrum clock generator compliant to PCI Express® 3.0 and Ethernet requirements. The device is used for PC or embedded systems to substantially reduce Electromagnetic Interference (EMI).

The PI6C557-05B provides four differential (HCSL) or LVDS spread spectrum outputs. The PI6C557-05B is configured to select spread and clock selection. Using Pericom's patented Phase-Locked Loop (PLL) techniques, the device takes a 25MHz crystal input and produces four pairs of differential outputs (HCSL) at 100MHz and 200MHz clock frequencies. It also provides spread selection of -0.5%, -1.0%, -1.5%, and no spread.

Block Diagram



Pin Configuration



Pin Description

| Pin # | Pin Name | I/O Type | Description |
|-------|--------------------------|----------|--|
| 1 | VDDXD | Power | Connect to a +3.3V source. |
| 2 | S0 | Input | Spread Spectrum Select pin #0. See Spread Spectrum Select table. Internal pull-up resistor. |
| 3 | S1 | Input | Spread Spectrum Select pin #1. See Spread Spectrum Select table. Internal pull-up resistor. |
| 4 | S2 | Input | Spread Spectrum Select pin #2. See Spread Spectrum Select table. Internal pull-up resistor. |
| 5 | X1 | Input | Crystal connection. |
| 6 | X2 | Output | Crystal connection. |
| 7 | $\overline{\text{PD}}$ | Input | Power down. Internal pull-up resistor. |
| 8 | OE | Input | Output enable. Tri-states output (High=enable outputs); Low=disable outputs). Internal pull-up resistor. |
| 9 | GND | Power | Connect to digital circuit ground. |
| 10 | IREF | Output | Precision resistor attached to this pin is connected to the internal current reference. |
| 11 | $\overline{\text{CLK3}}$ | Output | Selectable 100/200 MHz Spread Spectrum differential complement output clock 3. |
| 12 | CLK3 | Output | Selectable 100/200 MHz Spread Spectrum differential true output clock 3. |
| 13 | $\overline{\text{CLK2}}$ | Output | Selectable 100/200 MHz Spread Spectrum differential complement output clock 2. |
| 14 | CLK2 | Output | Selectable 100/200 MHz Spread Spectrum differential true output clock 2. |
| 15 | VDDODA | Power | Connect to a +3.3V analog source. |
| 16 | GND | Power | Output and Analog circuit ground |
| 17 | $\overline{\text{CLK1}}$ | Output | Selectable 100/200 MHz Spread Spectrum differential complement output clock 1. |
| 18 | CLK1 | Output | Selectable 100/200 MHz Spread Spectrum differential true output clock 1. |
| 19 | $\overline{\text{CLK0}}$ | Output | Selectable 100/200 MHz Spread Spectrum differential complement output clock 0. |
| 20 | CLK0 | Output | Selectable 100/200 MHz Spread Spectrum differential true output clock 0. |

Table 2: Spread Selection Table

| S2 | S1 | S0 | Spread % | Spread Type | Output Frequency |
|----|----|----|-----------|----------------|------------------|
| 0 | 0 | 0 | -0.5 | Down | 100 |
| 0 | 0 | 1 | -1.0 | Down | 100 |
| 0 | 1 | 0 | -1.5 | Down | 100 |
| 0 | 1 | 1 | No Spread | Not Applicable | 100 |
| 1 | 0 | 0 | -0.5 | Down | 200 |
| 1 | 0 | 1 | -1.0 | Down | 200 |
| 1 | 1 | 0 | -1.5 | Down | 200 |
| 1 | 1 | 1 | No Spread | Not Applicable | 200 |

Application Information

Decoupling Capacitors

Decoupling capacitors of 0.01 μ F or 0.1 μ F must be connected between each VDD pin and the PCB ground plane and placed as close to the VDD pin as possible.

PI6C557-05B must be isolated from system power supply noise to perform optimally.

Crystal

Use a 25MHz fundamental mode parallel resonant crystal with less than 30PPM of error across temperature.

Current Source (Iref) Reference Resistor - R_R

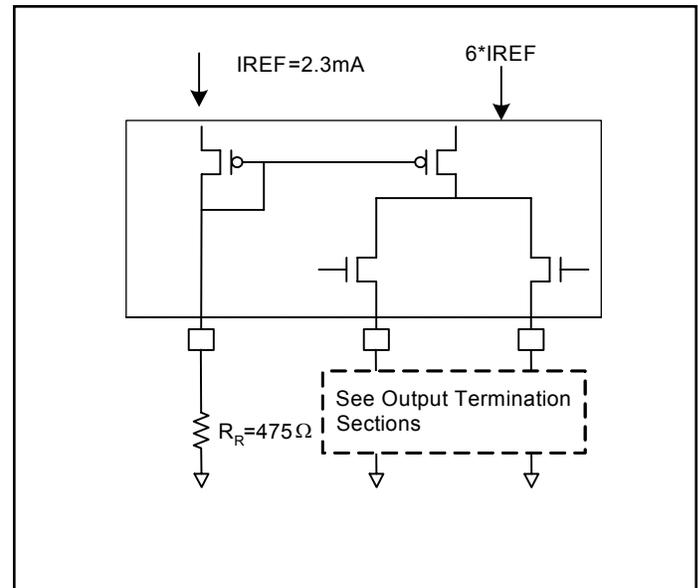
If board target trace impedance is 50-Ohm, then $R_R = 475$ -Ohm providing an IREF of 2.32 mA. The output current (I_{OH}) is 6*IREF.

Output Termination

The PCI-Express differential clock outputs of the PI6C557-05B are open source drivers and require an external series resistor and a resistor to ground. These resistor values and their allowable locations are shown in detail in the PCI-Express Layout Guidelines section.

The PI6C557-05B can be configured for LVDS compatible voltage levels. See the LVDS Compatible Layout Guidelines section.

Output Structures



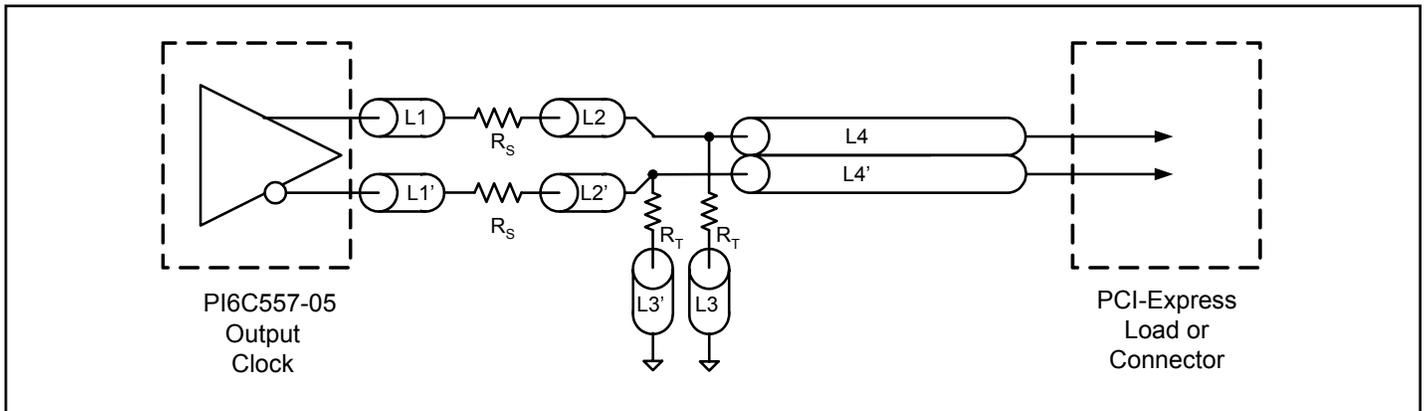
PCI-Express Layout Guidelines

| Common Recommendations for Differential Routing | Dimension or Value | Unit |
|---|--------------------|------|
| L1 length, route as non-coupled 50-Ohm trace. | 0.5 max | inch |
| L2 length, route as non-coupled 50-Ohm trace. | 0.2 max | inch |
| L3 length, route as non-coupled 50-Ohm trace. | 0.2 max | inch |
| R_S | 33 | Ohm |
| R_T | 49.9 | Ohm |

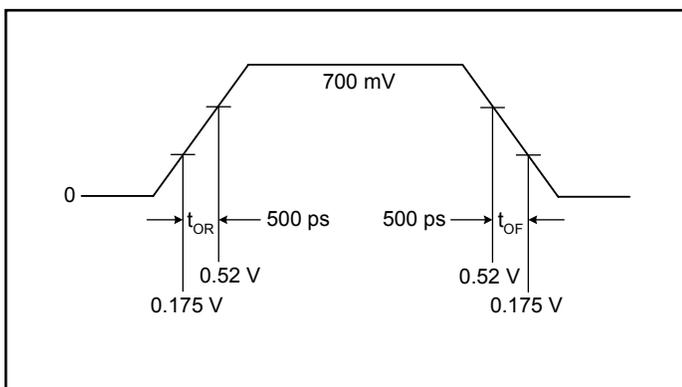
| Differential Routing on a Single PCB | Dimension or Value | Unit |
|--|---------------------|------|
| L4 length, route as coupled microstrip 100-Ohm differential trace. | 2 min to 16 max | inch |
| L4 length, route as coupled stripline 100-Ohm differential trace. | 1.8 min to 14.4 max | inch |

| Differential Routing to a PCI Express connector | Dimension or Value | Unit |
|--|-----------------------|------|
| L4 length, route as coupled microstrip 100-Ohm differential trace. | 0.25 min to 14 max | inch |
| L4 length, route as coupled stripline 100-Ohm differential trace. | 0.225 min to 12.6 max | inch |

PCI-Express Device Routing



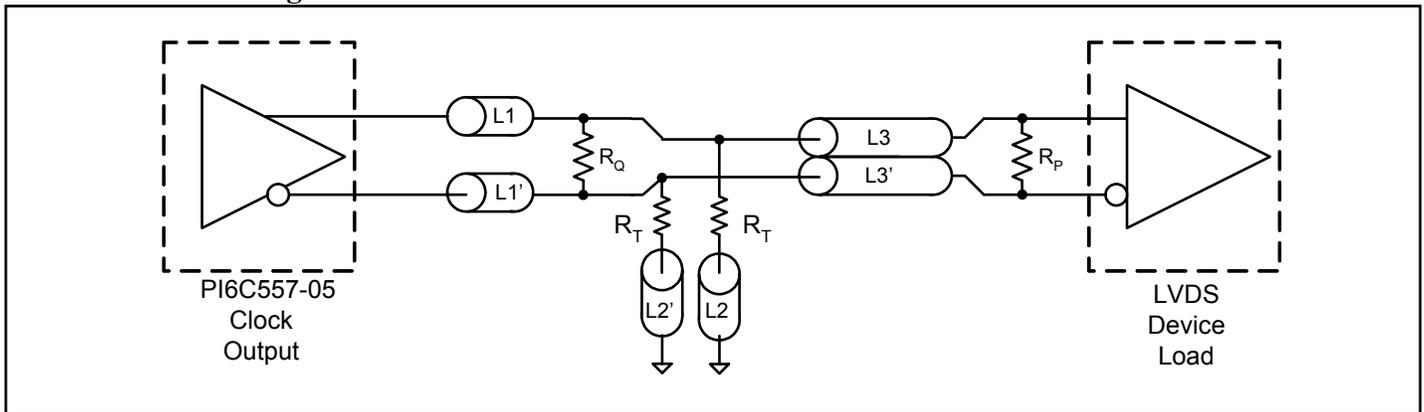
Typical PCI-Express (HCSL) Waveform



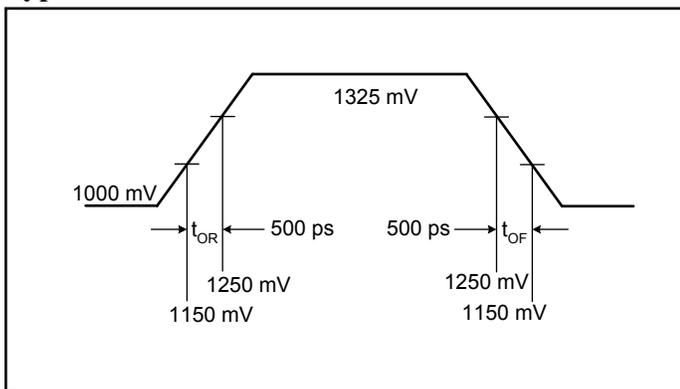
Application Information

| LVDS Recommendations for Differential Routing | Dimension or Value | Unit |
|---|--------------------|------|
| L1 length, route as non-coupled 50-Ohm trace. | 0.5 max | inch |
| L2 length, route as non-coupled 50-Ohm trace. | 0.2 max | inch |
| R_p | 100 | Ohm |
| R_Q | 100 | Ohm |
| R_T | 150 | Ohm |
| L3 length, route as 100Ω differential trace. | | |
| L3 length, route as 100Ω differential trace. | | |

LVDS Device Routing



Typical LVDS Waveform



Electrical Specifications

Maximum Ratings

| | |
|---|--------------------------------|
| Supply Voltage to Ground Potential..... | 5.5V |
| All Inputs and Outputs..... | -0.5V to V _{DD} +0.5V |
| Ambient Operating Temperature | -40 to +80°C |
| Storage Temperature | -65 to +150°C |
| Junction Temperature | 150°C |
| Soldering Temperature | 260°C |
| ESD Protection (Input) | 2000 V min (HBM) |

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operation Conditions

| Parameter | Min. | Typ. | Max. | Unit |
|---|-------|------|-------|------|
| Ambient Operating Temperature | -40 | | +85 | °C |
| Power Supply Voltage (measured in respect to GND) | 3.135 | | 3.465 | V |

DC Characteristics (V_{DD} = 3.3V ±5%, T_A = -40°C to +85°C)

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|-------------------|-----------------------------------|--|----------|------|----------------------|------|
| V _{DD} | Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| V _{IH} | Input High Voltage ⁽¹⁾ | | 2.0 | | V _{DD} +0.3 | V |
| V _{IL} | Input Low Voltage ⁽¹⁾ | | GND -0.3 | | 0.8 | V |
| I _{IL} | Input Leakage Current | 0 < V _{in} < V _{DD} Without input pull-up and pull-downs | -5 | | 5 | μA |
| I _{DD} | Operating Supply Current | R _L = 50Ω, C _L = 2pF @100MHz | | 105 | 120 | mA |
| I _{DDOE} | | OE = LOW | | 40 | 50 | mA |
| I _{DDPD} | | No load $\overline{\text{PD}}$ = LOW | | 60 | 100 | μA |
| C _{IN} | Input Capacitance | Input pin capacitance | | | 7 | pF |
| C _{OUT} | Output Capacitance | Output pin capacitance | | | 6 | pF |
| L _{PIN} | Pin Inductance | | | | 5 | nH |
| R _{OUT} | Output Resistance | CLK Outputs | 3.0 | | | kΩ |

Note:

- Single edge is monotonic when transitioning through region.

AC Characteristics (V_{DD} = 3.3V ±5%, T_A = -40°C to +85°C)

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|------------------|---|--------------------------|------|------|------|------|
| F _{IN} | Input Frequency | | | 25 | | MHz |
| V _{OUT} | Output Frequency | HCSL terminal | | | 200 | MHz |
| | | LVDS terminal | | | 100 | |
| V _{OH} | Output High Voltage ^(1,2) | @V _{DD} = 3.3V | 660 | 700 | 850 | mV |
| V _{OL} | Output Low Voltage ^(1,2) | | -150 | 0 | 27 | mV |
| V _{CPA} | Crossing Point Voltage ^(1,2) | Absolute | 250 | 350 | 550 | mV |
| V _{CN} | Crossing Point Voltage ^(1,2,4) | Variation over all edges | | | 140 | mV |
| J _{CC} | Jitter, Cycle-to-Cycle ^(1,3) | | | 40 | 60 | ps |

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|-------------------------|------------------------------------|------------------------------------|------|------|------|------|
| J _{RMS2.0} | PCIe 2.0 RMS Jitter | PCI-SIG jitter test method | | | 3.1 | ps |
| J _{RMS3.0} | PCIe 3.0 RMS Jitter | PLL L-BW @ 2M & 5M 1st H3 | | 2.1 | 3 | ps |
| | | PLL L-BW @ 2M & 4M 1st H3 | | 2.38 | 3 | ps |
| | | PLL H-BW @ 2M & 5M 1st H3 | | 0.48 | 1 | ps |
| | | PLL H-BW @ 2M & 4M 1st H3 | | 0.47 | 1 | ps |
| MF | Modulation Frequency | Spread Spectrum | 30 | 31.5 | 33 | kHz |
| t _{OR} | Rise Time ^(1,2) | From 0.175V to 0.525V | 175 | 332 | 700 | ps |
| t _{OF} | Fall Time ^(1,2) | From 0.525V to 0.175V | 175 | 344 | 700 | ps |
| T _{SKEW} | Skew between outputs | At Crossing Point Voltage | | | 50 | ps |
| T _{DUTY-CYCLE} | Duty Cycle ^(1,3) | | 45 | | 55 | % |
| T _{OE} | Output Enable Time ⁽⁵⁾ | All outputs | | | 10 | μs |
| T _{OT} | Output Disable Time ⁽⁵⁾ | All outputs | | | 10 | μs |
| t _{STABLE} | From power-up to VDD=3.3V | From Power-up VDD=3.3V | | 3.0 | | ms |
| t _{SPREAD} | Setting period after spread change | Setting period after spread change | | 3.0 | | ms |

Notes:

1. R_L = 50-Ohm with C_L = 2 pF and R_R
2. Single-ended waveform
3. Differential waveform
4. Measured at the crossing point
5. CLK pins are tri-stated when OE is LOW

Thermal Characteristics

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|-----------------|--|------------|------|------|------|------|
| θ _{JA} | Thermal Resistance Junction to Ambient | Still air | | | 93 | °C/W |
| θ _{JC} | Thermal Resistance Junction to Case | | | | 20 | °C/W |

Recommended Crystal Specification

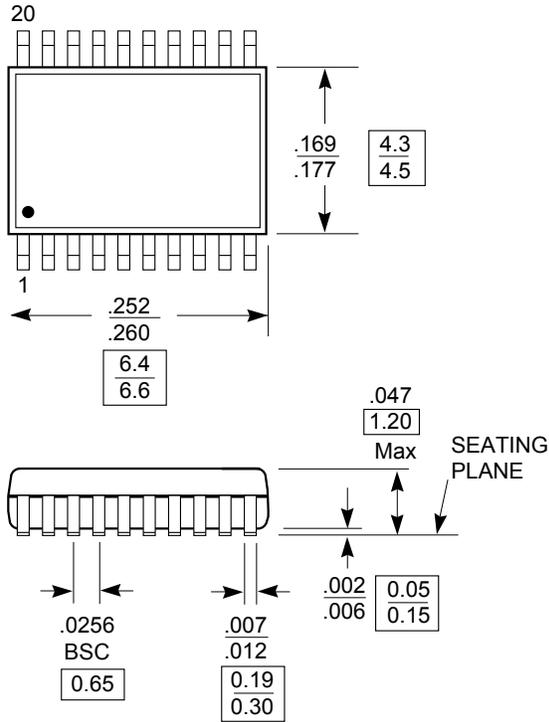
Pericom recommends:

- a) GC2500003 XTAL 49S/SMD(4.0 mm), 25M, CL=18pF, +/-30ppm
http://www.pericom.com/pdf/datasheets/se/GC_GF.pdf
- b) FY2500081, SMD 5x3.2(4P), 25M, CL=18pF, +/-30ppm
http://www.pericom.com/pdf/datasheets/se/FY_F9.pdf
- c) FL2500047, SMD 3.2x2.5(4P), 25M, CL=18pF, +/-20ppm
<http://www.pericom.com/pdf/datasheets/se/FL.pdf>

Packaging Mechanical: 20-pin TSSOP (L)

DOCUMENT CONTROL NO.
PD - 1311

REVISION: E
DATE: 03/09/05



- Note:**
1. Package Outline Exclusive of Mold Flash and Metal Burr
 2. Controlling dimensions in millimeters
 3. Ref: JEDEC MO-153F/AC



Pericom Semiconductor Corporation
3545 N. 1st Street, San Jose, CA 95134
1-800-435-2336 • www.pericom.com

DESCRIPTION: 20-Pin, 173-Mil Wide, TSSOP

PACKAGE CODE: L

Ordering Information(1-3)

| Ordering Code | Package Code | Package Type |
|---------------|--------------|-------------------------------|
| PI6C557-05BLE | L | Pb-free & Green, 20-Pin TSSOP |

Note:

1. Thermal characteristics and package top marking information can be found at <http://www.pericom.com/packaging/>
2. E = lead-free and green packaging
3. Adding an X suffix = tape/reel