SL23EP05

Low Jitter and Skew 10 to 220 MHz Zero Delay Buffer (ZDB)

Key Features

- 10 to 220 MHz operating frequency range
- Low output clock jitter:
  - 20 ps-typ cycle-to-cycle jitter
  - 15 ps-typ period jitter
- Low output-to-output skew: 30 ps-typ
- Low product-to-product skew: xx ps-typ
- Wide 2.5 V to 3.3 V power supply range
- Low power dissipation:
  - 12 mA-typ at 66 MHz and VDD=3.3 V
  - 10 mA-typ at 66 MHz and VDD=2.5V
- One input drives 5 outputs organized as 4+1
- SpreadThru™ PLL that allows use of SSCG
- Standard and High-Drive options
- Available in 150 mil 8-pin SOIC package
- Available in Commercial and Industrial grades

Applications

- Printers and MFPs
- Digital Copiers
- PCs and Work Stations
- Routers, Switchers and Servers
- Digital Embeded Systems

Description

The SL23EP05 is a low skew, low jitter and low power Zero Delay Buffer (ZDB) designed to produce up to five (5) clock outputs from one (1) reference input clock for high speed clock distribution applications. The product has an on-chip PLL which locks to the input clock at CLKIN and receives its feedback internally from the CLKOUT pin.

The SL23EP05 is available with two (2) drive strength versions called -1 and -1H. The -1 is the standard-drive version and -1H is the high-drive version.

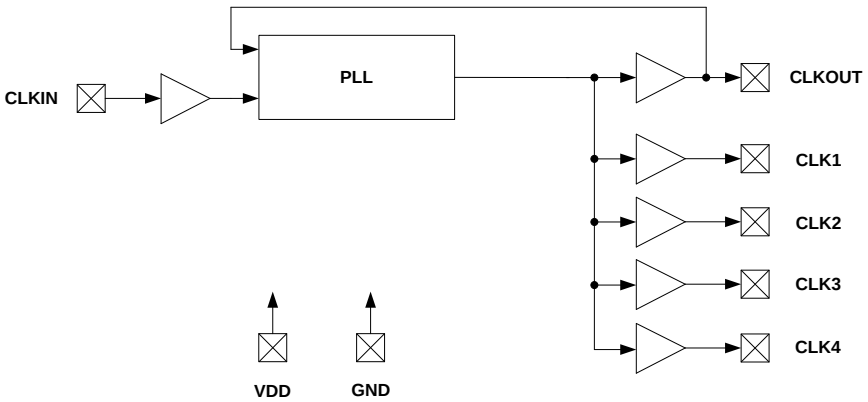
The SL23EP05 high-drive version operates up to 220MHz and 200MHz at 3.3V and 2.5V power supplies respectively. The standard drive version -1 operates up to 167MHz and 133MHz at 3.3V and 2.5V respectively.

The SL23EP05 enter into Power Down (PD) mode if the input at CLKIN is less then 2.0MHz or there is no rising edge. In this state all five (5) outputs are tri-stated and the PLL is turned off leading to less than 25µA of power supply current draw.

Benefits

- Up to five (5) distribution of input clock
- Standard and High-Dirive levels to control impedance level, frequency range and EMI
- Low power dissipation, jitter and skew
- Low cost

Block Diagram



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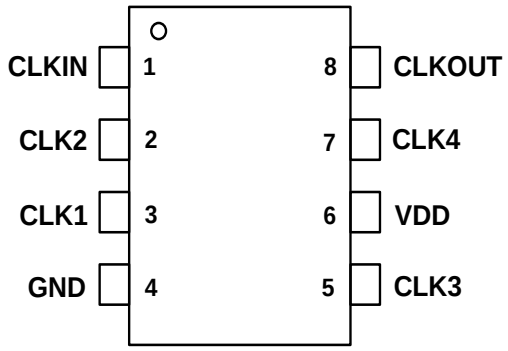
Pin Configuration



8-Pin (150 mil) SOIC

Pin Description

Pin Number	Pin Name	Pin Type	Pin Description
1	CLKIN	Input	Reference Frequency Clock Input. Weak pull-down (150kΩ).
2	CLK2	Output	Buffered Clock Output Weak pull-down (150kΩ).
3	CLK1	Output	Buffered Clock Output. Weak pull-down (150kΩ).
4	GND	Power	Power Ground.
5	CLK3	Output	Buffered Clock Output. Weak pull-down (150kΩ).
6	VDD	Power	3.3V or 2.5V Power Supply.
7	CLK4	Output	Buffered Clock Output. Weak pull-down (150kΩ).
8	CLKOUT	Output	Buffered Clock Output, Used for Internal Feedback to PLL Input. Weak pull-down (150kΩ).

General Description

The SL23EP09 is a low skew, low jitter Zero Delay Buffer with very low operating current.

The product includes an on-chip high performance PLL that locks into the input reference clock and produces nine (9) output clock drivers tracking the input reference clock for systems requiring clock distribution.

in addition to CLKOUT that is used for internal PLL feedback, there are two (2) banks with four (4) outputs in each bank, bringing the number of total available output clocks to nine (9).

Input and output Frequency Range

The input and output frequency range is the same. But, it depends on VDD and drive levels as given in the below Table 1.

VDD(V)	Drive	Min(MHz)	Max(MHz)
3.3	HIGH	10	220
3.3	STD	10	167
2.5	HIGH	10	200
2.5	STD	10	133

Table 1. Input/Output Frequency Range

If the input clock frequency is less than 2 MHz or floating, this is detected by an input frequency detection circuitry and all nine (9) clock outputs are forced to Hi-Z. The PLL is shutdown to save power. In this shutdown state, the product draws less than 25 µA supply current.

SpreadThru™ Feature

If a Spread Spectrum Clock (SSC) were to be used as an input clock, the SL23EP09 is designed to pass the modulated Spread Spectrum Clock (SSC) signal from its reference input to the output clocks. The same spread characteristics at the input are passed through the PLL and drivers without any degradation in spread percent (%), spread profile and modulation frequency.

Select Input Control

The SL23EP09 provides two (2) input select control pins called S1 and S2. This feature enables users to selects various states of output clock banks-A and bank-B, output source and PLL shutdown features as shown in the Table 2.

The S1 (Pin-9) and S2 (Pin-8) inputs include 150 kΩ weak pull-down resistors to GND.

PLL Bypass Mode

If the S1 and S2 pins are logic Low(0) and High(1) respectively, the on-chip PLL is shutdown and bypassed, and all the nine output clocks bank A, bank B and CLKOUT clocks are driven by directly from the reference input clock. In this operation mode SL23EP09 works like a non-ZDB product.

High and Low-Drive Product Options

The SL23EP09 is offered with High-Drive “-1H” and Standard-Drive “-1” options. These drive options enable the users to control load levels, frequency range and EMI control. Refer to the AC electrical tables for the details.

Skew and Zero Delay

All outputs should drive the similar load to achieve output-to-output skew and input-to-output specifications given in the AC electrical tables. However, Zero delay between input and outputs can be adjusted by changing the loading of CLKOUT relative to the banks A and B clocks since CLKOUT is the feedback to the PLL.

Power Supply Range (VDD)

The SL23EP09 is designed to operate in a wide power supply range from 2.250V (Min) to 3.360V (Max). This power supply range complies with 3.3V+/-10% and 2.5V+/-10% standard power supply requirements used in most systems. An internal on-chip voltage regulator is used to supply PLL constant power supply of 1.8V, leading to a consistent and stable PLL electrical performance in terms of skew, jitter and power dissipation. Contact SLI for 1.8V power supply version ZDB called SL23EPL09.

Absolute Maximum Ratings

Description	Condition	Min.	Max.	Unit
Supply voltage, VDD		– 0.5	4.6	V
All Inputs and Outputs		– 0.5	VDD+0.5	V
Ambient Operating Temperature	In operation, C-Grade	0	70	°C
Ambient Operating Temperature	In operation, I-Grade	– 40	85	°C
Storage Temperature	No power is applied	– 65	150	°C
Junction Temperature	In operation, power is applied	–	125	°C
Soldering Temperature		–	260	°C
ESD Rating (Human Body Model)	MIL-STD-883, Method 3015	2000	–	V

Operating Conditions: Unless otherwise stated VDD=2.5V to 3.3V and for both C and I Grades

Symbol	Description	Condition	Min.	Max.	Unit
VDD3.3	3.3V Supply Voltage		3.0	3.6	V
VDD2.5	2.5V Supply Voltage		2.3	2.7	V
TA	Operating Temperature(Ambient)	Commercial	0	70	°C
		Industrial	–40	85	°C
CLOAD	Load Capacitance	<100 MHz, 3.3V	–	30	pF
		<100 MHz, 2.5V with High drive	–	30	pF
		<133.3 MHz, 3.3V	–	22	pF
		<133.3 MHz, 2.5V with High drive	–	22	pF
		<133.3 MHz, 2.5V with Standard drive	–	15	pF
		>133.3 MHz, 3.3V	–	15	pF
		>133.3 MHz, 2.5V with High drive	–	15	pF
CIN	Input Capacitance	CLKIN pin	–	5	pF
CLBW	Closed-loop bandwidth	3.3V, (typical)	1-1.5		MHz
		2.5V, (typical)	0.8		MHz
ZOUT	Output Impedance	3.3V, (typical), High drive	29		Ω
		3.3V, (typical), Standard drive	41		Ω
		2.5V, (typical), High drive	37		Ω
		2.5V, (typical), Standard drive	41		Ω

DC Electrical Specifications (VDD=3.3V): Unless otherwise stated for both C and I Grades

Symbol	Description	Condition	Min.	Max.	Unit
VDD	Supply Voltage		3.0	3.6	V
VIL	Input LOW Voltage		–	0.8	V
VIH	Input HIGH Voltage		2.0	V_{DD}+0.3	V
IIL	Input Leakage Current	0 < VIN < 0.8V	–	±10	µA
IIH	Input HIGH Current	VIN = VDD	–	100	µA
VOL	Output LOW Voltage	IOL = 8 mA (standard drive)	–	0.4	V
		IOL = 12 mA (high drive)	–	0.4	V
VOH	Output HIGH Voltage	IOH = –8 mA (standard drive)	2.4	–	V
		IOH = –12 mA (high drive)	2.4	–	V
IDDPD	Power Down Supply Current	CLKIN = 0 MHz (Commercial)	–	12	µA
		CLKIN = 0 MHz (Industrial)	–	25	µA
IDD	Power Supply Current	All Outputs CL=0, 66-MHz CLKIN	–	12	mA

DC Electrical Specifications (VDD=2.5V): Unless otherwise stated for both C and I Grades

Symbol	Description	Condition	Min.	Max.	Unit.
VDD	Supply Voltage		2.3	2.7	V
VIL	Input LOW Voltage		–	0.7	V
VIH	Input HIGH Voltage		1.7	V_{DD}+ 0.3	V
IIL	Input Leakage Current	0<VIN < 0.8V	–	+/-10	µA
IIH	Input HIGH Current	VIN = VDD	–	100	µA
VOL	Output LOW Voltage	IOL = 8 mA (Standard drive)	–	0.5	V
		IOL = 12 mA (High drive)	–	0.5	V
VOH	Output HIGH Voltage	IOH = –8 mA (Standard drive)	V_{DD} – 0.6	–	V
		IOH = –12 mA (High drive)	V_{DD} – 0.6	–	V
IDDPD	Power Down Supply Current	CLKIN = 0 MHz (Commercial)	–	12	µA
		CLKIN = 0 MHz (Industrial)	–	25	µA
IDD	Power Supply Current	All Outputs CL=0, 66-MHz CLKIN	–	10	mA

AC Electrical Specifications (VDD=3.3V and 2.5V)

Symbol	Description	Condition	Min	Typ	Max	Unit
FMAX	Maximum Frequency [1] (Input=Output)	3.3V High Drive	10	–	220	MHz
		3.3V Standard Drive	10	–	167	MHz
		2.5V High Drive	10	–	200	MHz
		2.5V Standard Drive	10	–	133	MHz
INDC	Input Duty Cycle	<135 MHz, VDD=3.3V	25	–	75	%
		<135 MHz, VDD=2.5V	40	–	60	%
OUTDC	Output Duty Cycle[2]	<135 MHz, VDD=3.3V	47	–	53	%
		<135 MHz, VDD=2.5V	45		55	%
tr/f3.3	Rise, Fall Time (3.3V) [2] Measured at: 0.8 to 2.0V	Std drive, CL = 30 pF, <100 MHz	–	–	1.6	ns
		Std drive, CL = 22 pF, <135 MHz	–	–	1.6	ns
		Std drive, CL = 15 pF, <170 MHz	–	–	0.6	ns
		High drive, CL = 30 pF, <100 MHz	–	–	1.2	ns
		High drive, CL = 22 pF, <135 MHz	–	–	1.2	ns
		High drive, CL = 15 pF, >135 MHz	–	–	0.5	ns
tr/f2.5	Rise, Fall Time (2.5) [2] Measured at: 0.6 to 1.8V	Std drive, CL = 15 pF, <135 MHz	–	–	1.5	ns
		High drive, CL = 30 pF, <100 MHz	–	–	2.1	ns
		High drive, CL = 22 pF, <135 MHz	–	–	1.3	ns
		High drive, CL = 15 pF, >135 MHz	–	–	1.2	ns
t_1	Output-to-Output Skew [9]	All outputs CL=0, 3.3V supply, 2.5 power supply, standard drive	–	40	90	ps
		All outputs CL=0, 2.5V power supply, high drive	–	–	100	ps
t2	Delay Time, CLKIN Rising Edge to CLKOUT Rising Edge[2]	PLL Bypass mode	1.5	–	4.4	ns
		PLL enabled @ 3.3V	–100	–	100	ps
		PLL enabled @2.5V	–200	–	200	ps
t3	Part-to-Part Skew[2]	Measured at VDD/2. Any output to any output, 3.3V supply	–	–	±150	ps
		Measured at VDD/2. Any output to any output, 2.5V supply	–	–	±300	ps

Notes:

1. For the given maximum loading conditions. See CL in Operating Conditions Table.
2. Parameter is guaranteed by design and characterization. Not 100% tested in production.

AC Electrical Specifications (VDD=3.3V and 2.5V) (cont.)

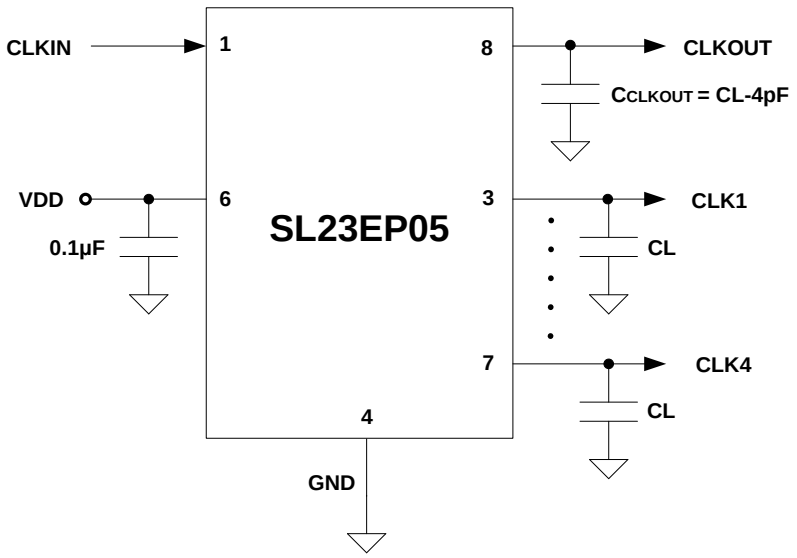
Symbol	Description	Condition	Min	Typ	Max	Unit
tPLLOCK	PLL Lock Time[9]	From 90% of VDD to valid clocks presented on all output clock pins	–	–	1.0	ms
CCJ [2,3]	Cycle-to-cycle Jitter	3.3V supply, >66 MHz, <15 pF	–	20	50	ps
		3.3V supply, >66 MHz, <30 pF, standard drive	–	40	100	ps
		3.3V supply, >66 MHz, <30 pF, high drive	–	40	100	ps
		2.5V supply, >66 MHz, <15 pF, standard drive	–	35	90	ps
		2.5V supply, >66 MHz, <15 pF, high drive	–	30	60	ps
		2.5V supply, >66 MHz, <30 pF, high drive	–	50	125	ps
PPJ [2,3]	Peak Period Jitter	3.3V supply, 66–100 MHz, <15 pF	–	18	50	ps
		3.3V supply, >100 MHz, <15 pF	–	15	35	ps
		3.3V supply, >66 MHz, <30 pF, standard drive	–	30	75	ps
		3.3V supply, >66 MHz, <30 pF, high drive	–	25	60	ps
		2.5V supply, >66 MHz, <15 pF, standard drive	–	25	60	ps
		2.5V supply, 66–100 MHz, <15 pF, high drive	–	20	60	ps
		2.5V supply, >100 MHz, <15 pF, high drive	–	20	45	ps

Notes:

3. Typical jitter is measured at 3.3V or 2.5V, 30°C with all outputs driven into the maximum specified load.

External Components & Design Considerations

Typical Application Schematic



Comments and Recommendations

Decoupling Capacitor: A decoupling capacitor of 0.1µF must be used between VDD and VSS on the pins 6 and 4. Place the capacitor on the component side of the PCB as close to the VDD pin as possible. The PCB trace to the VDD pin and to the GND via should be kept as short as possible. Do not use vias between the decoupling capacitor and the VDD pin.

Series Termination Resistor: A series termination resistor is recommended if the distance between the output (SSCLK) and the load is over 1 ½ inch. The nominal impedance of the SSCLK output is about 30 Ω. Use 20 Ω resistor in series with the output to terminate 50Ω trace impedance and place 20 Ω resistor as close to the clock outputs as possible.

Zero Delay and Skew Control: All outputs and CLKIN pins should be loaded with the same load to achieve “Zero Delay” between the CLKIN and the outputs. The CLKOUT pin is connected to CLKIN internally on-chip for internal feedback to PLL, and sees an additional 4 pF load with respect to the clock pins. For applications requiring zero input/output delay, the load at the all output pins including the CLKOUT pin must be the same. If any delay adjustment is required, the capacitance at the CLKOUT pin could be increased or decreased to increase or decrease the delay between clocks and CLKIN.

For minimum pin-to-pin skew, the external load at the clocks must be the same.

Switching Waveforms

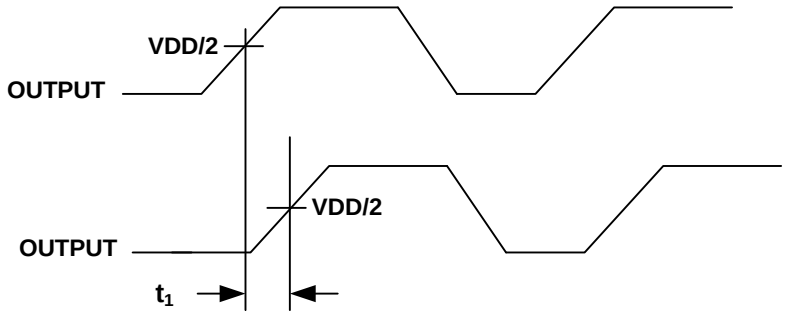


Figure 1. Output to Output Skew

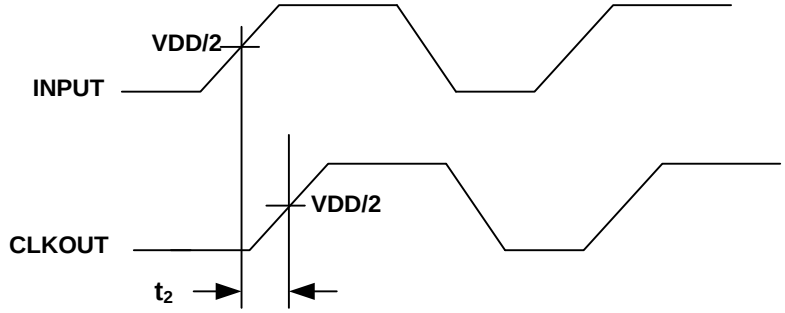


Figure 2. Input to Output Skew

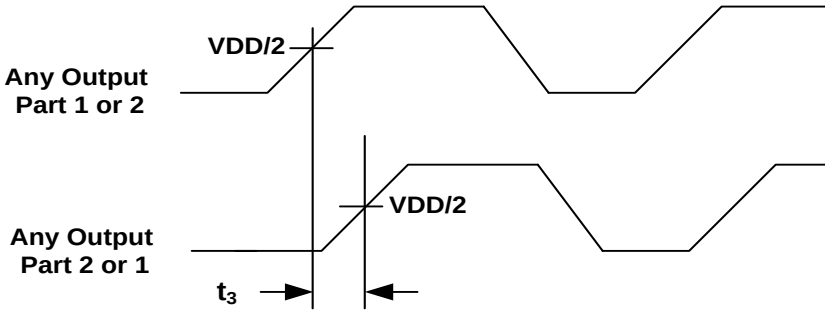
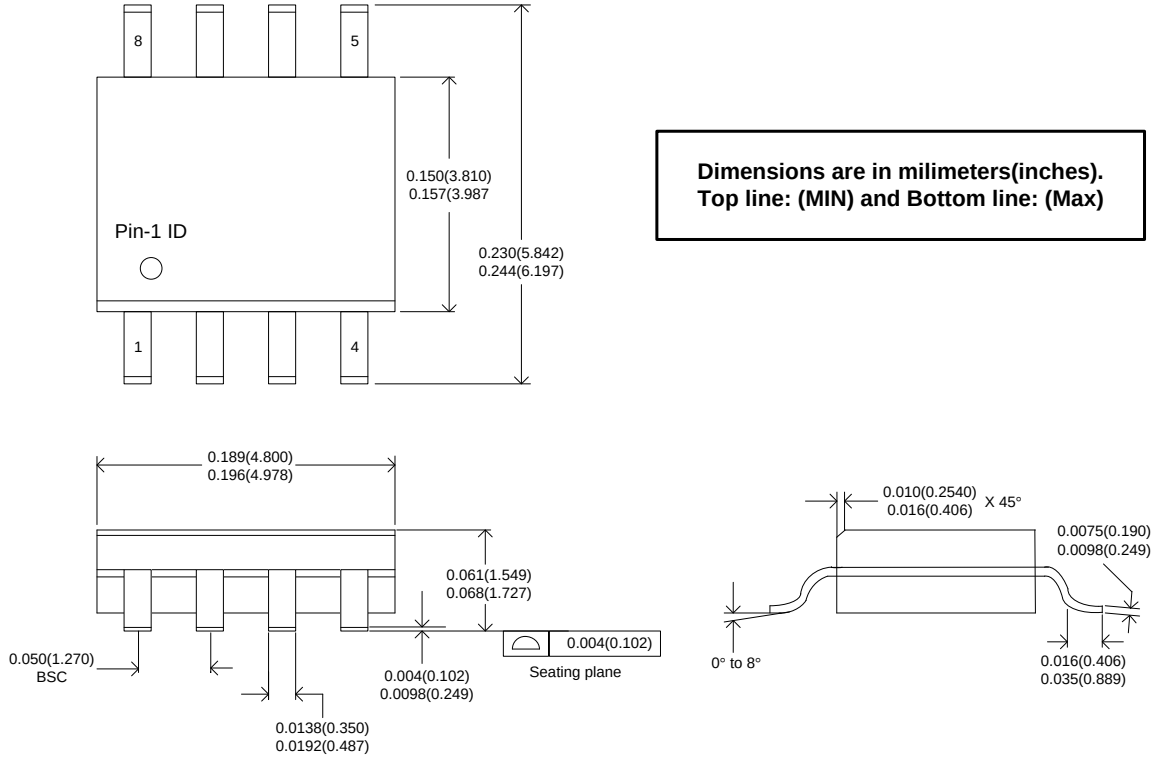


Figure 3. Part-to-Part Skew

Package Drawing and Dimensions

8-Lead SOIC (150 Mil)



Dimensions are in milimeters(inches).
Top line: (MIN) and Bottom line: (Max)

Thermal Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Thermal Resistance Junction to Ambient	θ JA	Still air	-	150	-	°C/W
	θ JA	1m/s air flow	-	140	-	°C/W
	θ JA	3m/s air flow	-	120	-	°C/W
Thermal Resistance Junction to Case	θ JC	Independent of air flow	-	40	-	°C/W

Ordering Information

Ordering Number	Marking	Shipping Package	Package	Temperature	MOQ
SL23EP05CT-1	SL23EP05CT-1	Tube	8-pin SOIC	0 to 70°C	TBD
SL23EP05CT-1R	SL23EP05CT-1	Tape and Reel	8-pin SOIC	0 to 70°C	TBD
SL23EP05IT-1	SL23EP05IT-1	Tube	8-pin SOIC	-40 to 85°C	TBD
SL23EP05IT-1R	SL23EP05IT-1	Tape and Reel	8-pin SOIC	-40 to 85°C	TBD
SL23EP05CT-1H	SL23EP05CT-1H	Tube	8-pin SOIC	0 to 70°C	TBD
SL23EP05CT-1HR	SL23EP05CT-1H	Tape and Reel	8-pin SOIC	0 to 70°C	TBD
SL23EP05IT-1H	SL23EP05IT-1H	Tube	8-pin SOIC	-40 to 85°C	TBD
SL23EP05IT-1HR	SL23EP05IT-1H	Tape and Reel	8-pin SOIC	-40 to 85°C	TBD

Notes:

4. The SL23EP05 products are RoHS compliant.
5. Minimum Order Quantity (MOQ) is for production orders. SLI provides lesser quantities for pre-production samples.