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December 2011

## **FDMQ8203**

# GreenBridge<sup>TM</sup> Series of High-Efficiency Bridge Rectifiers Dual N-Channel and Dual P-Channel PowerTrench<sup>®</sup> MOSFET N-Channel: 100 V, 6 A, 110 m $\Omega$ P-Channel: -80 V, -6 A, 190 m $\Omega$

#### **Features**

Q1/Q4: N-Channel

- Max  $r_{DS(on)}$  = 110 m $\Omega$  at  $V_{GS}$  = 10 V,  $I_D$  = 3 A
- Max  $r_{DS(on)}$  = 175 m $\Omega$  at  $V_{GS}$  = 6 V,  $I_D$  = 2.4 A

Q2/Q3: P-Channel

- Max  $r_{DS(on)}$  = 190 m $\Omega$  at  $V_{GS}$  = -10 V,  $I_D$  = -2.3 A
- Max  $r_{DS(qn)} = 235 \text{ m}\Omega$  at  $V_{GS} = -4.5 \text{ V}$ ,  $I_D = -2.1 \text{ A}$
- Substantial efficiency benefit in PD solutions
- RoHS Compliant

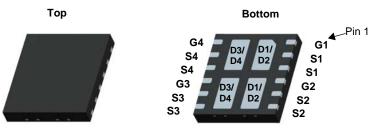


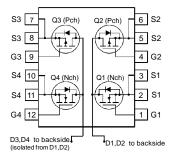
### **General Description**

This quad mosfet solution provides ten-fold improvement in power dissipation over diode bridge.

#### **Application**

■ High-Efficiency Bridge Rectifiers





MLP 4.5x5

## MOSFET Maximum Ratings TA = 25 °C unless otherwise noted

Symbol	Parameter	Parameter				Units
V <sub>DS</sub>	Drain to Source Voltage			100	-80	V
$V_{GS}$	Gate to Source Voltage			±20	±20	V
	Drain Current -Continuous (Package limited)	T <sub>C</sub> = 25 °C		6	-6	
	-Continuous (Silicon limited)	T <sub>C</sub> = 25 °C		10	-10	A
ID	-Continuous	T <sub>A</sub> = 25 °C	(Note 1a)	3.4	-2.6	A
	-Pulsed			12	-10	
Б	Power Dissipation for Single Operation	T <sub>C</sub> = 25 °C		22	37	W
$P_{D}$	Power Dissipation for Dual Operation $T_A = 25 ^{\circ}\text{C}$ (Note 1a)		2	.5	- VV	
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temperature Range	ge		-55 to	+150	°C

#### **Thermal Characteristics**

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	50	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1b)	160	C/ VV

## **Package Marking and Ordering Information**

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMQ8203	FDMQ8203	MLP4.5x5	13 "	12 mm	3000 units

# **Electrical Characteristics** $T_J = 25 \, ^{\circ}\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Тур	Max	Units
Off Chara	cteristics						
BV <sub>DSS</sub>	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$ $I_D = -250 \mu A, V_{GS} = 0 V$	Q1/Q4 Q2/Q3	100 -80			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D$ = 250 μA, referenced to 25 °C $I_D$ = -250 μA, referenced to 25 °C	Q1/Q4 Q2/Q3		72 -79		mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 80 V, V <sub>GS</sub> = 0 V V <sub>DS</sub> = -64 V, V <sub>GS</sub> = 0 V	Q1/Q4 Q2/Q3			1 -1	μ <b>Α</b> μ <b>Α</b>
I <sub>GSS</sub>	Gate to Source Leakage Current	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0 V	Q1/Q4 Q2/Q3			±100 ±100	nA nA

## **On Characteristics**

V <sub>GS(th)</sub>	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu A$ $V_{GS} = V_{DS}, I_D = -250 \mu A$	Q1/Q4 Q2/Q3	2 -1	3 -1.6	4 -3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D$ = 250 μA, referenced to 25 °C $I_D$ = -250 μA, referenced to 25 °C	Q1/Q4 Q2/Q3		-8 5		mV/°C
-	Durin to Course On Decistors	$V_{GS} = 10 \text{ V}, \ I_D = 3 \text{ A}$ $V_{GS} = 6 \text{ V}, \ I_D = 2.4 \text{ A}$ $V_{GS} = 10 \text{ V}, \ I_D = 3 \text{ A}, \ T_J = 125 \text{ °C}$	Q1/Q4		85 118 147	110 175 191	
r <sub>DS(on)</sub>	Drain to Source On Resistance	$V_{GS}$ = -10 V, $I_D$ = -2.3 A $V_{GS}$ = -4.5 V, $I_D$ = -2.1 A $V_{GS}$ = -10 V, $I_D$ = -2.3 A, $T_J$ = 125 °C	Q2/Q3		161 188 273	190 235 323	mΩ
g <sub>FS</sub>	Forward Transconductance	$V_{DS} = 10 \text{ V}, I_D = 3 \text{ A}$ $V_{DS} = -10 \text{ V}, I_D = -2.3 \text{ A}$	Q1/Q4 Q2/Q3		6 6		S

## **Dynamic Characteristics**

C <sub>iss</sub>	Input Capacitance	Q1/Q4: V <sub>DS</sub> = 50 V, V <sub>GS</sub> = 0 V, f = 1 MHZ	Q1/Q4 Q2/Q3	158 639	210 850	pF
C <sub>oss</sub>	Output Capacitance	Q2/Q3:	Q1/Q4 Q2/Q3	41 46	55 65	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	$V_{DS} = -40 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHZ}$	Q1/Q4 Q2/Q3	2.6 24	5 40	pF

## **Switching Characteristics**

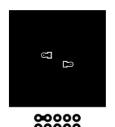
t <sub>d(on)</sub>	Turn-On Delay Time	Q1/Q4:	Q1/Q4 Q2/Q3	3.8 4.7	10 10	ns
t <sub>r</sub>	Rise Time	$V_{DD} = 50 \text{ V}, I_{D} = 3 \text{ A},$ $V_{GS} = 10 \text{ V}, R_{GEN} = 6 \Omega$	Q1/Q4 Q2/Q3	1.3 2.8	10 10	ns
t <sub>d(off)</sub>	Turn-Off Delay Time	Q2/Q3: V <sub>DD</sub> = -40 V, I <sub>D</sub> = -2.3 A,	Q1/Q4 Q2/Q3	7.5 22	15 35	ns
t <sub>f</sub>	Fall Time	$V_{GS} = -10 \text{ V}, R_{GEN} = 6 \Omega$	Q1/Q4 Q2/Q3	1.9 2.7	10 10	ns
Qg	Total Gate Charge	VGS = 0 V to 10 V VGS = 0 V to -10 V Q1/Q4:	Q1/Q4 Q2/Q3	2.9 13	5 19	nC
Q <sub>g</sub>	Total Gate Charge	VGS = 0 V to 5 V VGS = 0 V to -4.5 V I <sub>D</sub> = 3 A	Q1/Q4 Q2/Q3	1.6 6.4	3 10	nC
Q <sub>gs</sub>	Gate to Source Gate Charge	Q2/Q3: V <sub>DD</sub> = -40 V,	Q1/Q4 Q2/Q3	0.8 1.6		nC
$Q_{gd}$	Gate to Drain "Miller" Charge	$I_{D} = -2.3A$	Q1/Q4 Q2/Q3	0.8 2.6		nC

# **Electrical Characteristics** $T_J = 25$ °C unless otherwise noted

Symbol	Parameter	Test Conditions	Туре	Min	Тур	Max	Units
Drain-Sou	Orain-Source Diode Characteristics						
V <sub>SD</sub>	Source to Drain Diode Forward Voltage	$V_{GS} = 0 \text{ V, } I_S = 3 \text{ A}$ (Note 2) $V_{GS} = 0 \text{ V, } I_S = -2.3 \text{ A}$ (Note 2)			0.86 -0.82	1.3 -1.3	V
t <sub>rr</sub>	Reverse Recovery Time	Q1/Q4: I <sub>F</sub> = 3 A, di/dt = 100 A/μs	Q1/Q4 Q2/Q3		32 26	52 42	ns
Q <sub>rr</sub>	Reverse Recovery Charge	Q2/Q3: I <sub>F</sub> = -2.3 A, di/dt = 100 A/μs	Q1/Q4 Q2/Q3		21 26	34 42	nC

#### Notes:

13 R<sub>0,JA</sub> is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. R<sub>0,JC</sub> is guaranteed by design while R<sub>0CA</sub> is determined by the user's board design.



a. 50 °C/W when mounted on a 1 in  $^2$ pad of 2 oz copper, the board designed Q1+Q3 or Q2+Q4.



b. 160 °C/W when mounted on a minimum pad of 2 oz copper, the board designed Q1+Q3 or Q2+Q4.

2: Pulse Test: Pulse Width < 300  $\mu$ s, Duty cycle < 2.0%.

## Typical Characteristics (N-Channel) T<sub>J</sub> = 25 °C unless otherwise noted

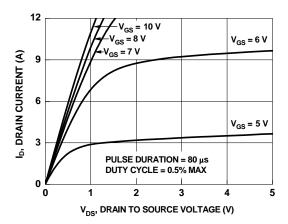


Figure 1. On Region Characteristics

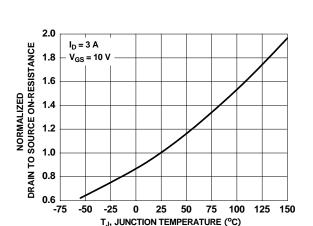


Figure 3. Normalized On Resistance vs Junction Temperature

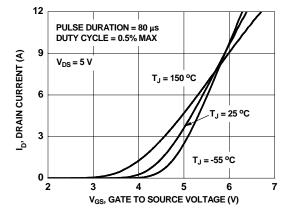


Figure 5. Transfer Characteristics

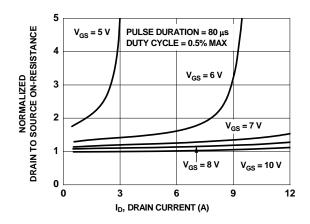


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

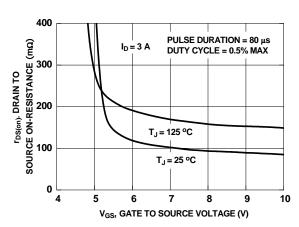


Figure 4. On-Resistance vs Gate to Source Voltage

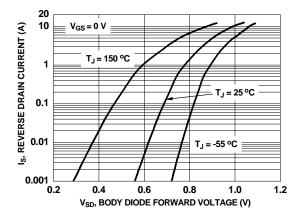


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

## Typical Characteristics (N-Channel) $T_J = 25$ °C unless otherwise noted

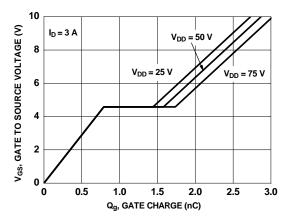


Figure 7. Gate Charge Characteristics

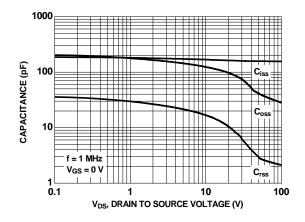


Figure 8. Capacitance vs Drain to Source Voltage

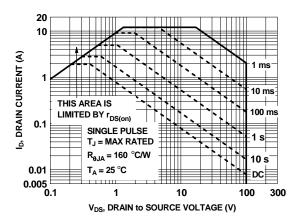
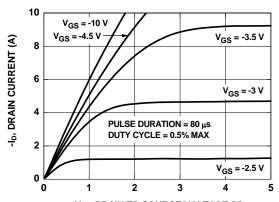


Figure 9. Forward Bias Safe Operating Area

# Typical Characteristics (P-Channel) $T_J = 25$ °C unlenss otherwise noted



-V<sub>DS</sub>, DRAIN TO SOURCE VOLTAGE (V) Figure 10. On-Region Characteristics

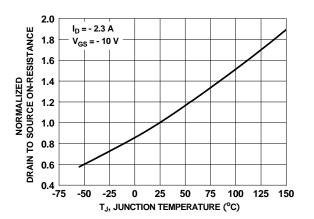


Figure 12. Normalized On-Resistance vs Junction Temperature

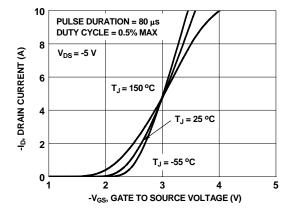


Figure 14. Transfer Characteristics

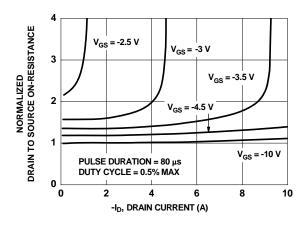


Figure 11. Normalized on-Resistance vs Drain Current and Gate Voltage

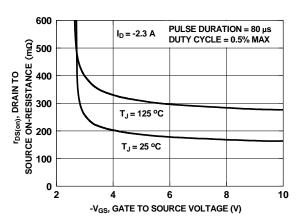


Figure 13. On-Resistance vs Gate to Source Voltage

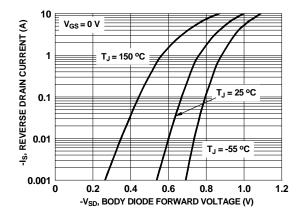


Figure 15. Source to Drain Diode Forward Voltage vs Source Current

# Typical Characteristics (P-Channel) $T_J = 25$ °C unlenss otherwise noted

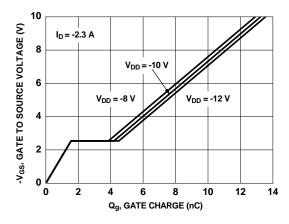


Figure 16. Gate Charge Characteristics

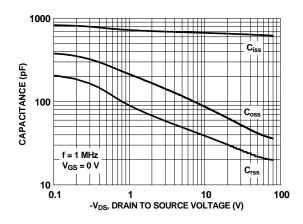


Figure 17. Capacitance vs Drain to Source Voltage

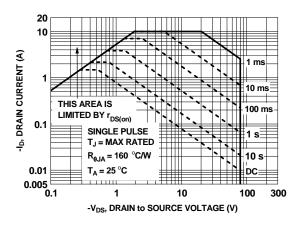


Figure 18. Forward Bias Safe Operating Area

# Typical Characteristics $T_J = 25$ °C unlenss otherwise noted

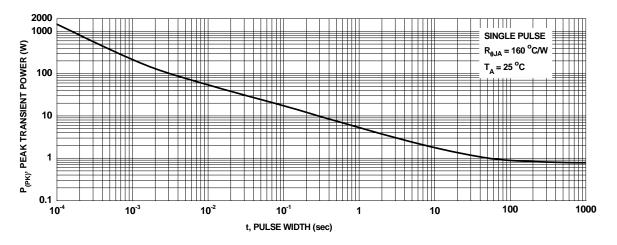


Figure 19. Single Pulse Maximum Power Dissipation

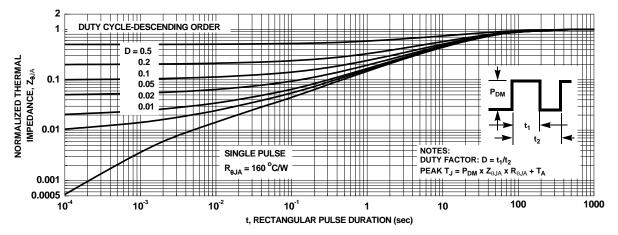
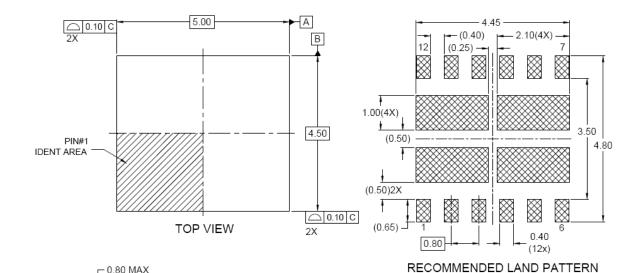
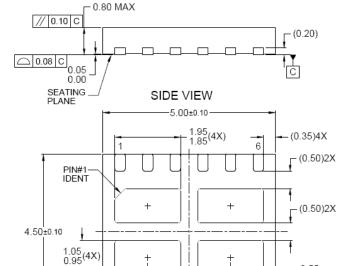


Figure 20. Junction-to-Ambient Transient Thermal Response Curve

## **Dimensional Outline and Pad Layout**





0.80

**BOTTOM VIEW** 

12

## NOTES:

- A. PACKAGE DOES NOT FULLY CONFORM TO JEDEC MO-229 REGISTRATION
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
- LAND PATTERN RECOMMENDATION IS BASED ON FSC DESIGN ONLY.
- E. DRAWING FILENAME: MKT-MLP12Erev2.

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