

#### **60V N-CHANNEL ENHANCEMENT MODE MOSFET**

## **Product Summary**

V <sub>(BR)DSS</sub>	R <sub>DS(ON)</sub> max	Package	I <sub>D max</sub> T <sub>A</sub> = +25°C	
60V	$38m\Omega$ @ $V_{GS} = 10V$	U-DFN2020-6	6.5A	
607	47mΩ @ V <sub>GS</sub> = 4.5V	Type E	5.2A	

### **Description**

This new generation MOSFET has been designed to minimize the onstate resistance (R<sub>DS(on)</sub>) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

## **Applications**

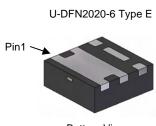
- General Purpose Interfacing Switch
- **Power Management Functions**

## **Features and Benefits**

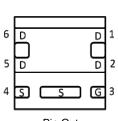
- 100% Unclamped Inductive Switch (UIS) test in production
- 0.6mm profile ideal for low profile applications
- PCB footprint of 4mm<sup>2</sup>
- Low On-Resistance
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- Qualified to AEC-Q101 Standards for High Reliability

# **Mechanical Data**

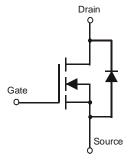
- Case: U-DFN2020-6 Type E
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish NiPdAu over Copper leadframe. Solderable per MIL-STD-202, Method 208 @4
- Weight: 0.0065 grams (approximate)







Pin Out **Bottom View** 



**Equivalent Circuit** 

### **Ordering Information** (Note 4)

Part Number	Marking	Reel size (inches)	Quantity per reel	
DMN6040SFDE-7	N8	7	3,000	
DMN6040SFDE-13	N8	13	10,000	

Notes:

- 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
- 2. See http://www.diodes.com for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + CI) and <1000ppm antimony compounds.
- 4. For packaging details, go to our website at http://www.diodes.com.

# **Marking Information**



N8 = Product Type Marking Code YM = Date Code Marking Y = Year (ex: Y = 2011)M = Month (ex: 9 = September)

Date Code Kev

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Year	201	1	2012		2013	20	14	2015		2016	2	2017
Code	Υ		Z		Α	Е	3	С		D		Е
Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
WOTILIT	Jan	Len	iviai	Αþi	iviay	Juli	Jui	Aug	Sep	OCI	NOV	Dec
Code	1	2	3	4	5	6	7	8	9	0	N	D



# **Maximum Ratings** (@ $T_A = +25$ °C, unless otherwise specified.)

Characteristic	Symbol	Value	Units		
Drain-Source Voltage	$V_{DSS}$	60	V		
Gate-Source Voltage			V <sub>GSS</sub>	±20	V
Continuous Drain Current (Note C) / 40/	Steady State	$T_A = +25^{\circ}C$ $T_A = +70^{\circ}C$	lD	5.3 4.1	А
Continuous Drain Current (Note 6) V <sub>GS</sub> = 10V	t<10s	$T_A = +25^{\circ}C$ $T_A = +70^{\circ}C$	I <sub>D</sub>	6.5 5.1	А
Pulsed Drain Current (10µs pulse, duty cycle = 1%)		I <sub>DM</sub>	30	Α	
Maximum Body Diode Continuous Current	Is	2.5	Α		
Avalanche Current (Note 7) L = 0.1mH	I <sub>AR</sub>	14.2	Α		
Avalanche Energy (Note 7) L = 0.1mH	E <sub>AR</sub>	10	mJ		

## **Thermal Characteristics**

Characteristic		Symbol	Value	Units	
Total Power Dissipation (Note 5)	$T_A = +25^{\circ}C$	П	0.66	W	
Total Power Dissipation (Note 5)	$T_A = +70$ °C	$P_{D}$	0.42	VV	
Thermal Resistance, Junction to Ambient (Note 5)	Steady state	D	189	°C/W	
Thermal Resistance, Junction to Ambient (Note 3)	t<10s	$R_{\theta JA}$	132	C/VV	
Total Power Dissipation (Note 6)	$T_A = +25$ °C	Pn	2.03	W	
Total Fower Dissipation (Note o)	$T_A = +70^{\circ}C$	FD	1.31		
Thermal Resistance, Junction to Ambient (Note 6)	Steady state	_	61		
Thermal Resistance, Junction to Ambient (Note 6)	t<10s	$R_{\theta JA}$	43	°C/W	
Thermal Resistance, Junction to Case (Note 6)	$R_{\theta JC}$	9.3			
Operating and Storage Temperature Range	_	$T_{J_{i}}T_{STG}$	-55 to +150	°C	

# Electrical Characteristics (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition	
OFF CHARACTERISTICS (Note 8)	OFF CHARACTERISTICS (Note 8)						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	60	_	_	V	$V_{GS} = 0V, I_D = 250\mu A$	
Zero Gate Voltage Drain Current	IDSS	_	_	100	nA	$V_{DS} = 60V, V_{GS} = 0V$	
Gate-Source Leakage	I <sub>GSS</sub>	_	_	±100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$	
ON CHARACTERISTICS (Note 8)							
Gate Threshold Voltage	$V_{GS(th)}$	1		3	٧	$V_{DS} = V_{GS}, I_D = 250 \mu A$	
Static Drain-Source On-Resistance	D		30	38	mΩ	$V_{GS} = 10V, I_D = 4.3A$	
Static Dialii-Source Oil-Resistance	R <sub>DS</sub> (ON)		35	47	1112.2	$V_{GS} = 4.5V, I_D = 4A$	
Forward Transfer Admittance	Y <sub>fs</sub>		4.5	_	S	$V_{DS} = 10V, I_D = 4.3A$	
Diode Forward Voltage	$V_{SD}$		0.7	1.2	V	$V_{GS} = 0V, I_{S} = 1A$	
DYNAMIC CHARACTERISTICS (Note 9)							
Input Capacitance	C <sub>iss</sub>		1287	_		V 05V V 0V	
Output Capacitance	Coss	_	57	_	pF	$V_{DS} = 25V$ , $V_{GS} = 0V$ f = 1.0MHz	
Reverse Transfer Capacitance	$C_{rss}$	_	44	_			
Gate Resistance	Rg	_	1.2	_	Ω	$V_{DS} = 0V, V_{GS} = 0V, f = 1.0MHz$	
Total Gate Charge (V <sub>GS</sub> = 10V)	$Q_g$	_	22.4	_			
Total Gate Charge (V <sub>GS</sub> = 4.5V)	$Q_g$	_	10.4	_	nC	V 20V L 42A	
Gate-Source Charge	$Q_{gs}$	_	4.9	_	nc	$V_{DS} = 30V, I_{D} = 4.3A$	
Gate-Drain Charge	$Q_{gd}$	_	3.0	_			
Turn-On Delay Time	t <sub>D(on)</sub>	_	6.6	_			
Turn-On Rise Time	t <sub>r</sub>	_	8.1	_	nS	$V_{GS} = 10V$ , $V_{DD} = 30V$ , $R_{G} = 6\Omega$ ,	
Turn-Off Delay Time	t <sub>D(off)</sub>	_	20.1	_	113	$I_D = 4.3A$	
Turn-Off Fall Time	t <sub>f</sub>	_	4.0	_			
Body Diode Reverse Recovery Time	t <sub>rr</sub>		18	_	nS	I <sub>S</sub> = 4.3A, dl/dt = 100A/μs	
Body Diode Reverse Recovery Charge	Qrr		11.9	_	nC	$I_S = 4.3A$ , $dI/dt = 100A/\mu s$	

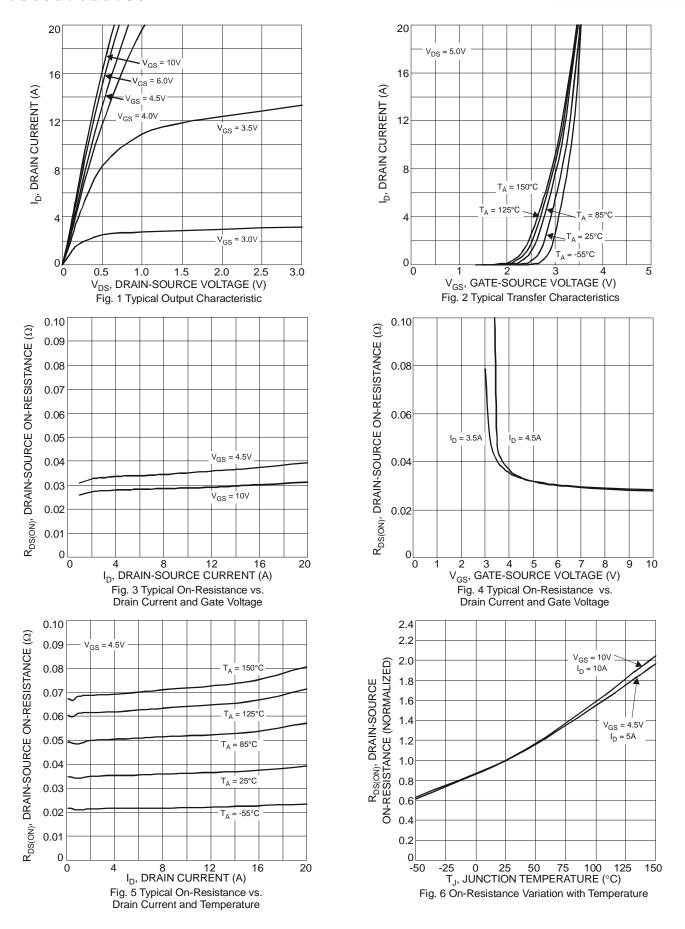
 Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate. Notes:

<sup>7.</sup>  $I_{AR}$  and  $E_{AR}$  rating are based on low frequency and duty cycles to keep  $T_J = +25^{\circ}C$ .

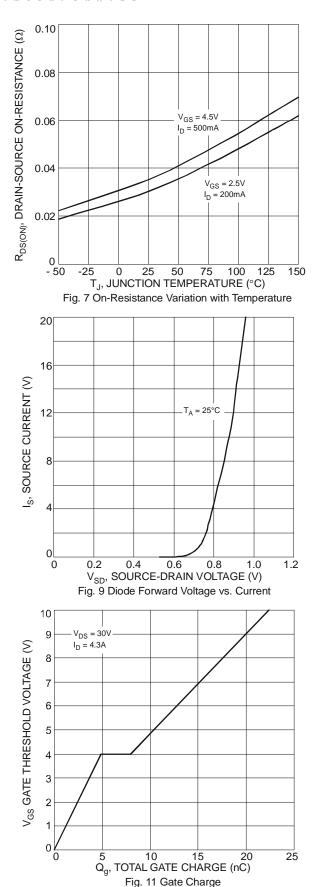
<sup>8.</sup> Short duration pulse test used to minimize self-heating effect.

<sup>9.</sup> Guaranteed by design. Not subject to product testing.









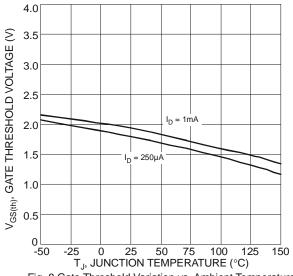
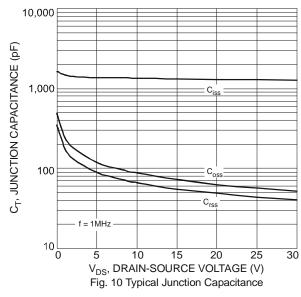
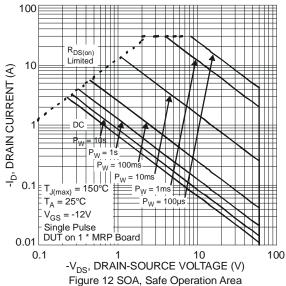
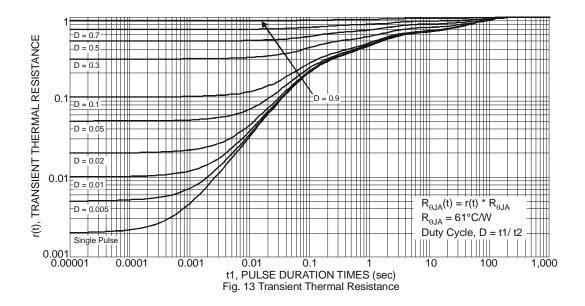


Fig. 8 Gate Threshold Variation vs. Ambient Temperature



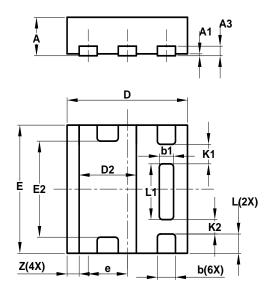






# **Package Outline Dimensions**

Please see AP02002 at http://www.diodes.com/datasheets/ap02002.pdf for latest version.

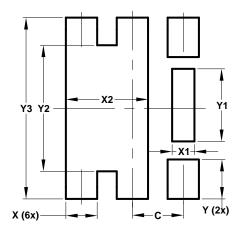


	U-DFN2020-6 Type E							
Dim	Min Max Typ							
Α	0.57	0.63	0.60					
A1	0	0.05	0.03					
A3	_	_	0.15					
b	0.25	0.35	0.30					
b1	0.185	0.285	0.235					
D	1.95	2.05	2.00					
D2	0.85	1.05	0.95					
Е	1.95	2.05	2.00					
E2	1.40	1.60	1.50					
е	_	_	0.65					
L	0.25	0.35	0.30					
L1	0.82	0.92	0.87					
K1	_	_	0.305					
K2	_	_	0.225					
Z	_	_	0.20					
All	Dimens	ions in r	nm					



### **Suggested Pad Layout**

Please see AP02001 at http://www.diodes.com/datasheets/ap02001.pdf for the latest version.



Dimensions	Value (in mm)
С	0.650
Х	0.400
X1	0.285
X2	1.050
Υ	0.500
Y1	0.920
Y2	1.600
Y3	2.300

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