

#### **General Description**

The MAX5073 is a dual-output DC-DC converter with integrated high-side n-channel power MOSFETs. Each output can be configured either as a buck converter or a boost converter. The device is capable of operating from a wide 5.5V to 23V input voltage range. Each output is programmable down to 0.8V in the buck mode and up to 28V in the boost mode with an output voltage accuracy of  $\pm 1\%$ . In the buck mode, converter 1 and converter 2 can deliver 2A and 1A, respectively. The output switching frequency of each converter can be programmed from 200kHz to 2.2MHz to avoid harmonics in a radio power supply or to reduce the size of the power supply. Each output operates 180° out-of-phase thus reducing input-capacitor ripple current, size, and cost. A SYNC input facilitates external frequency synchronization. Moreover, a CLKOUT output provides out-of-phase clock signal with respect to converter 2, allowing four-phase operation using two MAX5073 ICs in master-slave configuration.

The MAX5073 includes an internal digital soft-start that reduces inrush current, eliminates output-voltage overshoot, and ensures monotonic rise in output voltage during power-up. The device includes individual shutdown and a power-good output for each converter. Protection features include output short-circuit protection for buck mode and maximum duty-cycle limit for boost operation, as well as thermal shutdown.

The MAX5073 is available in a thermally enhanced 28pin thin QFN package that can dissipate 2.7W at +70°C ambient temperature. The device is rated for operation over the -40°C to +85°C extended, or -40°C to +125°C automotive temperature range.

## **Applications**

Automotive Radio Power Supply Point-of-Load DC-DC Converters Telecom Line Card Networking Line Card

Power-Over-Ethernet Postregulation for PDs

## **Ordering Information**

| PART        | PART TEMP RANGE |                                | PKG<br>CODE |
|-------------|-----------------|--------------------------------|-------------|
| MAX5073ETI  | -40°C to +85°C  | 28 Thin QFN-EP*<br>(5mm x 5mm) | T2855-6     |
| MAX5073ETI+ | -40°C to +85°C  | 28 Thin QFN-EP*<br>(5mm x 5mm) | T2855-6     |

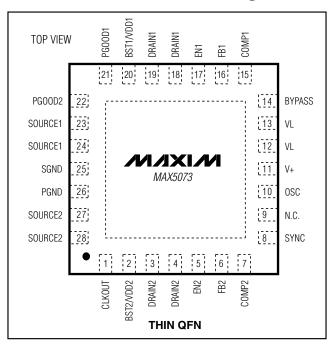
<sup>\*</sup>EP = Exposed pad.

Ordering Information continued at end of data sheet.

## **Features**

- ♦ 4.5V to 5.5V or 5.5V to 23V Input Supply **Voltage Range**
- ♦ 0.8V (Buck) to 28V (Boost) Output Voltage
- **♦ Two Independent Output DC-DC Converters** with Internal Power MOSFETs
- ♦ Each Output can be Configured in Buck or Boost Mode
- ♦ IOUT1 and IOUT2 of 2A and 1A (Respectively) in **Buck Mode**
- **♦ 180° Out-of-Phase Operation**
- **♦ Clock Output for Four Phase Operation**
- ♦ Switching Frequency Programmable from 200kHz to 2.2MHz
- ♦ Digital Soft-Start and Sync Input
- ♦ Individual Converter Shutdown and Power-Good Output
- ♦ Short-Circuit Protection (Buck)/Maximum Duty-Cycle Limit (Boost)
- **♦ Thermal Shutdown**
- ♦ Thermally Enhanced 28-Pin Thin QFN Package Dissipates up to 2.7W at +70°C

#### Pin Configuration



Maxim Integrated Products 1

<sup>+</sup>Denotes lead-free package.

#### **ABSOLUTE MAXIMUM RATINGS**

| V+ to PGND0.3V to +25V SGND to PGND0.3V to +0.3V  |
|---|
| VL to SGND0.3V to the lower of +6V or (V+ + 0.3V) |
| BST1/VDD1, BST2/VDD2, DRAIN, PGOOD2, PGOOD1 to    |
| SGND0.3V to +30V                                  |
| BST1/VDD1 to SOURCE1,                             |
| BST2/VDD2 to SOURCE20.3V to +6V                   |
| SOURCE_ to SGND0.6V to +25V                       |
| EN_ to SGND0.3V to (VL to +0.3V)                  |
| CLKOUT, BYPASS, OSC, COMP1,                       |
| COMP2, SYNC, FB_ to SGND0.3V to (VL + 0.3V)       |
| SOURCE1, DRAIN1 Peak Current5A for 1ms            |

| SOURCE2, DRAIN2 Peak Current                                | 3A for 1ms   |
|---|--------------|
| VL, BYPASS to SGND Short Circuit                            | Continuous   |
| Continuous Power Dissipation ( $T_A = +70$ °C)              |              |
| 28-Pin Thin QFN (derate 21.3mW/°C above +70°C               | )2758mW*     |
| Package Junction-to-Case Thermal Resistance (θ <sub>J</sub> | c)2°C/W      |
| Operating Temperature Ranges:                               |              |
| MAX5073ETI (TMIN to TMAX)40                                 | J°C to +85°C |
| MAX5073ATI (T <sub>MIN</sub> to T <sub>MAX</sub> )40°       | °C to +125°C |
| Junction Temperature  |              |
| Storage Temperature Range65°                                |              |
| Lead Temperature (soldering, 10s)                           | +300°C       |
| *As per JEDEC51 standard.                                   |              |

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

#### **ELECTRICAL CHARACTERISTICS**

(V+ = VL = 5.2V or V+ = 5.5V to 23V, EN\_ = VL, SYNC = GND, I<sub>VL</sub> = 0mA, PGND = SGND, C<sub>BYPASS</sub> = 0.22μF, C<sub>VL</sub> = 4.7μF (ceramic),  $R_{OSC} = 10k\Omega$  (circuit of Figure 1),  $T_A = T_J = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted.) (Note 1)

| PARAMETER                             | SYMBOL              | CONDITIO  | MIN                            | TYP   | MAX  | UNITS |                         |  |
|---------------------------------------|---------------------|---|--------------------------------|-------|------|-------|-------------------------|--|
| SYSTEM SPECIFICATIONS                 |                     |   |                                |       |      |       |                         |  |
| Inner Valtage Dance                   | V+                  | (Note 2)  | 5.5                            |       | 23.0 | V     |                         |  |
| Input Voltage Range                   | V+                  | VL = V+   |                                | 4.5   |      | 5.5   | ]                       |  |
| Operating Supply Current              | IQ                  | VL unloaded, no switching 12V, $R_{OSC} = 60k\Omega$              | , V <sub>FB</sub> _ = 1V, V+ = |       | 2.2  | 4     | mA                      |  |
| V+ Standby Supply Current             | I <sub>STBY</sub>   | EN_ = 0, PGOOD_ floating<br>ROSC = $60k\Omega$ (MAX5073E          |                                |       | 0.6  | 1.2   | mA                      |  |
| v+ Standby Supply Guitent             | 12181               | $EN_{-}$ = 0, PGOOD_ floating $R_{OSC}$ = 60k $\Omega$ (MAX5073A) |                                | 0.6   | 1.4  | IIIA  |                         |  |
|                                       |                     | $V_{OUT1} = 3.3V \text{ at } 1.5A,$                               | V+ = VL = 5V                   |       | 82   |       |                         |  |
| Efficiency                            | η                   | $V_{OUT2} = 2.5V \text{ at } 0.75A$                               | V+ = 12V                       |       | 80   |       | %                       |  |
|                                       |                     | $(f_{SW} = 1.25MHz)$  | V+ = 16V                       |       | 78   |       |                         |  |
| STARTUP/VL REGULATOR                  |                     |   |                                |       |      |       |                         |  |
| VL Undervoltage Lockout Trip<br>Level | UVLO                | VL falling  |                                | 3.95  | 4.1  | 4.25  | V                       |  |
| VL Undervoltage Lockout<br>Hysteresis |                     |   |                                |       | 175  |       | mV                      |  |
| VL Output Voltage                     | VL                  | V+ = 5.5V to 23V, ISOURCE   | = 0 to 40mA                    | 4.9   | 5.2  | 5.5   | V                       |  |
| BYPASS OUTPUT                         |                     |   |                                |       |      |       |                         |  |
| DVDASS Voltage                        | \/p\/p\@\@@         | $IBYPASS = 0$ , $ROSC = 60k\Omega$                                | 2 (MAX5073ETI)                 | 1.98  | 2.00 | 2.02  | V                       |  |
| BYPASS Voltage                        | V <sub>BYPASS</sub> | $I_{BYPASS} = 0$ , $R_{OSC} = 60$ kΩ                              | 2 (MAX5073ATI)                 | 1.975 | 2.00 | 2.025 | ] v                     |  |
| BYPASS Load Regulation                | ΔVBYPASS            | 0 ≤ IBYPASS ≤ 50µA, ROSC  | = 60kΩ                         | 0     | 2    | 10    | mV                      |  |
| SOFT-START                            |                     |   |                                |       |      |       |                         |  |
| Digital Ramp Period                   |                     | Internal 6-bit DAC  |                                |       | 2048 |       | fosc<br>clock<br>cycles |  |
| Soft-Start Steps                      |                     |   |                                |       | 64   |       | steps                   |  |

#### **ELECTRICAL CHARACTERISTICS (continued)**

 $(V+ = VL = 5.2V \text{ or } V+ = 5.5V \text{ to } 23V, \text{EN}\_ = VL, \text{SYNC} = \text{GND}, \text{I}_{VL} = 0\text{mA}, \text{PGND} = \text{SGND}, \text{C}_{BYPASS} = 0.22\mu\text{F}, \text{C}_{VL} = 4.7\mu\text{F} \text{ (ceramic)}, \text{R}_{OSC} = 10\text{k}\Omega \text{ (circuit of Figure 1)}, \text{T}_{A} = \text{T}_{J} = \text{T}_{MIN} \text{ to T}_{MAX}, \text{unless otherwise noted.)} \text{ (Note 1)}$ 

| PARAMETER                             | SYMBOL             | CONDITIONS  | MIN      | TYP | MAX   | UNITS |  |
|---------------------------------------|--------------------|---|----------|-----|-------|-------|--|
| VOLTAGE-ERROR AMPLIFIER               |                    |   | <b>,</b> |     |       | I.    |  |
| FB_ Input Bias Current                | I <sub>B(EA)</sub> |   |          |     | 250   | nA    |  |
|                                       |                    | 0°C ≤ T <sub>A</sub> ≤ +70°C                                      | 0.792    | 0.8 | 0.808 |       |  |
| FB_ Input Voltage Set Point           |                    | -40°C ≤ T <sub>A</sub> ≤ +85°C                                    | 0.788    | 0.8 | 0.812 | V     |  |
|                                       |                    | -40°C ≤ T <sub>J</sub> ≤ +125°C (MAX5073ATI only)                 | 0.788    | 0.8 | 0.812 |       |  |
|                                       |                    | 0°C to +85°C  | 1.25     | 2   | 2.70  |       |  |
| FB_ to COMP_<br>Transconductance      | дм                 | -40°C to +85°C  | 1.2      | 2   | 2.9   | mS    |  |
| Transconductance                      |                    | -40°C to +125°C (MAX5073ATI only)                                 | 1.2      | 2   | 2.9   |       |  |
| INTERNAL PMOSFETS                     |                    | ·   | •        |     |       | •     |  |
|                                       |                    | ISWITCH = 100mA,<br>VBST1/VDD1 to VSOURCE1 = 5.2V<br>(MAX5073ETI) |          | 195 | 290   |       |  |
| On Decistores Converter 1             | D                  | Iswitch = 100mA,<br>VBST1/VDD1 to VSOURCE1 = 5.2V<br>(MAX5073ATI) |          | 195 | 330   |       |  |
| On-Resistance Converter 1             | Ron1               | ISWITCH = 100mA,<br>VBST1/VDD1 to VSOURCE1 = 4.5V<br>(MAX5073ETI) |          | 200 | 315   | mΩ    |  |
|                                       |                    | ISWITCH = 100mA,<br>VBST1/VDD1 to VSOURCE1 = 4.5V<br>(MAX5073ATI) |          | 200 | 350   |       |  |
| On-Resistance Converter 2             | R <sub>ON2</sub>   | ISWITCH = 100mA,<br>VBST2/VDD2 to VSOURCE2 = 5.2V                 |          | 330 | 630   | mΩ    |  |
| On-nesistance Conventer 2             | nON2               | ISWITCH = 100mA,<br>VBST2/VDD2 to VSOURCE2 = 4.5V                 |          | 350 | 690   | 11122 |  |
| Minimum Converter 1 Output Current    | I <sub>OUT1</sub>  | V <sub>OUT1</sub> = 3.3V, V+ = 12V (Note 3)                       |          | 2   |       | А     |  |
| Minimum Converter 2 Output Current    | I <sub>OUT2</sub>  | V <sub>OUT2</sub> = 2.5V, V+ = 12V (Note 3)                       |          | 1   |       | А     |  |
| Converter 1 MOSFET Leakage<br>Current | I <sub>LK1</sub>   | EN1 = 0V, V <sub>DS</sub> = 23V                                   |          |     | 10    | μΑ    |  |
| Converter 2 MOSFET Leakage<br>Current | I <sub>LK2</sub>   | EN2 = 0V, V <sub>DS</sub> = 23V                                   |          |     | 10    | μA    |  |
| INTERNAL SWITCH CURRENT LI            | MIT                |   |          |     |       |       |  |
| Command Limit Command 1               | L                  | V+ = 12V (MAX5073ETI)   | 2.3      | 3   | 4.3   | ^     |  |
| Current-Limit Converter 1             | ICL1               | V+ = 12V (MAX5073ATI)   | 2.3      | 3   | 4.6   | А     |  |
| Command Limit Command of              | L                  | MAX5073ETI  | 1.38     | 1.8 | 2.10  | Δ     |  |
| Current-Limit Converter 2             | I <sub>CL2</sub>   | MAX5073ATI  | 1.38     | 1.8 | 2.20  | A     |  |

#### **ELECTRICAL CHARACTERISTICS (continued)**

 $(V+ = VL = 5.2V \text{ or } V+ = 5.5V \text{ to } 23V, \text{ EN}\_ = VL, \text{ SYNC} = \text{GND}, \text{ } \text{I}_{VL} = \text{0mA}, \text{ PGND} = \text{SGND}, \text{ } \text{C}_{BYPASS} = 0.22\mu\text{F}, \text{ } \text{C}_{VL} = 4.7\mu\text{F} \text{ (ceramic)}, \text{ } \text{R}_{OSC} = 10\text{k}\Omega \text{ (circuit of Figure 1)}, \text{ } \text{T}_{A} = \text{T}_{J} = \text{T}_{MIN} \text{ to } \text{T}_{MAX}, \text{ unless otherwise noted.)} \text{ (Note 1)}$ 

| PARAMETER                     | SYMBOL             | CONDITIONS   | MIN  | TYP  | MAX  | UNITS   |
|-------------------------------|--------------------|--|------|------|------|---------|
| INTERNAL OSCILLATOR/SYNC      |                    |  |      |      |      |         |
| Mariana Distriction           |                    | SYNC = SGND, f <sub>SW</sub> = 1.25MHz                                     | 84   | 86   | 95   | 0/      |
| Maximum Duty Cycle            | DMAX               | SYNC = SGND, f <sub>SW</sub> = 2.2MHz                                      | 84   | 86   | 95   | %       |
| Switching Frequency Range     | fsw                | Each converter   | 200  |      | 2200 | kHz     |
| Switching Frequency           | fSET               | $R_{OSC} = 10k\Omega$ , each converter                                     | 1125 | 1250 | 1375 | kHz     |
| Switching Frequency Accuracy  |                    | $5.6k\Omega \le R_{OSC} \le 56k\Omega$ , 1% each converter                 | -15  |      | +15  | %       |
| SYNC Frequency Range          | fsync              | SYNC input frequency is twice the individual converter frequency           | 400  |      | 4400 | kHz     |
| SYNC High Threshold           | Vsynch             |  | 2.4  |      |      | V       |
| SYNC Low Threshold            | VSYNCL             |  |      |      | 0.8  | V       |
| SYNC Input Min Pulse Width    | tsyncin            |  |      | 100  |      | ns      |
| Clock Output Phase Delay      | CLKOUT<br>PHASE    | $R_{OSC} = 60k\Omega$ , 1%, with respect to converter 2 / SOURCE2 waveform |      | 45   |      | degrees |
| SYNC to SOURCE1 Phase Delay   | SYNCPHASE          | $R_{OSC} = 60k\Omega$ , 1%   |      | 45   |      | degrees |
| Clock Output High Level       | VCLKOUTH           | VL = 5.2V, sourcing 5mA  | 4    |      |      | V       |
| Clock Output Low Level        | VCLKOUTL           | VL = 5.2V, sinking 5mA   |      |      | 0.4  | V       |
| EN_ INPUTS                    |                    |  |      |      |      |         |
| EN_ Input High Threshold      | VIH                | V + = VL = 5.2V  | 2.4  | 1.8  |      | V       |
| EN_ Input Low Threshold       | V <sub>IL</sub>    | V + = VL = 5.2V  |      | 1.2  | 0.8  | V       |
| EN_ Bias Current              | I <sub>B(EN)</sub> |  |      |      | 250  | nA      |
| POWER-GOOD OUTPUT (PGOOI      | <b>O_</b> )        |  |      |      |      |         |
| PGOOD_ Threshold              | PGOODVTH_          | PGOOD goes high after V <sub>OUT</sub> crosses PGOOD_threshold             | 90   | 92.5 | 95   | % Vout  |
| DOOOD Outsid Vallage          | M                  | I <sub>SINK</sub> = 3mA (MAX5073ETI)                                       |      |      | 0.4  | V       |
| PGOOD_ Output Voltage         | Vpgood_            | I <sub>SINK</sub> = 3mA (MAX5073ATI)                                       |      |      | 0.52 | \ \ \   |
| PGOOD_ Output Leakage Current | ILKPGOOD_          | V+ = VL = 5.2V, V <sub>PGOOD</sub> _ = 23V, V <sub>FB</sub> _ = 1V         |      |      | 1    | μΑ      |
| THERMAL MANAGEMENT            |                    |  |      |      |      |         |
| Thermal Shutdown              | TSHDN              | Junction temperature   |      | +150 |      | °C      |
| Thermal Hysteresis            | T <sub>HYST</sub>  | Junction temperature   |      | 30   |      | °C      |

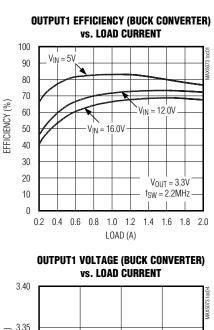
Note 1: Specifications at -40°C are guaranteed by design and not production tested.

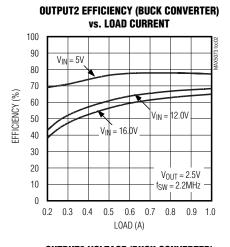
Note 2: Operating supply range (V+) is guaranteed by VL line regulation test. Connect V+ to VL for 5V operation.

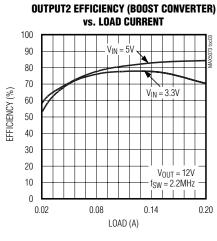
**Note 3:** Output current may be limited by the power dissipation of the package, refer to the *Power Dissipation* section in the *Applications Information*.

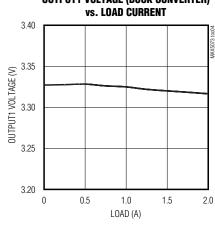
#### **Typical Operating Characteristics**

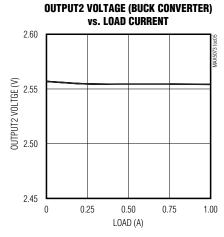
 $(V + = VL = 5.2V, T_A = +25^{\circ}C, unless otherwise noted.)$ 

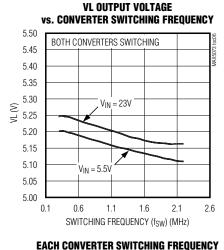


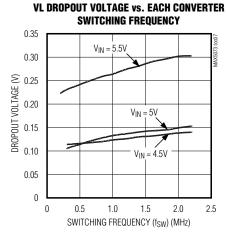


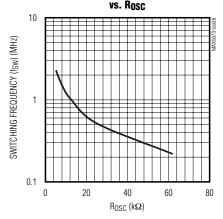




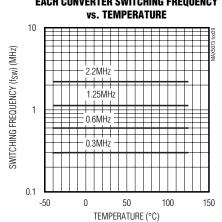






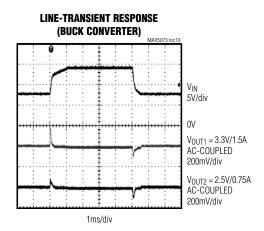


**EACH CONVERTER SWITCHING FREQUENCY** 

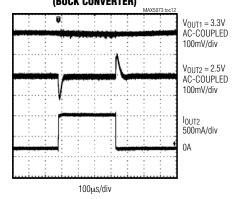


Typical Operating Characteristics (continued)

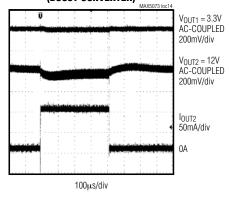
 $(V + = VL = 5.2V, T_A = +25^{\circ}C, unless otherwise noted.)$ 



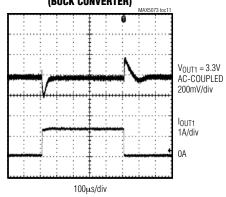
## CONVERTER 2 LOAD-TRANSIENT RESPONSE (BUCK CONVERTER)



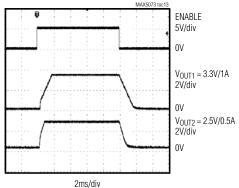
#### LOAD-TRANSIENT RESPONSE (BOOST CONVERTER)



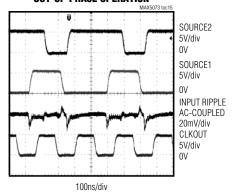
## CONVERTER 1 LOAD-TRANSIENT RESPONSE (BUCK CONVERTER)



#### SOFT-START/SOFT-STOP



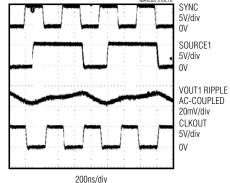
#### **OUT-OF-PHASE OPERATION**

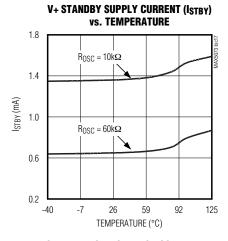


### Typical Operating Characteristics (continued)

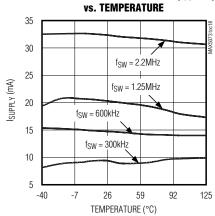
 $(V + = VL = 5.2V, T_A = +25^{\circ}C, unless otherwise noted.)$ 

## EXTERNAL SYNCHRONIZATION MAXSO

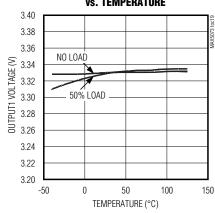




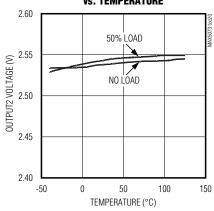
## V+ SWITCHING SUPPLY CURRENT (ISUPPLY)



## OUTPUT1 VOLTAGE (BUCK CONVERTER) vs. TEMPERATURE

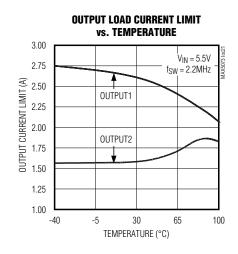


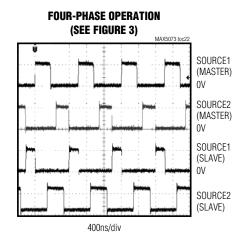
## OUTPUT2 VOLTAGE (BUCK CONVERTER) vs. TEMPERATURE



#### Typical Operating Characteristics (continued)

(V+ = VL = 5.2V,  $T_A = +25$ °C, unless otherwise noted.)





#### **Pin Description**

| PIN  | NAME      | FUNCTION  |
|------|-----------|---|
| 1    | CLKOUT    | Clock Output. CLKOUT is 45° phase-shifted with respect to converter 2 (SOURCE2, Figure 3). Connect CLKOUT (master) to the SYNC of a second MAX5073 (slave) for a four-phase converter.  |
| 2    | BST2/VDD2 | Buck Converter Operation—Bootstrap Flying-Capacitor Connection for Converter 2. Connect BST2/VDD2 to an external ceramic capacitor and diode according to the standard application circuit (Figure 1). Boost Converter Operation—Driver Bypass Capacitor Connection. Connect a low-ESR 0.1µF ceramic capacitor from BST2/VDD2 to PGND (Figure 8). |
| 3, 4 | DRAIN2    | Connection to Converter 2 Internal MOSFET Drain. Buck converter operation—use the MOSFET as a high-side switch and connect DRAIN2 to the input supply. Boost converter operation—use the MOSFET as a low-side switch and connect DRAIN2 to the inductor and diode junction (Figure 8).  |
| 5    | EN2       | Active-High Enable Input for Converter 2. Drive EN2 low to shut down converter 2, drive EN2 high for normal operation. Use EN2 in conjunction with EN1 for supply sequencing. Connect to VL for always-on operation.  |
| 6    | FB2       | Feedback Input for Converter 2. Connect FB2 to a resistive divider between converter 2's output and SGND to adjust the output voltage. To set the output voltage below 0.8V, connect FB2 to a resistive voltage-divider from BYPASS to regulator 2's output (Figure 5). See the Setting the Output Voltage section.                               |
| 7    | COMP2     | Compensation Connection for Converter 2. See the <i>Compensation</i> section to compensate converter 2's control loop.  |
| 8    | SYNC      | External Clock Synchronization Input. Connect SYNC to a 400kHz to 4400kHz clock to synchronize the switching frequency with the system clock. Each converter frequency is one half the frequency applied to SYNC. Connect SYNC to SGND when not used.   |
| 9    | N.C.      | No Connection. Not internally connected.  |

## Pin Description (continued)

| OSC Illator Frequency Set Input. Connect a resistor from OSC to SGND (R <sub>OSC</sub> ) to set the switching frequency (see the <i>Oscillator</i> section). Set R <sub>OSC</sub> for equal to or lower oscillator frequency than the SYNC input frequency when using external synchronization (0.2fsync, or 5 <sub>0</sub> SC < 1.2fsyn <sub>C</sub> ). R <sub>OSC</sub> is still required when an external clock is connected to the SYNC input.  11 V+ Input Supply Voltage, V+ voltage range from 5.5V to 23V. Connect the V+ and VL together for 4.5V to 5.5V input operation. Bypass with a minimum 0.1µF ceramic capacitor to SGND.  12. 13 VL Internal 5.2V Linear Regulator Output. Use VL to drive the high-side switch at BST1/VDD1 and BST2/VDD2. Bypass VL with a 0.1µF capacitor to PGND and a 4.7µF ceramic capacitor to SGND.  14 BYPASS 2.0V Output. Bypass to SGND with a 0.22µF or greater ceramic capacitor.  15 COMP1 Compensation Connection for Converter 1 (See the <i>Compensation</i> Section)  Feedback Input for Converter 1. Connect FB1 to a resistive divider between converter 1's output and SGND to program the output voltage. To set the output voltage below 0.8V, connect FB1 to a resistive divider from BYRASS to regulator 1's autput (Figure 5). See the <i>Setting the Output Voltage</i> section.  17 EN1 Active-High Enable Input for Converter 1. Drive EN1 low to shut down converter 1, drive EN1 high for normal operation. Use EN1 in conjunction with EN2 for supply sequencing. Connect to VL for always-on operation.  28 BST1/VDD1 Boost converter operation—use the MCSFET as a high-side switch and connect DRAIN1 to the input supply. Boost converter operation—use the MCSFET as a low-side switch and connect DRAIN1 to the inductor and diode junction of portion and diode junction voltage.  29 PGOOD2 Converter 1 Power-Good Output. Open-drain output goes low when converter 1's output falls below 92.5% of its set regulation voltage. Use PGOOD1, PGOOD2, EN1, and EN2 to sequence the converters.  29 PGOD2 Connection to the Converter 1 Internal MOSFET Source.  Buck converter operation—connect SOURCE to the switched s | PIN    | NAME      | FUNCTION   |  |  |  |  |  |  |
|--|--------|-----------|--|--|--|--|--|--|--|
| 12, 13  VL Internal 5.2V Linear Regulator Output. Use VL to drive the high-side switch at BST1/VDD1 and BST2/VDD2. Bypass VL with a 0.1µF capacitor to PGND and a 4.7µF ceramic capacitor to SGND.  14 BYPASS 2.0V Output. Bypass to SGND with a 0.2µF or greater ceramic capacitor.  15 COMP1 Compensation Connection for Converter 1 (See the Compensation Section)  16 FB1 Feedback Input for Converter 1. Connect FB1 to a resistive divider between converter 1's output and SGND to program the output voltage. To set the output voltage below 0.8V, connect FB1 to a resistive voltage-divider from BYPASS to regulator 1's output (Figure 5). See the Setting the Output Voltage-section.  17 EN1 Active-High Enable Input for Converter 1. Drive EN1 low to shut down converter 1, drive EN1 high for normal operation. Use EN1 in conjunction with EN2 for supply sequencing. Connect to VL for always-on operation.  18 19 DRAIN1  BAIN1 DRAIN1  BEST1/VDD1  Connection to the Converter 1 Internal MOSFET Drain.  Buck Converter operation—use the MOSFET as a high-side switch and connect DRAIN1 to the inductor and diode junction.  BEST1/VDD1  BEST1/VDD1  BUCK Converter Operation—Bootstrap Flying-Capacitor Connection for Converter 1. Connect BST1/VDD1 to an external ceramic capacitor and diode according to the Standard Application Circuit (Figure 1). Boost Converter 1 Power-Good Output. Open-drain output goes low when converter 1's output falls below 92.5% of its set regulation voltage. Use PGOOD1, PGOOD2, EN1, and EN2 to sequence the converters.  22 PGOOD2  Converter 2 Power-Good Output. Open-drain output goes low when converter 1's output falls below 92.5% of its set regulation voltage. Use PGOOD1, PGOOD2, EN1, and EN2 to sequence the converters. Boost converter operation—connect SOURCE1 to PGND.  Connection to the Converter 1 Internal MOSFET Source. Buck converter operation—connect SOURCE1 to the switched side of the inductor as shown in Figure 1. Boost converter operation—connect SOURCE2 to the switched side of the inductor as shown in Figure 1. B   | 10     | OSC       | frequency (see the $Oscillator$ section). Set $R_{OSC}$ for equal to or lower oscillator frequency than the Sinput frequency when using external synchronization (0.2fSYNC < fOSC < 1.2fSYNC). Rosc is still reduced by the contraction of the still reduced by the |  |  |  |  |  |  |
| 12, 13  VL BST2/VDD2. Bypass VL with a 0.1 µF capacitor to PGND and a 4.7 µF ceramic capacitor to SGND.  15 COMP1 Compensation Connection for Converter 1 (See the Compensation Section)  Feedback Input for Converter 1. Connect FB1 to a resistive divider between converter 1's output and SGND to program the output voltage. To set the output voltage below 0.8 %, connect FB1 to a resistive voltage-divider from BYPASS to regulator 1's output (Figure 5). See the Setting the Output Voltage section.  EN1  Active-High Enable Input for Converter 1. Drive EN1 low to shut down converter 1, drive EN1 high for normal operation. Use EN1 in conjunction with EN2 for supply sequencing. Connect to VL for always-on operation.  Connection to the Converter 1 Internal MOSFET Drain.  Buck converter operation—use the MOSFET as a high-side switch and connect DRAIN1 to the input supply. Boost converter operation—use the MOSFET as a high-side switch and connect DRAIN1 to the inductor and diode junction.  Buck Converter Operation—Bootstrap Flying-Capacitor Connection for Converter 1. Connect BST1/VDD1 to an external ceramic capacitor and diode according to the Standard Application Circuit (Figure 1). Boost Converter Operation—Driver Bypass Capacitor Connection. Connect a low-ESR 0.1 µF ceramic capacitor from BST1/VDD1 to PGND.  Converter 1 Power-Good Output. Open-drain output goes low when converter 1's output falls below 92.5% of its set regulation voltage. Use PGOOD1, PGOOD2, EN1, and EN2 to sequence the converters.  Connection to the Converter 1 Internal MOSFET Source.  Buck converter operation—connect SOURCE1 to the switched side of the inductor as shown in Figure 1. Boost converter operation—connect SOURCE1 to the switched side of the inductor as shown in Figure 1. Power Ground. Connect extiller diode anode, input capacitor negative, output capacitor negative, and VL bypass capacitor returns to PGND.  Power Ground. Connect rectifier diode anode, input capacitor negative, output capacitor negative, and VL bypass capacitor returns to PGN   | 11     | V+        |  |  |  |  |  |  |  |
| 15 COMP1 Compensation Connection for Converter 1 (See the Compensation Section)  16 FB1 Fedback Input for Converter 1. Connect FB1 to a resistive divider between converter 1's output and SGND to program the output voltage. To set the output voltage below 0.8V, connect FB1 to a resistive voltage-divider from BYPASS to regulator 1's output (Figure 5). See the Setting the Output Voltage section.  17 EN1 Active-High Enable Input for Converter 1. Drive EN1 low to shut down converter 1, drive EN1 high for normal operation. Use EN1 in conjunction with EN2 for supply sequencing. Connect to VL for always-on operation.  18, 19 DRAIN1 Connection to the Converter 1 Internal MOSFET Drain.  18, 19 BURK converter operation—use the MOSFET as a high-side switch and connect DRAIN1 to the input supply. Boost converter operation—use the MOSFET as a low-side switch and connect DRAIN1 to the inductor and diode junction.  19 BST1/VDD1 BURK Converter Operation—Bootstrap Flying-Capacitor Connection for Converter 1. Connect BST1/VDD1 to an external ceramic capacitor and diode according to the Standard Application Circuit (Figure 1). Boost Converter Operation—Driver Bypass Capacitor Connection. Connect a low-ESR 0.1µF ceramic capacitor from BST1/VDD1 to PGND.  20 PGOOD1 Converter 1 Power-Good Output. Open-drain output goes low when converter 1's output falls below 92.5% of its set regulation voltage. Use PGOOD1, PGOOD2, EN1, and EN2 to sequence the converters.  21 PGOOD2 Converter 2 Power-Good Output. Open-drain output goes low when converter 2's output falls below 92.5% of its set regulation voltage.  22 PGOOD3 Signal Ground. Connect SGND to the exposed pad. Connect SGND and PGND together at a single point. Boost converter operation—connect SOURCE1 to PGND.  23 PGND Signal Ground. Connect FGND to the exposed pad. Connect SGND and PGND together at a single point. Power Ground. Connect rectifier diode anode, input capacitor negative, output capacitor negative, and VL bypass capacitor returns to PGND.  24 SOURCE2 SOURCE2 SOURCE2 SOURCE2 to   | 12, 13 | VL        |  |  |  |  |  |  |  |
| Feedback Input for Converter 1. Connect FB1 to a resistive divider between converter 1's output and SGND to program the output voltage. To set the output voltage below 0.8V, connect FB1 to a resistive voltage-divider from BYPASS to regulator 1's output (Figure 5). See the Setting the Output Voltage section.  EN1  EN1  Active-High Enable Input for Converter 1. Drive EN1 low to shut down converter 1, drive EN1 high for normal operation. Use EN1 in conjunction with EN2 for supply sequencing. Connect to VL for always-on operation.  Connection to the Converter 1 Internal MOSFET Drain.  Buck converter operation—use the MOSFET as a high-side switch and connect DRAIN1 to the input supply. Boost converter operation—use the MOSFET as a low-side switch and connect DRAIN1 to the inductor and diode junction.  Buck Converter Operation—Bootstrap Flying-Capacitor Connection for Converter 1. Connect BST1/VDD1 to an external ceramic capacitor and diode according to the Standard Application Circuit (Figure 1). Boost Converter 1 Power-Good Output. Open-drain output goes low when converter 1's output falls below 92.5% of its set regulation voltage. Use PGOOD1, PGOOD2, EN1, and EN2 to sequence the converters.  Converter 2 Power-Good Output. Open-drain output goes low when converter 2's output falls below 92.5% of its set regulation voltage.  Connection to the Converter 1 Internal MOSFET Source.  Buck converter operation—connect SOURCE1 to the switched side of the inductor as shown in Figure 1. Boost converter operation—connect SOURCE1 to PGND.  Connection to the Converter 2 GND to the exposed pad. Connect SGND and PGND together at a single point.  Power Ground. Connect SGND to the exposed pad. Connect SGND and PGND together at a single point.  Power Ground. Connect rectifier diode anode, input capacitor negative, output capacitor negative, and VL bypass capacitor returns to PGND.  Connection to the Converter 2 Internal MOSFET Source.  Buck converter operation—connect SOURCE2 to the switched side of the inductor as shown in Figure 1.   | 14     | BYPASS    | 2.0V Output. Bypass to SGND with a 0.22µF or greater ceramic capacitor.  |  |  |  |  |  |  |
| to program the output voltage. To set the output voltage below 0.8V, connect FB1 to a resistive voltage-divider from BYPASS to regulator 1's output (Figure 5). See the Setting the Output Voltage section.  RN1  Active-High Enable Input for Converter 1. Drive EN1 low to shut down converter 1, drive EN1 high for normal operation. Use EN1 in conjunction with EN2 for supply sequencing. Connect to VL for always-on operation.  Connection to the Converter 1 Internal MOSFET Drain.  Buck converter operation—use the MOSFET as a high-side switch and connect DRAIN1 to the input supply. Boost converter operation—use the MOSFET as a low-side switch and connect DRAIN1 to the inductor and diode junction.  Buck Converter Operation—Bootstrap Flying-Capacitor Connection for Converter 1. Connect BST1/VDD1 to an external ceramic capacitor and diode according to the Standard Application Circuit (Figure 1). Boost Converter Operation—Driver Bypass Capacitor Connection. Connect a low-ESR 0.1µF ceramic capacitor from BST1/VDD1 to PGND.  PGOOD1  Converter 1 Power-Good Output. Open-drain output goes low when converter 1's output falls below 92.5% of its set regulation voltage. Use PGOOD1, PGOOD2, EN1, and EN2 to sequence the converters.  Converter 2 Power-Good Output. Open-drain output goes low when converter 2's output falls below 92.5% of its set regulation voltage.  Connection to the Converter 1 Internal MOSFET Source.  Buck converter operation—connect SOURCE1 to PGND.  Signal Ground. Connect SGND to the exposed pad. Connect SGND and PGND together at a single point.  Power Ground. Connect rectifier diode anode, input capacitor negative, output capacitor negative, and VL bypass capacitor returns to PGND.  Connection to the Converter 2 Internal MOSFET Source.  Buck converter operation—connect SOURCE2 to the switched side of the inductor as shown in Figure 1. Boost converter operation—connect SOURCE2 to the switched side of the inductor as shown in Figure 1. Boost converter operation—connect SOURCE2 to the switched side of the inductor as  | 15     | COMP1     | Compensation Connection for Converter 1 (See the Compensation Section)   |  |  |  |  |  |  |
| peration. Use EN1 in conjunction with EN2 for supply sequencing. Connect to VL for always-on operation.    DRAIN1  | 16     | FB1       | to program the output voltage. To set the output voltage below 0.8V, connect FB1 to a resistive voltage-   |  |  |  |  |  |  |
| Buck converter operation—use the MOSFET as a high-side switch and connect DRAIN1 to the input supply. Boost converter operation—use the MOSFET as a low-side switch and connect DRAIN1 to the inductor and diode junction.  BST1/VDD1  BST1/VDD1  Buck Converter Operation—Bootstrap Flying-Capacitor Connection for Converter 1. Connect BST1/VDD1 to an external ceramic capacitor and diode according to the Standard Application Circuit (Figure 1). Boost Converter Operation—Driver Bypass Capacitor Connection. Connect a low-ESR 0.1µF ceramic capacitor from BST1/VDD1 to PGND.  Converter 1 Power-Good Output. Open-drain output goes low when converter 1's output falls below 92.5% of its set regulation voltage. Use PGOOD1, PGOOD2, EN1, and EN2 to sequence the converters.  Converter 2 Power-Good Output. Open-drain output goes low when converter 2's output falls below 92.5% of its set regulation voltage.  Connection to the Converter 1 Internal MOSFET Source.  Buck converter operation—connect SOURCE1 to the switched side of the inductor as shown in Figure 1. Boost converter operation—connect SOURCE1 to PGND.  SGND  Signal Ground. Connect SGND to the exposed pad. Connect SGND and PGND together at a single point.  Power Ground. Connect rectifier diode anode, input capacitor negative, output capacitor negative, and VL bypass capacitor returns to PGND.  Connection to the Converter 2 Internal MOSFET Source. Buck converter operation—connect SOURCE2 to the switched side of the inductor as shown in Figure 1. Boost converter operation—connect SOURCE2 to the switched side of the inductor as shown in Figure 1. Boost converter operation—connect SOURCE2 to the switched side of the inductor as shown in Figure 1. Boost converter operation—connect SOURCE2 to the switched side of the inductor as shown in Figure 1. Boost converter operation—connect SOURCE2 to PGND (Figure 8).  | 17     | EN1       |  |  |  |  |  |  |  |
| to an external ceramic capacitor and diode according to the Standard Application Circuit (Figure 1). Boost Converter Operation—Driver Bypass Capacitor Connection. Connect a low-ESR 0.1μF ceramic capacitor from BST1/VDD1 to PGND.  PGOOD1 Converter 1 Power-Good Output. Open-drain output goes low when converter 1's output falls below 92.5% of its set regulation voltage. Use PGOOD1, PGOOD2, EN1, and EN2 to sequence the converters.  Converter 2 Power-Good Output. Open-drain output goes low when converter 2's output falls below 92.5% of its set regulation voltage.  Connection to the Converter 1 Internal MOSFET Source. Buck converter operation—connect SOURCE1 to the switched side of the inductor as shown in Figure 1. Boost converter operation—connect SOURCE1 to PGND.  SGND Signal Ground. Connect SGND to the exposed pad. Connect SGND and PGND together at a single point.  Power Ground. Connect rectifier diode anode, input capacitor negative, output capacitor negative, and VL bypass capacitor returns to PGND.  Connection to the Converter 2 Internal MOSFET Source. Buck converter operation—connect SOURCE2 to the switched side of the inductor as shown in Figure 1. Boost converter operation—connect SOURCE2 to the switched side of the inductor as shown in Figure 1. Boost converter operation—connect SOURCE2 to the switched side of the inductor as shown in Figure 1. Boost converter operation—connect SOURCE2 to PGND (Figure 8).  | 18, 19 | DRAIN1    | Buck converter operation—use the MOSFET as a high-side switch and connect DRAIN1 to the input supply.  Boost converter operation—use the MOSFET as a low-side switch and connect DRAIN1 to the inductor  |  |  |  |  |  |  |
| PGOOD1 92.5% of its set regulation voltage. Use PGOOD1, PGOOD2, EN1, and EN2 to sequence the converters.  PGOOD2 Converter 2 Power-Good Output. Open-drain output goes low when converter 2's output falls below 92.5% of its set regulation voltage.  Connection to the Converter 1 Internal MOSFET Source.  Buck converter operation—connect SOURCE1 to the switched side of the inductor as shown in Figure 1.  Boost converter operation—connect SOURCE1 to PGND.  Signal Ground. Connect SGND to the exposed pad. Connect SGND and PGND together at a single point.  Power Ground. Connect rectifier diode anode, input capacitor negative, output capacitor negative, and VL bypass capacitor returns to PGND.  Connection to the Converter 2 Internal MOSFET Source.  Buck converter operation—connect SOURCE2 to the switched side of the inductor as shown in Figure 1.  Boost converter operation—connect SOURCE2 to PGND (Figure 8).  | 20     | BST1/VDD1 | to an external ceramic capacitor and diode according to the Standard Application Circuit (Figure 1).  Boost Converter Operation—Driver Bypass Capacitor Connection. Connect a low-ESR 0.1µF ceramic  |  |  |  |  |  |  |
| 23, 24 SOURCE1  SOURCE3  SOURC   | 21     | PGOOD1    |  |  |  |  |  |  |  |
| 23, 24 SOURCE1 Buck converter operation—connect SOURCE1 to the switched side of the inductor as shown in Figure 1.  25 SGND Signal Ground. Connect SGND to the exposed pad. Connect SGND and PGND together at a single point.  26 PGND Power Ground. Connect rectifier diode anode, input capacitor negative, output capacitor negative, and VL bypass capacitor returns to PGND.  27, 28 SOURCE2 Connection to the Converter 2 Internal MOSFET Source.  Buck converter operation—connect SOURCE2 to the switched side of the inductor as shown in Figure 1.  Boost converter operation—connect SOURCE2 to PGND (Figure 8).  | 22     | PGOOD2    | , , , , , , , , , , , , , , , , , , ,  |  |  |  |  |  |  |
| PGND Power Ground. Connect rectifier diode anode, input capacitor negative, output capacitor negative, and VL bypass capacitor returns to PGND.  Connection to the Converter 2 Internal MOSFET Source.  Buck converter operation—connect SOURCE2 to the switched side of the inductor as shown in Figure 1.  Boost converter operation—connect SOURCE2 to PGND (Figure 8).   | 23, 24 | SOURCE1   | Buck converter operation—connect SOURCE1 to the switched side of the inductor as shown in Figure 1.  |  |  |  |  |  |  |
| VL bypass capacitor returns to PGND.  Connection to the Converter 2 Internal MOSFET Source.  Buck converter operation—connect SOURCE2 to the switched side of the inductor as shown in Figure 1.  Boost converter operation—connect SOURCE2 to PGND (Figure 8).  | 25     | SGND      | Signal Ground. Connect SGND to the exposed pad. Connect SGND and PGND together at a single point.  |  |  |  |  |  |  |
| 27, 28 SOURCE2 Buck converter operation—connect SOURCE2 to the switched side of the inductor as shown in Figure 1.  Boost converter operation—connect SOURCE2 to PGND (Figure 8).  | 26     | PGND      |  |  |  |  |  |  |  |
| EP SGND Exposed Paddle. Connect to SGND. Solder EP to the SGND plane for better thermal performance.   | 27, 28 | SOURCE2   | Buck converter operation—connect SOURCE2 to the switched side of the inductor as shown in Figure 1.  |  |  |  |  |  |  |
|  | EP     | SGND      | Exposed Paddle. Connect to SGND. Solder EP to the SGND plane for better thermal performance.   |  |  |  |  |  |  |

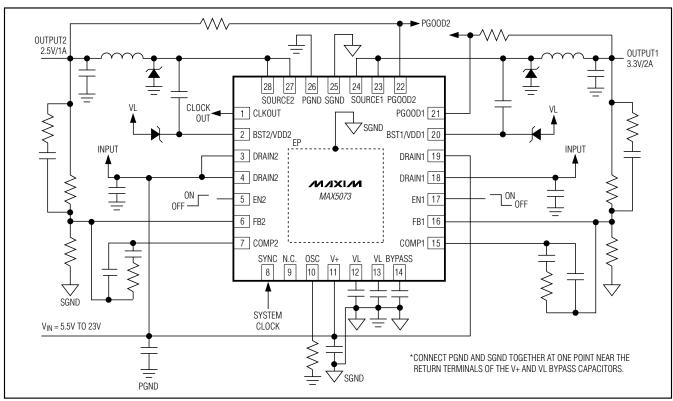


Figure 1. MAX5073 Dual Buck Regulator Application Circuit

#### **Detailed Description**

#### PWM Controller

The MAX5073 converter uses a pulse-width modulation (PWM) voltage-mode control scheme for each out-ofphase controller. It is nonsynchronous rectification and uses an external low-forward-drop Schottky diode for rectification. The controller generates the clock signal by dividing down the internal oscillator or the SYNC input when driven by an external clock, so each controller's switching frequency equals half the oscillator frequency (fsw = fosc / 2). An internal transconductance error amplifier produces an integrated error voltage at the COMP pin, providing high DC accuracy. The voltage at COMP sets the duty cycle using a PWM comparator and a ramp generator. At each rising edge of the clock, converter 1's high-side n-channel MOSFET turns on and remains on until either the appropriate or maximum duty cycle is reached, or the maximum current limit for the switch is detected. Converter 2 operates out-of-phase, so the second high-side MOSFET turns on at each falling edge of the clock.

In the case of buck operation (Figure 1), during each high-side MOSFET's on-time, the associated inductor cur-

rent ramps up. During the second half of the switching cycle, the high-side MOSFET turns off and forward biases the Schottky rectifier. During this time, the SOURCE voltage is clamped to 0.4V (VD) below ground. The inductor releases the stored energy as its current ramps down, and provides current to the output. The bootstrap capacitor is also recharged from the inductance energy when the MOSFET turns off. The circuit goes in discontinuous conduction mode operation at light load, when the inductor current completely discharges before the next cycle commences. Under overload conditions, when the inductor current exceeds the peak current limit of the respective switch, the high-side MOSFET turns off quickly and waits until the next clock cycle.

In the case of boost operation, the MOSFET is a low-side switch (Figure 8). During each on-time, the inductor current ramps up. During the second half of the switching cycle, the low-side switch turns off and forward biases the Schottky diode. During this time, the DRAIN voltage is clamped to 0.4V (VD) above VOUT\_ and the inductor provides energy to the output as well as replenishes the output capacitor charge.

#### Internal Oscillator/Out-of-Phase Operation

The internal oscillator generates the 180° out-of-phase clock signal required by each regulator. The internal oscillator frequency is programmable from 400kHz to 4.4MHz using a single 1% resistor at ROSC. Use the following equation to calculate ROSC:

$$R_{OSC} = \frac{25 \times 10^9}{f_{OSC}}$$

where fosc is the internal oscillator frequency in hertz and Rosc in ohms.

The two independent regulators in the MAX5073 switch 180° out-of-phase to reduce input filtering requirements, to reduce electromagnetic interference (EMI), and to improve efficiency. This effectively lowers component cost and saves board space, making the MAX5073 ideal for cost-sensitive applications.

With dual synchronized out-of-phase operation, the MAX5073's high-side MOSFETs turn on 180° out-of-phase. The instantaneous input current peaks of both regulators do not overlap, resulting in reduced RMS ripple current and input voltage ripple. This reduces the required input capacitor ripple current rating, allows for fewer or less expensive capacitors, and reduces shielding requirements for EMI. The out-of-phase waveforms in the *Typical Operating Characteristics* demonstrate synchronized 180° out-of-phase operation.

#### Synchronization (SYNC)/ Clock Output (CLKOUT)

The main oscillator can be synchronized to the system clock by applying an external clock (fsync) at SYNC. The fsync frequency must be twice the required operating frequency of an individual converter. Use a TTL logic signal for the external clock with at least a 100ns pulse width. Rosc is still required when using external synchronization. Program the internal oscillator frequency so 0.2fsync < fosc < 1.2fsync. The rising edge of fsync synchronizes the turn-on edge of the internal MOSFET (see Figure 3).

$$R_{OSC} = \frac{25 \times 10^9}{f_{OSC}}$$

where fosc is the internal oscillator frequency in hertz and Rosc in ohms, fosc =  $2 \times fsw$ .

Two MAX5073s can be connected in the master-slave configuration for four ripple-phase operation. The MAX5073 provides a clock output (CLKOUT) that is 45° phase-shifted with respect to the internal switch turn-on edge. Feed the CLKOUT of the master to the SYNC

input of the slave. The effective input ripple switching frequency shall be four times the individual converter's switching frequency. When driving the master converter using external clock at SYNC, set the clock duty cycle to 50% for a 90° phase-shifted operation.

#### Input Voltage (V+)/Internal Linear Regulator (VL)

All internal control circuitry operates from an internally regulated nominal voltage of 5.2V (VL). At higher input voltages (V+) of 5.5V to 23V, VL is regulated to 5.2V. At 5.5V or below, the internal linear regulator operates in dropout mode, where VL follows V+. Depending on the load on VL, the dropout voltage can be high enough to reduce VL below the undervoltage lockout (UVLO) threshold.

For input voltages of less than 5.5V, connect V+ and VL together. The load on VL is proportional to the switching frequency of converter 1 and converter 2. See the Dropout Voltage vs. Switching Frequency graph in the *Typical Operating Characteristics*. For input voltage ranges higher than 5.5V, use the internal regulator.

Bypass V+ to SGND with a low-ESR, 0.1µF or greater ceramic capacitor placed close to the MAX5073. Current spikes from VL may disturb internal circuitry powered by VL. Bypass VL with a low-ESR, ceramic 0.1µF capacitor to PGND and 4.7µF capacitor to SGND.

#### **Undervoltage Lockout/Soft-Start**

The MAX5073 includes an undervoltage lockout with hysteresis and a power-on-reset circuit for converter turn-on and monotonic rise of the output voltage. The rising UVLO threshold is internally set to 4.3V with a 175mV hysteresis. Hysteresis at UVLO eliminates "chattering" during startup. When VL drops below UVLO, the internal switches are turned off.

Digital soft-start is provided internally to reduce input surge currents and glitches at the input during turn-on. When UVLO is cleared and EN\_ is high, digital soft-start slowly ramps up the internal reference voltage in 64 steps. The total soft-start period is 2048 switching cycles of the internal oscillator.

To calculate the soft-start period, use the following equation:

$$t_{SS} = \frac{2048}{f_{OSC}}$$

where fosc is the internal oscillator frequency in hertz, which is twice the switching frequency of each converter.

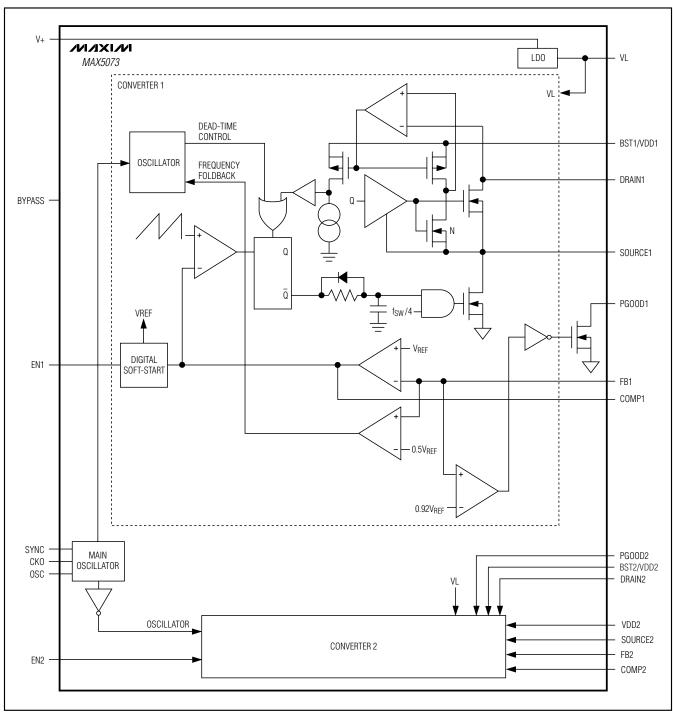


Figure 2. Functional Diagram

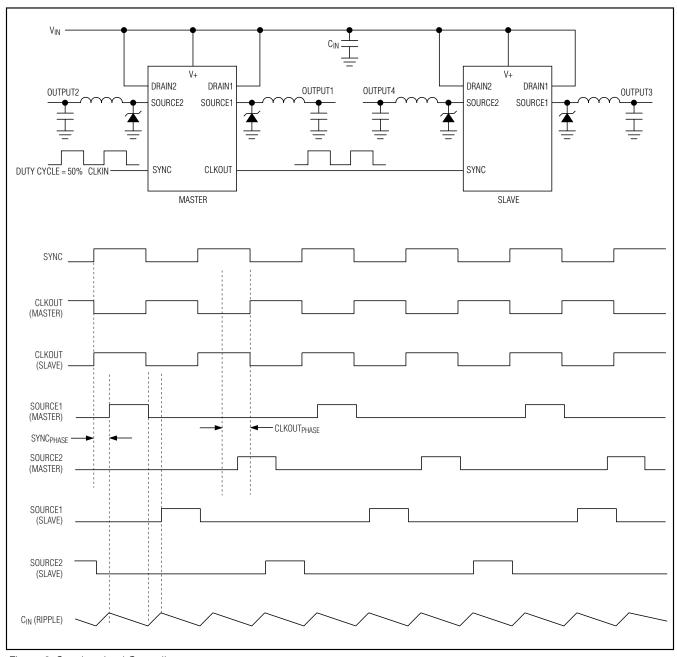


Figure 3. Synchronized Controllers

#### Enable

The MAX5073 dual converter provides separate enable inputs EN1 and EN2 to individually control or sequence the output voltages. These active-high enable inputs are TTL compatible. Pulling EN\_ high ramps up the reference slowly, which provides soft-start at the outputs. Forcing the EN\_ low externally disables the individual output and generates a PGOOD\_ signal. Use EN1, EN2, and PGOOD1 for sequencing (see Figure 4). Connect PGOOD1 to EN2 to make sure converter 1's output is within regulation before converter 2 starts. Add an RC network from VL to EN1 and EN2 to delay the individual converter. A larger RC time constant means a more delayed output. Sequencing reduces input inrush current and possible chattering. Connect the EN\_ to VL for always-on operation.

#### **PGOOD**

Converter 1 and converter 2 includes a power-good flag, PGOOD1 and PGOOD2, respectively. Since PGOOD is an open-drain output and can sink 3mA while providing the TTL logic-low signal, pull PGOOD to a logic voltage to provide a logic-level output. PGOOD goes low when converter 1's output drops to 92.5% of its nominal regulated voltage. Connect PGOOD to SGND or leave unconnected if not used.

#### **Current Limit**

The internal switch current of each converter is sensed using an internal current mirror. Converter 1 and converter 2 have 2A and 1A internal switches. When the peak switch current crosses the current-limit threshold of 3A (typ) and 1.8A (typ) for converter 1 and converter 2, respectively, the on cycle is terminated immediately and the inductor is allowed to discharge. The next cycle resumes at the next clock pulse.

In deep overload or short-circuit conditions when the FB voltage drops below 0.4V, the switching frequency is reduced to 1/4 x fsw to provide sufficient time for the inductor to discharge. During overload conditions, if the voltage across the inductor is not high enough to allow for the inductor current to properly discharge, current runaway may occur. Current runaway can destroy the device in spite of internal thermal-overload protection. Reducing the switching frequency during overload conditions prevents current runaway.

#### **Thermal-Overload Protection**

During continuous short circuit or overload at the output, the power dissipation in the IC can exceed its limit. Internal thermal shutdown is provided to avoid irreversible damage to the device. When the die temperature or junction temperature exceeds +150°C, an on-chip thermal sensor shuts down the device, forcing the internal switches to turn off, allowing the IC to cool. The thermal sensor turns the part on again after the junction temperature cools by +30°C. During thermal shutdown, both regulators shut down, PGOOD\_ go low, and soft-start resets.

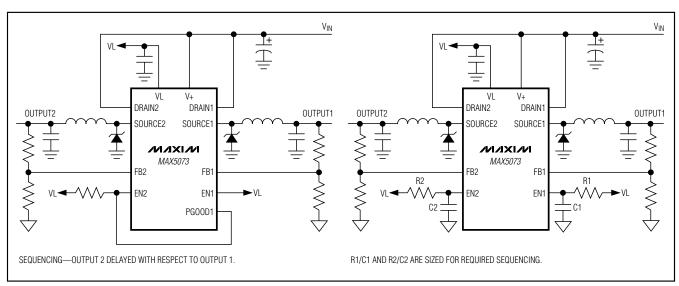


Figure 4. Power-Supply Sequencing Configurations

#### **Applications Information**

#### **Setting the Switching Frequency**

The controller generates the clock signal by dividing down the internal oscillator or the SYNC input signal when driven by an external oscillator. The switching frequency equals half the oscillator frequency (fsw = fosc / 2). The internal oscillator frequency is set by a resistor (Rosc) connected from OSC to SGND. The relationship between fsw and Rosc is:

$$R_{OSC} = \frac{12.5 \times 10^9}{f_{SW}}$$

where fsw and fosc are in hertz, and Rosc is in ohms. For example, a 1250kHz switching frequency is set with Rosc =  $10k\Omega$ . Higher frequencies allow designs with lower inductor values and less output capacitance. Consequently, peak currents and I²R losses are lower at higher switching frequencies, but core losses, gatecharge currents, and switching losses increase.

A rising clock edge on SYNC is interpreted as a synchronization input. If the SYNC signal is lost, the internal oscillator takes control of the switching rate, returning the switching frequency to that set by ROSC. This maintains output regulation even with intermittent SYNC signals. When an external synchronization signal is used, ROSC should be set for the oscillator frequency to be lower than or equal to the SYNC rate (fSYNC).

#### **Buck Converter**

#### Effective Input Voltage Range

Although the MAX5073 converters can operate from input supplies ranging from 5.5V to 23V, the input voltage range can be effectively limited by the MAX5073 duty-cycle limitations for a given output voltage. The maximum input voltage is limited by the minimum ontime (ton(MIN)):

$$V_{\text{IN(MAX)}} \le \frac{V_{\text{OUT}}}{t_{\text{ON(MIN)}} \times f_{\text{SW}}}$$

where  $t_{ON(MIN)}$  is 100ns. The minimum input voltage is limited by the maximum duty cycle (DMAX = 0.88):

$$V_{\text{IN(MIN)}} = \left[\frac{V_{\text{OUT}} + V_{\text{DROP1}}}{0.88}\right] + V_{\text{DROP2}} - V_{\text{DROP1}}$$

where V<sub>DROP1</sub> is the total parasitic voltage drops in the inductor discharge path, which includes the forward voltage drop (V<sub>D</sub>) of the rectifier, the series resistance of the inductor, and the PC board resistance. V<sub>DROP2</sub> is the total resistance in the charging path, which includes the on-resistance of the high-side switch, the series resistance of the inductor, and the PC board resistance.

#### Setting the Output Voltage

For 0.8V or greater output voltages, connect a voltage-divider from OUT\_ to FB\_ to SGND (Figure 5). Select RB (FB\_ to SGND resistor) to between 1k $\Omega$  and 10k $\Omega$ . Calculate RA (OUT\_ to FB\_ resistor) with the following equation:

$$R_A = R_B \left[ \left( \frac{V_{OUT}}{V_{FB}} \right) - 1 \right]$$

where  $V_{FB}$  = 0.8V (see the *Electrical Characteristics* table) and  $V_{OUT}$  can range from  $V_{FB}$  to 28V (boost operation).

For output voltages below 0.8V, set the MAX5073 output voltage by connecting a voltage-divider from the output to FB\_ to BYPASS (Figure 5). Select Rc (FB to BYPASS resistor) higher than a  $50k\Omega$  range. Calculate RA with the following equation:

$$R_{A} = R_{C} \left[ \frac{V_{FB} - V_{OUT}}{V_{BYPASS} - V_{FB}} \right]$$

where VFB = 0.8V, VBYPASS = 2V (see the *Electrical Characteristics* table), and VOUT\_ can range from 0V to VFB .

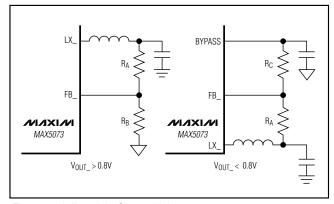


Figure 5. Adjustable Output Voltage

#### Inductor Selection

Three key inductor parameters must be specified for operation with the MAX5073: inductance value (L), peak inductor current (IL), and inductor saturation current (ISAT). The minimum required inductance is a function of operating frequency, input-to-output voltage differential and the peak-to-peak inductor current ( $\Delta I_{\perp}$ ). Higher  $\Delta I_{\perp}$ allows for a lower inductor value while a lower  $\Delta I_1$ requires a higher inductor value. A lower inductor value minimizes size and cost, improves large-signal transient response, but reduces efficiency due to higher peak currents and higher peak-to-peak output ripple voltage for the same output capacitor. On the other hand, higher inductance increases efficiency by reducing the ripple current. However, resistive losses due to extra wire turns can exceed the benefit gained from lower ripple current levels, especially when the inductance is increased without also allowing for larger inductor dimensions. A good compromise is to choose  $\Delta I_{\perp}$  equal to 30% of the full load current. To calculate the inductance use the following equation:

$$L = \frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_{L}}$$

where V<sub>IN</sub> and V<sub>OUT</sub> are typical values (so that efficiency is optimum for typical conditions). The switching frequency is set by R<sub>OSC</sub> (see the *Setting the Switching Frequency* section). The peak-to-peak inductor current, which reflects the peak-to-peak output ripple, is worse at the maximum input voltage. See the *Output Capacitor Selection* section to verify that the worst-case output ripple is acceptable. The inductor saturating current is also important to avoid runaway current during output overload and continuous short circuit. Select the I<sub>SAT</sub> to be higher than the maximum peak current limits of 4.5A and 2.2A for converter 1 and converter 2.

#### Input Capacitors

The discontinuous input current waveform of the buck converter causes large ripple currents at the input. The switching frequency, peak inductor current, and the allowable peak-to-peak voltage ripple dictate the input capacitance requirement. Increasing the switching frequency or the inductor value lowers the peak to average current ratio, yielding a lower input capacitance requirement. Note that two converters of MAX5073 run 180° out-of-phase, thereby effectively doubling the switching frequency at the input.

The input ripple waveform would be unsymmetrical due to the difference in load current and duty cycle between converter 1 and converter 2. The input ripple is comprised of  $\Delta V_Q$  (caused by the capacitor discharge) and  $\Delta V_{ESR}$  (caused by the ESR of the capacitor). A higher load converter dictates the ESR requirement, while the capacitance requirement is a function of the loading mismatch between the two converters. The worst-case mismatch is when one converter is at full load while the other is at no load or in shutdown. Use low-ESR ceramic capacitors with high ripple-current capability at the input. Assume the contribution from the ESR and capacitor discharge equal to 50%. Calculate the input capacitance and ESR required for a specified ripple using the following equations:

$$ESR_{IN} = \frac{\Delta V_{ESR}}{\left(I_{OUT} + \frac{\Delta I_{L}}{2}\right)}$$

where

$$\Delta I_{L} = \frac{\left(V_{IN} - V_{OUT}\right) \times V_{OUT}}{V_{IN} \times f_{SW} \times L}$$

and

$$C_{IN} = \frac{I_{OUT} \times D(1-D)}{\Delta V_{O} \times f_{SW}}$$

where

$$D = \frac{V_{OUT}}{V_{IN}}$$

where I<sub>OUT</sub> is the maximum output current from either converter 1 or converter 2, and D is the duty cycle for that converter. fsw is the frequency of each individual converter. For example, at V<sub>IN</sub> = 12V, V<sub>OUT</sub> = 3.3V at I<sub>OUT</sub> = 2A, and with L = 3.3  $\mu$ H, the ESR and input capacitance are calculated for a peak-to-peak input ripple of 100mV or less, yielding an ESR and capacitance value of 20m $\Omega$  and 6.8  $\mu$ F for 1.25MHz frequency. Use a 100  $\mu$ F capacitor at low input voltages to avoid possible undershoot below the undervoltage lockout threshold during power-on and transient loading.

#### **Output Capacitors**

The allowable output ripple voltage and the maximum deviation of the output voltage during step load currents determines the output capacitance and its ESR.

The output ripple is comprised of  $\Delta V_Q$  (caused by the capacitor discharge) and  $\Delta V_{ESR}$  (caused by the ESR of the capacitor). Use low-ESR ceramic or aluminum electrolytic capacitors at the output. For aluminum electrolytic capacitors, the entire output ripple is contributed by  $\Delta V_{ESR}.$  Use the ESROUT equation to calculate the ESR requirement and choose the capacitor accordingly. If using ceramic capacitors, assume the contribution to the output ripple voltage from the ESR and the capacitor discharge are equal. Calculate the output capacitance and ESR required for a specified ripple using the following equations:

$$\mathsf{ESR}_{\mathsf{OUT}} = \frac{\Delta \mathsf{V}_{\mathsf{ESR}}}{\Delta \mathsf{I}_{\mathsf{I}}}$$

$$C_{OUT} = \frac{\Delta I_L}{8 \times \Delta V_O \times f_{SW}}$$

where

$$\Delta V_{O_RIPPLE} \cong \Delta V_{ESR} + \Delta V_{Q}$$

where  $\Delta I_L$  is the peak-to-peak inductor current as calculated above and fsw is the individual converter's switching frequency.

The allowable deviation of the output voltage during fast transient loads also determines the output capacitance and its ESR. The output capacitor supplies the step load current until the controller responds with a greater duty cycle. The response time (tresponse) depends on the closed-loop bandwidth of the converter. The high switching frequency of MAX5073 allows for higher closed-loop bandwidth, reducing tresponse and the output capacitance requirement. The resistive drop across the output capacitor ESR and the capacitor discharge causes a voltage droop during a step load. Use a combination of low-ESR tantalum and ceramic capacitors for better transient load and ripple/noise performance. Keep the maximum output voltage deviation above the tolerable limits of the electronics

being powered. When using a ceramic capacitor, assume 80% and 20% contribution from the output capacitance discharge and the ESR drop, respectively. Use the following equations to calculate the required ESR and capacitance value:

$$ESR_{OUT} = \frac{\Delta V_{ESR}}{I_{STEP}}$$

$$C_{OUT} = \frac{I_{STEP} \times t_{RESPONSE}}{\Delta V_{O}}$$

where ISTEP is the load step and tRESPONSE is the response time of the controller. Controller response time depends on the control-loop bandwidth.

#### **Boost Converter**

The MAX5073 can be configured for step-up conversion since the internal MOSFET can be used as a low-side switch. Use the following equations to calculate the inductor ( $L_{MIN}$ ), input capacitor ( $C_{IN}$ ), and output capacitor ( $C_{OUT}$ ) when using the converter in boost operation.

#### Inductor

Choose the minimum inductor value so the converter remains in continuous mode operation at minimum output current (IOMIN).

$$L_{MIN} = \frac{V^2|_{N} \times D \times \eta}{2 \times f_{SW} \times V_{O} \times I_{OMIN}}$$

where

$$D = \frac{V_{O} + V_{D} - V_{IN}}{V_{O} + V_{D} - V_{DS}}$$

and  $IOMIN = 0.25 \times IO$ 

The V<sub>D</sub> is the forward voltage drop of the external Schottky diode, D is the duty cycle, and V<sub>DS</sub> is the voltage drop across the internal switch. Select the inductor with low DC resistance and with a saturation current (ISAT) rating higher than the peak switch current limit of 4.5A and 2.2A of converter 1 and converter 2, respectively.

#### Input Capacitor

The input current for the boost converter is continuous and the RMS ripple current at the input is low. Calculate the capacitor value and ESR of the input capacitor using the following equations.

$$C_{IN} = \frac{\Delta I_L \times D}{4 \times f_{SW} \times \Delta V_O}$$

$$ESR = \frac{\Delta V_{ESR}}{\Delta I_{L}}$$

where

$$\Delta I_L = \frac{(V_{IN} - V_{DS}) \times D}{L \times f_{SW}}$$

where VDS is the total voltage drop across the internal MOSFET plus the voltage drop across the inductor ESR.  $\Delta I_L$  is the peak-to-peak inductor ripple current as calculated above.  $\Delta V_Q$  is the portion of input ripple due to the capacitor discharge and  $\Delta V_{ESR}$  is the contribution due to ESR of the capacitor.

#### **Output Capacitor**

For the boost converter, the output capacitor supplies the load current when the main switch is ON. The required output capacitance is high, especially at higher duty cycles. Also, the output capacitor ESR needs to be low enough to minimize the voltage drop due to the ESR while supporting the load current. Use the following equation to calculate the output capacitor for a specified output ripple tolerance.

$$ESR = \frac{\Delta V_{ESR}}{I_{O}}$$

$$C_{OUT} = \frac{I_O \times D_{MAX}}{\Delta V_Q \times f_{SW}}$$

I<sub>Q</sub> is the load current,  $\Delta V_Q$  is the portion of the ripple due to the capacitor discharge and  $\Delta V_{ESR}$  is the contribution due to the ESR of the capacitor. DMAX is the maximum duty cycle at minimum input voltage.

#### **Power Dissipation**

The MAX5073 includes a high-frequency, low RDS\_ON switching MOSFET. At +85°C, the RDS\_ON of the internal switch for converter 1 and converter 2 are  $290m\Omega$  and  $630m\Omega$ , respectively. The DC loss is a function of the RMS current in the switch while the switching loss is a function of switching frequency and input voltage. Use

the following equations to calculate the RMS current, DC loss, and switching loss of each converter. The MAX5073 device is available in a thermally enhanced package and can dissipate up to 2.7W at +70°C ambient temperature. The total power dissipation in the package must be limited so the junction temperature does not exceed its absolute maximum rating of +150°C at maximum ambient temperature.

For the buck converter:

$$I_{RMS} = \sqrt{(I_{DC}^2 + I_{PK}^2 + (I_{DC} \times I_{PK})) \times \frac{D_{MAX}}{3}}$$

$$P_{DC} = I_{RMS}^2 \times R_{DS(ON)MAX}$$

where

$$I_{DC} = I_{O} - \frac{\Delta I_{L}}{2}$$

$$I_{PK} = I_O + \frac{\Delta I_L}{2}$$

See the *Electrical Characteristics* table for the RDS(ON)MAX value.

$$P_{SW} = \frac{V_{INMAX} \times I_{O} \times (t_{R} + t_{F}) \times f_{SW}}{4}$$

For the boost converter:

$$I_{RMS} = \sqrt{(I_{DC}^2 + I_{PK}^2 + (I_{DC} \times I_{PK})) \times \frac{D_{MAX}}{3}}$$

$$I_{|N|} = \frac{V_O \times I_O}{V_{|N|} \times \eta}$$

$$\Delta I_{L} = \frac{\left(V_{IN} - V_{DS}\right) \times D}{L \times f_{SW}}$$

$$I_{DC} = I_{IN} - \frac{\Delta I_{L}}{2}$$

$$I_{PK} = I_{IN} + \frac{\Delta I_{L}}{2}$$

$$P_{DC} = I_{RMS}^2 \times R_{DS(ON)MAX}$$

where V<sub>DS</sub> is the drop across the internal MOSFET. See the *Electrical Characteristics* for the R<sub>DS</sub>(ON)MAX value.

$$P_{SW} = \frac{V_O \times I_{|N|} \times (t_R + t_F) \times f_{SW}}{4}$$

where  $t_{\rm R}$  and  $t_{\rm F}$  are rise and fall times of the internal MOSFET. The  $t_{\rm R}$  and  $t_{\rm F}$  are typically 20ns, and can be measured in the actual application.

The supply current in the MAX5073 is dependent on the switching frequency. See the *Typical Operating Characteristics* to find the supply current of the MAX5073 at a given operating frequency. The power dissipation (Ps) in the device due to supply current (Is) is calculated using following equation.

$$P_S = V_{INMAX} \times I_{SUPPLY}$$

The total power dissipation P<sub>T</sub> in the device is:

where P<sub>DC1</sub> and P<sub>DC2</sub> are DC losses in converter 1 and converter 2, respectively. Psw<sub>1</sub> and Psw<sub>2</sub> are switching losses in converter 1 and converter 2.

Calculate the temperature rise of the die using the following equation:

$$T_J = T_C + (P_T \times \theta_{JC})$$

where,  $\theta_{JC}$  is the junction-to-case thermal impedance of the package equal to +2°C/W. Solder the exposed pad of the package to a large copper area to minimize the case-to-ambient thermal impedance. Measure the temperature of the copper area near the device at a worst-case condition of power dissipation and use +2°C/W as  $\theta_{JC}$  thermal impedance. The case-to-ambient thermal impedance ( $\theta_{C-A}$ ) is dependent on how well the heat is transferred from the PC board to the ambient. Use a large copper area to keep the PC board temperature low. The  $\theta_{C-A}$  is usually in the +20°C/W to +40°C/W range .

#### Compensation

The MAX5073 provides an internal transconductance amplifier with its inverting input and its output available to the user for external frequency compensation. The flexibility of external compensation for each converter offers wide selection of output filtering components, especially the output capacitor. For cost-sensitive applications, use high-ESR aluminum electrolytic capacitors; for component size-sensitive applications, use low-ESR tantalum or ceramic capacitors at the out-

put. The high switching frequency of MAX5073 allows use of ceramic capacitors at the output.

Choose all the passive power components that meet the output ripple, component size, and component cost requirements. Choose the small-signal components for the error amplifier to achieve the desired closed-loop bandwidth and phase margin. Use a simple pole-zero pair (Type II) compensation if the output capacitor ESR zero frequency is below the unity-gain crossover frequency (fc). Type III compensation is necessary when the ESR zero frequency is higher than fc or when compensating for a continuous mode boost converter that has a right-half-plane zero.

Use the following procedure 1 to calculate the compensation network components when fZERO,ESR < fC.

## **Buck Converter Compensation Procedure 1 (See Figure 6)**

1) Calculate the fzero.esr and LC double pole:

$$f_{ZERO, ESR} = \frac{1}{2\pi \times ESR \times C_{OUT}}$$

$$f_{LC} = \frac{1}{2\pi \times \sqrt{L_{OUT} \times C_{OUT}}}$$

2) Calculate the unity-gain crossover frequency as:

$$f_C = \frac{f_{SW}}{20}$$

If the fZERO,ESR is lower than fC and close to fLC, use a Type II compensation network where RFCF provides a midband zero f<sub>mid,Zero</sub>, and RFCCF provides a high-frequency pole.

3) Calculate modulator gain G<sub>M</sub> at the crossover frequency.

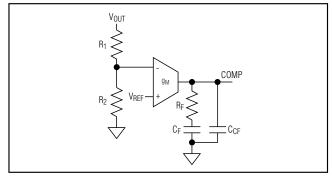


Figure 6. Type II Compensation Network

# *MAX5073*

## 2.2MHz, Dual-Output Buck or Boost Converter with Internal Power MOSFETs

$$G_{M} = \frac{V_{IN}}{V_{OSC}} \times \frac{ESR}{ESR + (2\pi \times f_{C} \times L_{OUT})} \times \frac{0.8}{V_{OUT}}$$

where Vosc is a peak-to-peak ramp amplitude equal

The transconductance error amplifier gain is:

$$G_{F/A} = g_m \times R_F$$

The total loop gain at fc should be equal to 1

$$G_M \times G_{F/A} = 1$$

or

$$R_{F} = \frac{V_{OSC} (ESR + 2\pi \times f_{C} \times L_{OUT})V_{OUT}}{0.8 \times V_{IN} \times g_{m} \times ESR}$$

4) Place a zero at or below the LC double pole:

$$C_{F} = \frac{1}{2\pi \times R_{F} \times f_{IC}}$$

5) Place a high-frequency pole at  $f_P = 0.5 \times f_{SW}$ .

#### Procedure 2 (see Figure 7)

If the output capacitor used is a low-ESR ceramic type, the ESR frequency is usually far away from the targeted unity crossover frequency (fc). In this case, Type III compensation is recommended. Type III compensation provides two-pole zero pairs. The locations of the zero and poles should be such that the phase margin peaks at fc.

$$\frac{f_C}{f_C} = \frac{f_P}{f_C} = 5$$

 $\frac{f_C}{f_Z} = \frac{f_P}{f_C} = 5$  is a good number to get about 60° phase margin at fc. However, it is important to place the two zeros at or below the double pole to avoid the conditional stability issue.

1) Select a crossover frequency:

$$f_C \le \frac{f_{SW}}{20}$$

2) Calculate the LC double-pole frequency, fLC:

$$f_{LC} = \frac{1}{2\pi \times \sqrt{L_{OUT} \times C_{OUT}}}$$

3) Place a zero

$$f_Z = \frac{1}{2\pi \times R_E \times C_E}$$
 at 0.75 ×  $f_{LC}$ 

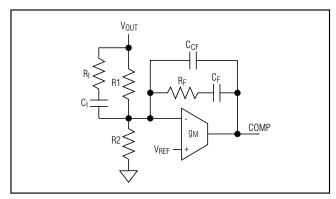


Figure 7. Type III Compensation Network

where:

$$C_{F} = \frac{1}{2\pi \times 0.75 \times f_{IC} \times R_{F}}$$

and R<sub>F</sub>  $\geq$  10k $\Omega$ .

4) Calculate C<sub>I</sub> for a target unity crossover frequency, fc:

$$C_{I} = \frac{2\pi \times f_{C} \times L_{OUT} \times C_{OUT} \times V_{OSC}}{V_{IN} \times R_{F}}$$

(f<sub>P1</sub> =  $\frac{1}{2\pi \times R_l \times C_l}$ )
5) Place a pole (f<sub>P1</sub> =  $\frac{1}{2\pi \times R_l \times C_l}$ ) at fzero.esr.

$$R_{I} = \frac{1}{2\pi \times f_{ZERO, ESR} \times C_{I}}$$

6) Place a second zero, fz2, at 0.2 x fc or at fcc, whichever is lower.

$$R1 = \frac{1}{2\pi \times f_{Z2} \times C_I} - R_I$$

7) Place a second pole  $(f_{P2} = \frac{1}{2\pi \times R_F \times C_{CF}})$  at 1/2 the switching frequency.

$$C_{CF} = \frac{C_F}{(2\pi \times 0.5 \times f_{SW} \times R_F \times C_F) - 1}$$

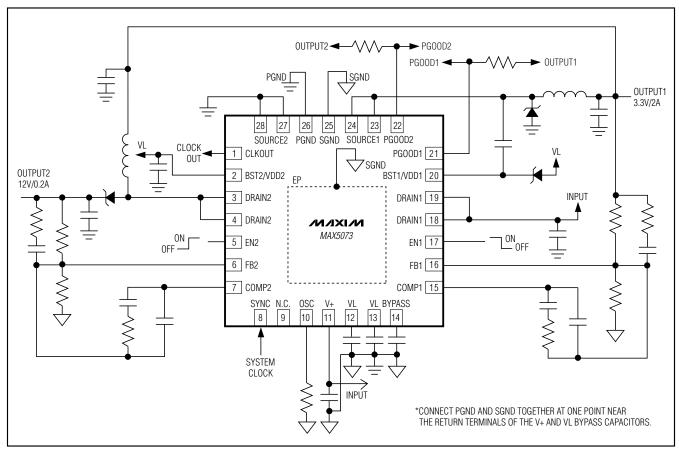


Figure 8. Buck-Boost Application

#### **Boost Converter Compensation**

The boost converter compensation gets complicated due to the presence of a right-half-plane zero fzero, RHP. The right-half-plane zero causes a drop in-phase while adding positive (+1) slope to the gain curve. It is important to drop the gain significantly below unity before the RHP frequency. Use the following procedure to calculate the compensation components.

1) Calculate the LC double-pole frequency, F<sub>LC</sub>, and the right half plane zero frequency.

$$f_{LC} = \frac{1 - D}{2\pi \times \sqrt{L_{OUT}C_{OUT}}}$$
$$f_{ZERO,RHP} = \frac{(1 - D)^2 R_{(MIN)}}{2\pi \times L_{OUT}}$$

where:

$$D = 1 - \frac{V_{IN}}{V_{OUT}}$$

$$R_{(MIN)} = \frac{V_{OUT}}{I_{OUT(MAX)}}$$

Target the unity-gain crossover frequency for:

$$f_{C} \le \frac{f_{ZERO,RHP}}{5}$$
2) Place a zero 
$$(f_{Z1} = \frac{1}{2\pi \times R_{F} \times C_{F}}) \text{ at } 0.75 \times f_{LC}.$$

$$C_{F} = \frac{1}{2\pi \times 0.75 \times f_{LC} \times R_{F}}$$

where R<sub>F</sub>  $\geq$  10k $\Omega$ .

3) Calculate C<sub>I</sub> for a target crossover frequency, fc:

$$C_{I} = \frac{V_{OSC} \left[ \left( 1 - D \right)^{2} + \omega_{C}^{2} L_{O} C_{O} \right]}{\omega_{C} R_{F} V_{IN}}$$

where  $\omega_{\rm C} = 2\pi$  fc

4) Place a pole  $(f_{P1} = \frac{1}{2\pi \times R_I \times C_I})$  at fZERO,RHP.

$$R_{I} = \frac{1}{2\pi \times f_{ZERO}, R_{HP} \times C_{I}}$$

5) Place the second zero  $(f_{Z2} = \frac{1}{2\pi \times R1 \times C_I})$  at fLC.

$$R1 = \frac{1}{2\pi \times f_{LC} \times C_{I}} - R_{I}$$

(f<sub>P2</sub> =  $\frac{1}{2\pi \times R_F \times C_{CF}}$  at 1/2 the switching frequency.

$$C_{CF} = \frac{C_F}{(2\pi \times 0.5 \times f_{SW} \times R_F \times C_F) - 1}$$

#### **Improving Noise Immunity**

In applications where the MAX5073 are subject to noisy environments, adjust the controller's compensation to improve the system's noise immunity. In particular, high-frequency noise coupled into the feedback loop causes jittery duty cycles. One solution is to lower the crossover frequency (see the *Compensation* section).

#### **PC Board Layout Guidelines**

Careful PC board layout is critical to achieve low switching losses and clean, stable operation. This is especially true for dual converters where one channel can affect the other. Refer to the MAX5073 EV kit data sheet for a specific layout example. Use a multilayer board whenever possible for better noise immunity. Follow these guidelines for good PC board layout:

 For SGND, use a large copper plane under the IC and solder it to the exposed paddle. To effectively use this copper area as a heat exchanger between the PC board and ambient, expose this copper area

- on the top and bottom side of the PC board. Do not make a direct connection from the exposed pad copper plane to SGND (pin 25) underneath the IC.
- 2) Isolate the power components and high-current path from the sensitive analog circuitry.
- Keep the high-current paths short, especially at the ground terminals. This practice is essential for stable, jitter-free operation.
- 4) Connect SGND and PGND together close to the IC at the ground terminals of VL and V+ bypass capacitors. Do not connect them together anywhere else.
- 5) Keep the power traces and load connections short. This practice is essential for high efficiency. Use thick copper PC boards (2oz vs. 1oz) to enhance full-load efficiency.
- Ensure that the feedback connection to Cout is short and direct.
- 7) Route high-speed switching nodes (BST\_/VDD\_, SOURCE\_) away from the sensitive analog areas (BYPASS, COMP\_, and FB\_). Use the internal PC board layer for SGND as EMI shields to keep radiated noise away from the IC, feedback dividers, and analog bypass capacitors.

#### **Layout Procedure**

- 1) Place the power components first, with ground terminals adjacent (inductor, C<sub>IN</sub>\_, and C<sub>OUT</sub>\_). Make all these connections on the top layer with wide, copper-filled areas (2oz copper recommended).
- 2) Group the gate-drive components (bootstrap diodes and capacitors, and VL bypass capacitor) together near the controller IC.
- 3) Make the DC-DC controller ground connections as follows:

- a) Create a small-signal ground plane underneath the IC.
- b) Connect this plane to SGND and use this plane for the ground connection for the reference (BYPASS), enable, compensation components, feedback dividers, and OSC resistor.
- c) Connect SGND and PGND together near the input bypass capacitors and the IC (this is the only connection between SGND and PGND).

#### Ordering Information (continued)

| PART        | TEMP RANGE      | PIN-PACKAGE                    | PKG<br>CODE |  |  |
|-------------|-----------------|--------------------------------|-------------|--|--|
| MAX5073ATI  | -40°C to +125°C | 28 Thin QFN-EP*<br>(5mm x 5mm) | T2855-6     |  |  |
| MAX5073ATI+ | -40°C to +125°C | 28 Thin QFN-EP*<br>(5mm x 5mm) | T2855-6     |  |  |

<sup>\*</sup>EP = Exposed pad.

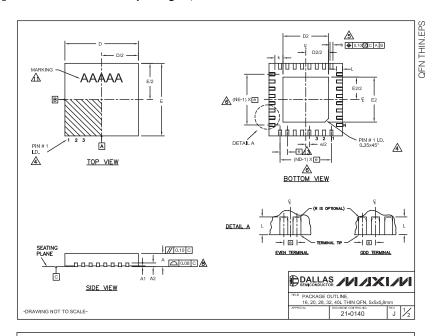
#### \_Chip Information

TRANSISTOR COUNT: 5994 PROCESS: BICMOS

<sup>+</sup>Denotes lead-free package.

#### **Package Information**

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to www.maxim-ic.com/packages.)



|        |      |       | С             | OMM       | ON D | IMEN      | SION   | S         |        |           |          |      |         |      |   |
|--------|------|-------|---------------|-----------|------|-----------|--------|-----------|--------|-----------|----------|------|---------|------|---|
| PKG.   | 1    | 6L 5x | :5            | 2         | 0L 5 | ¢5        | 2      | 8L 5:     | κ5     | 3         | 2L 5     | ι5   | 40L 5x5 |      |   |
| SYMBOL | MIN. | NOM.  | MAX.          | MIN.      | NOM. | MAX.      | MIN.   | NOM.      | MAX.   | MIN.      | NOM.     | MAX. | MIN.    | NOM. | ľ |
| A      | 0.70 | 0.75  | 0.80          | 0.70      | 0.75 | 0.80      | 0.70   | 0.75      | 0.80   | 0.70      | 0.75     | 0.80 | 0.70    | 0.75 | I |
| A1     | 0    | 0.02  | 0.05          | 0         | 0.02 | 0.05      | 0      | 0.02      | 0.05   | 0         | 0.02     | 0.05 | 0       | 0.02 | þ |
| A2     | 0.   | 20 RE | EF. 0.20 REF. |           |      | 0.20 REF. |        | 0.20 REF. |        | 0.20 REF. |          |      |         |      |   |
| b      | 0.25 | 0.30  | 0.35          | 0.25      | 0.30 | 0.35      | 0.20   | 0.25      | 0.30   | 0.20      | 0.25     | 0.30 | 0.15    | 0.20 | С |
| D      | 4.90 | 5.00  | 5.10          | 4.90      | 5.00 | 5.10      | 4.90   | 5.00      | 5.10   | 4.90      | 5.00     | 5.10 | 4.90    | 5.00 | 5 |
| E      | 4.90 | 5.00  | 5.10          | 4.90      | 5.00 | 5.10      | 4.90   | 5.00      | 5.10   | 4.90      | 5.00     | 5.10 | 4.90    | 5.00 | £ |
| 6      | 0    | .80 B | SC.           | 0.65 BSC. |      | 0.50 BSC. |        | 0.50 BSC. |        | SC.       | 0.40 BS0 |      |         |      |   |
| k      | 0.25 | -     | -             | 0.25      | -    | -         | 0.25   | -         | -      | 0.25      | -        | -    | 0.25    | -    |   |
| L      | 0.30 | 0.40  | 0.50          | 0.45      | 0.55 | 0.65      | 0.45   | 0.55      | 0.65   | 0.30      | 0.40     | 0.50 | 0.30    | 0.40 | o |
| N      | 16   |       | 20            |           | 28   |           | 32     |           | 40     |           |          |      |         |      |   |
| ND     | 4    |       |               | 5         |      |           | 7      |           |        | 8         |          |      | 10      | Ξ    |   |
| NE     | 4    |       |               | 5         |      |           | 7      |           |        | 8         |          |      | 10      | Τ    |   |
| JEDEC  | WHHB |       |               | WHHC      |      | 1         | WHHD-1 |           | WHHD-2 |           |          |      |         |      |   |

| PKG.     |      | D2   |      | E2   |      |      |  |  |
|----------|------|------|------|------|------|------|--|--|
| CODES    | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |  |  |
| T1655-2  | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |  |  |
| T1655-3  | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |  |  |
| T1655N-1 | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3,20 |  |  |
| T2055-3  | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |  |  |
| T2055-4  | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |  |  |
| T2055-5  | 3.15 | 3.25 | 3.35 | 3.15 | 3.25 | 3.35 |  |  |
| T2855-3  | 3.15 | 3.25 | 3.35 | 3.15 | 3.25 | 3.35 |  |  |
| T2855-4  | 2.60 | 2.70 | 2.80 | 2.60 | 2.70 | 2.80 |  |  |
| T2855-5  | 2.60 | 2.70 | 2.80 | 2.60 | 2.70 | 2.80 |  |  |
| T2855-6  | 3.15 | 3.25 | 3.35 | 3.15 | 3.25 | 3.35 |  |  |
| T2855-7  | 2.60 | 2.70 | 2.80 | 2.60 | 2.70 | 2.80 |  |  |
| T2855-8  | 3.15 | 3.25 | 3.35 | 3.15 | 3.25 | 3.35 |  |  |
| T2855N-1 | 3.15 | 3.25 | 3,35 | 3.15 | 3.25 | 3.35 |  |  |
| T3255-3  | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |  |  |
| T3255-4  | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |  |  |
| T3255-5  | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |  |  |
| T3255N-1 | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |  |  |

EXPOSED PAD VARIATIONS

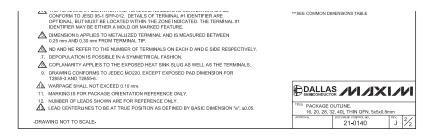
NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.

2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.

#### **Package Information (continued)**

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <a href="https://www.maxim-ic.com/packages">www.maxim-ic.com/packages</a>.)



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