

NYC0102BLT1G

Sensitive Gate Silicon Controlled Rectifiers Reverse Blocking Thyristors

Designed and tested for highly-sensitive triggering in low-power switching applications.

Features

- High dv/dt
- Gating Current < 200 μ A
- Miniature SOT-23 Package for High Density PCB
- SZ Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Repetitive Off-State Voltage (Note 1) ($R_{GK} = 1\text{K}$, $T_J = -40$ to $+110^\circ\text{C}$, Sine Wave, 50 to 60 Hz)	V_{DRM} , V_{RRM}	200	V
On-State Current RMS (180° Conduction Angle, $T_C = 80^\circ\text{C}$)	$I_{T(RMS)}$	0.25	A
Peak Non-repetitive Surge Current, $T_A = 25^\circ\text{C}$, (1/2 Cycle, Sine Wave, 60 Hz)	I_{TSM}	7.0	A
Circuit Fusing Considerations ($t = 8.3$ ms)	I^2t	0.2	A^2s
Forward Peak Gate Power (Pulse Width ≤ 1.0 μsec , $T_A = 25^\circ\text{C}$)	P_{GM}	0.1	W
Forward Average Gate Power ($t = 8.3$ msec, $T_A = 25^\circ\text{C}$)	$P_{G(AV)}$	0.02	W
Forward Peak Gate Current (Pulse Width ≤ 20 μs , $T_A = 25^\circ\text{C}$)	I_{FGM}	0.5	A
Reverse Peak Gate Voltage (Pulse Width ≤ 1.0 μs , $T_A = 25^\circ\text{C}$)	V_{RGM}	8.0	V
Operating Junction Temperature Range @ Rated V_{RRM} and V_{DRM}	T_J	-40 to +125	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-40 to +150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation FR-5 Board $T_A = 25^\circ\text{C}$	P_D	225	mW
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	380	$^\circ\text{C/W}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

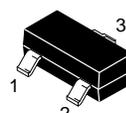
1. V_{DRM} and V_{RRM} for all types can be applied on a continuous basis. Ratings apply for zero or negative gate voltage; however, positive gate voltage shall not be applied concurrent with negative potential on the anode. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the devices are exceeded.



ON Semiconductor®

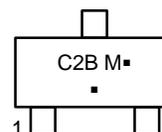
<http://onsemi.com>

0.25 AMP, 200 VOLT SCRs



SOT-23
CASE 318
STYLE 8

MARKING DIAGRAM



C2B = Specific Device Code
M = Date Code*
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or overbar may vary depending upon manufacturing location.

PIN ASSIGNMENT

Pin	Assignment
1	Cathode
2	Gate
3	Anode

ORDERING INFORMATION

Device	Package	Shipping†
NYC0102BLT1G	SOT-23 (Pb-Free)	3000 / Tape & Reel
SZNYC0102BLT1G	SOT-23 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NYC0102BLT1G

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

OFF CHARACTERISTICS

Peak Repetitive Forward Blocking Current (V _{DRM} = 200 V, R _{GK} = 1 kΩ)	T _C = 25°C	I _{DRM}	-	-	1.0	μA
	T _C = 125°C		-	-	100	μA
Peak Repetitive Reverse Blocking Current (V _{DRM} = 200 V, R _{GK} = 1 kΩ)	T _C = 25°C	I _{RDM}	-	-	1.0	μA
	T _C = 125°C		-	-	100	μA

ON CHARACTERISTICS

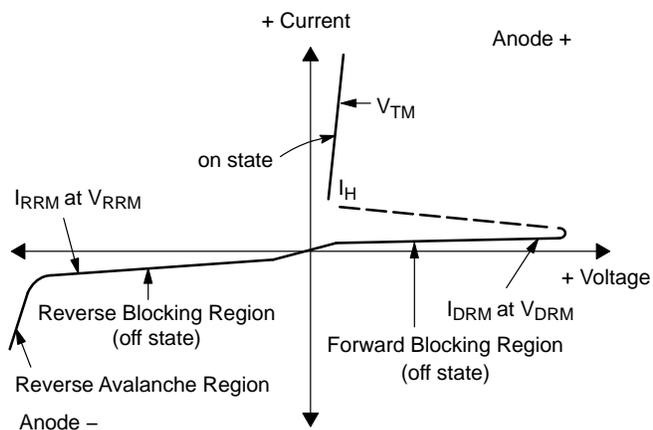
Peak Forward On-State Voltage (I _{TM} = 0.4 A, t _p < 1 ms, T _C = 25°C)	V _{TM}	-	-	1.7	V
Gate Trigger Current (V _D = 12 V, R _L = 100 Ω, T _C = 25°C)	I _{GT}	-	-	200	μA
Gate Trigger Voltage (V _D = 12 V, R _L = 100 Ω, T _C = 25°C)	V _{GT}	-	-	0.8	V
Holding Current (I _T = 50 mA, R _{GK} = 1 kΩ, T _C = 25°C)	I _H	-	-	6.0	mA
Gate Non-Trigger Voltage (V _D = V _{DRM} , R _L = 3.3 kΩ, T _C = 125°C)	V _{GD}	0.1	-	-	V
Latching Current (I _G = 1.0 mA, R _{GK} = 1 kΩ, T _C = 25°C)	I _L	-	-	7.0	mA
Gate Reverse Voltage (I _{RG} = 10 μA)	V _{RG}	8.0	-	-	V

DYNAMIC CHARACTERISTICS

Critical Rate of Rise of Off-State Voltage (R _{GK} = 1 kΩ, T _C = 125°C)	dv/dt	200	-	-	V/μs
Critical Rate of Rise of On-State Current (I _G = 2xI _{GT} 60 Hz, t _r < 100 ns, T _J = 125°C)	di/dt	-	-	50	A/μs

Voltage Current Characteristic of SCR

Symbol	Parameter
V _{DRM}	Peak Repetitive Off State Forward Voltage
I _{DRM}	Peak Forward Blocking Current
V _{RDM}	Peak Repetitive Off State Reverse Voltage
I _{RDM}	Peak Reverse Blocking Current
V _{TM}	Peak on State Voltage
I _H	Holding Current



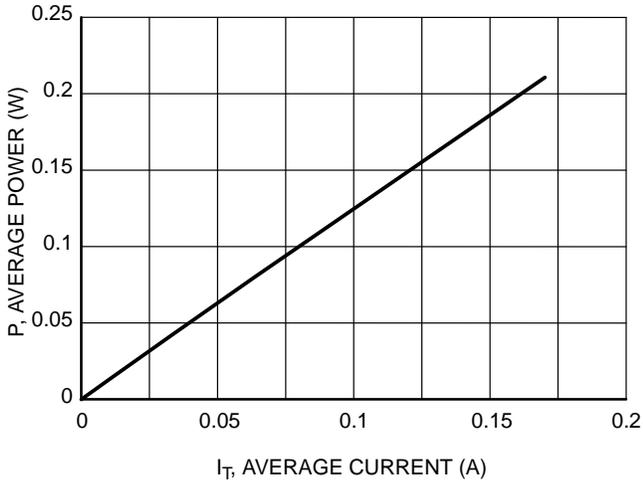


Figure 1. Maximum Average Power vs. Average Current

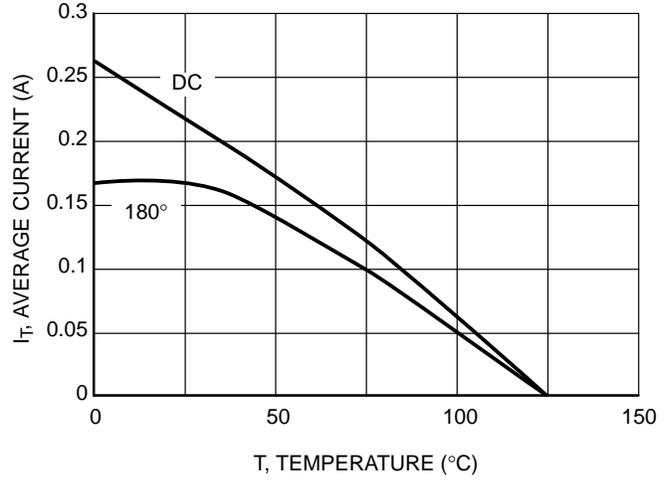


Figure 2. Current Derating

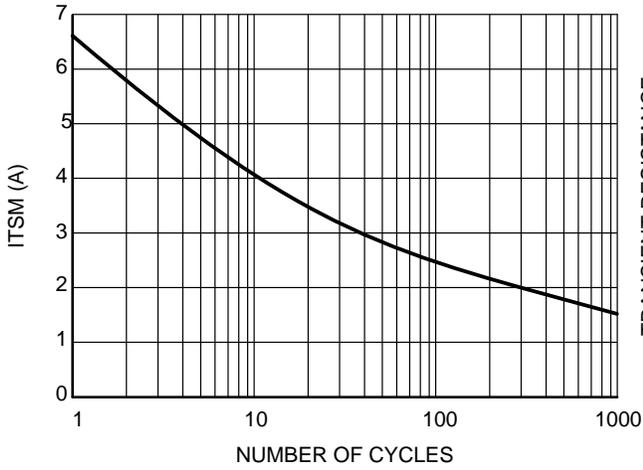


Figure 3. Surge Current ITSM vs. Number of Cycles

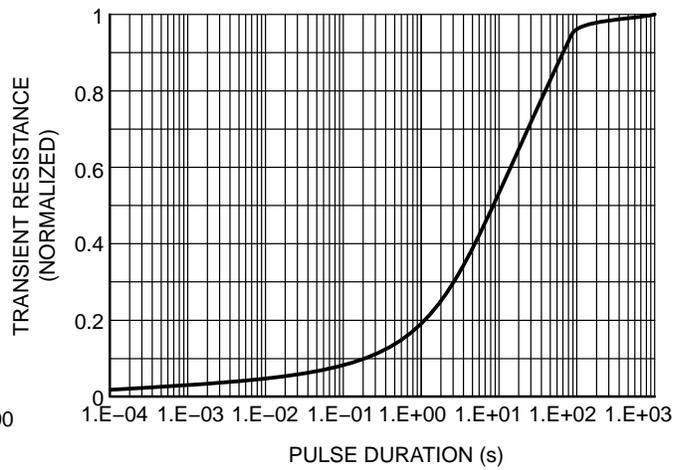


Figure 4. Thermal Response

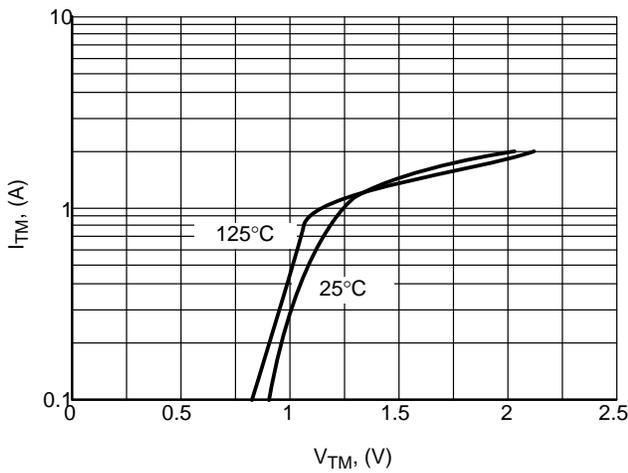


Figure 5. ON-State Characteristics

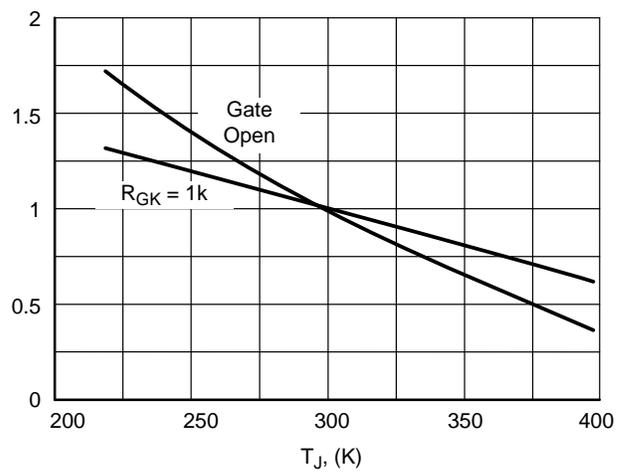
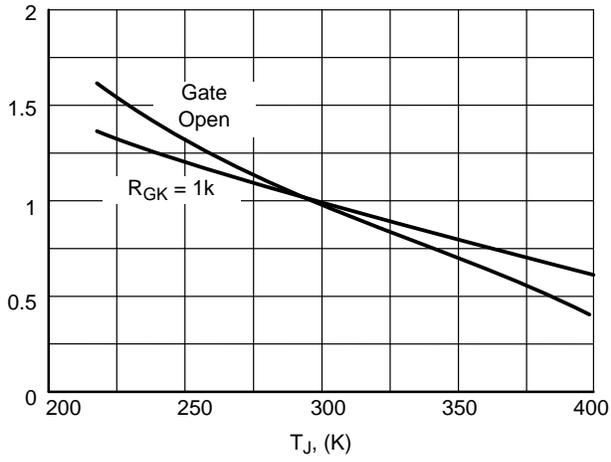


Figure 6. Gate Trigger Current vs. T_J (Normalized to 25°C)

NYC0102BLT1G



**Figure 7. Gate Trigger Current vs. T_J
(Normalized to 25°C)**

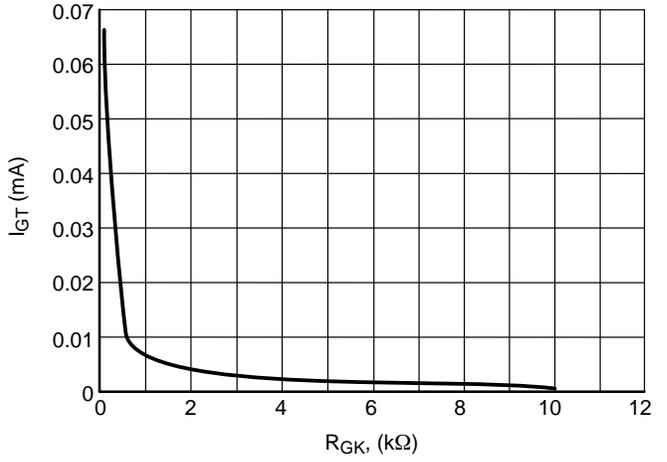


Figure 8. Gate Trigger Current vs. R_{GK}

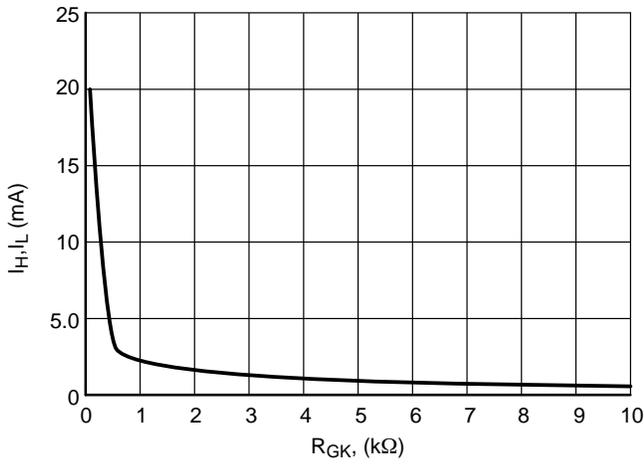


Figure 9. Holding and Latching Current vs. R_{GK}

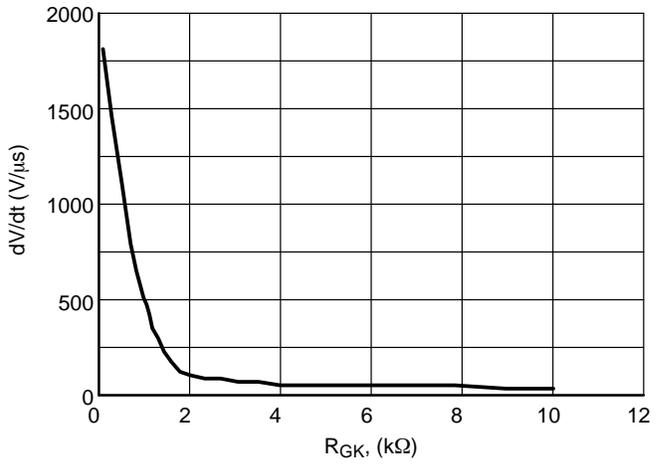


Figure 10. dV/dt vs. R_{GK}

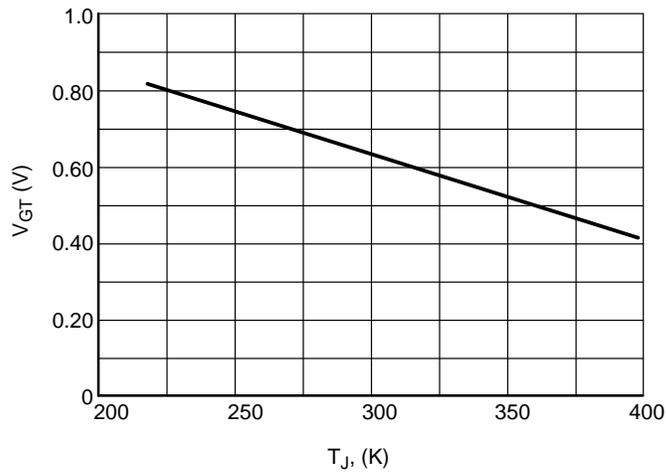
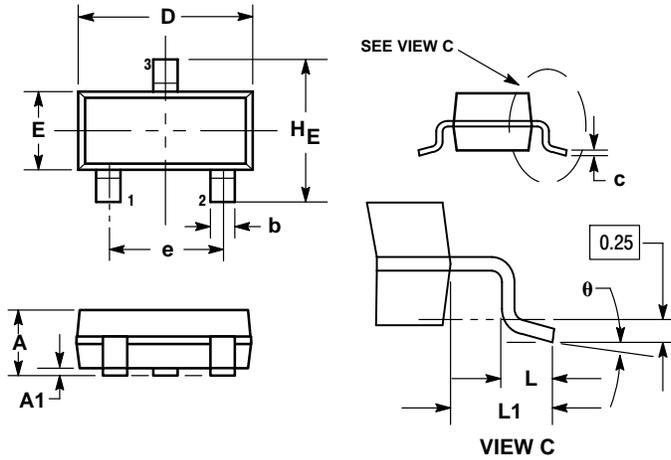


Figure 11. Gate Triggering Voltage vs. T_J

NYC0102BLT1G

PACKAGE DIMENSIONS

SOT-23 (TO-236)
CASE 318-08
ISSUE AP



NOTES:

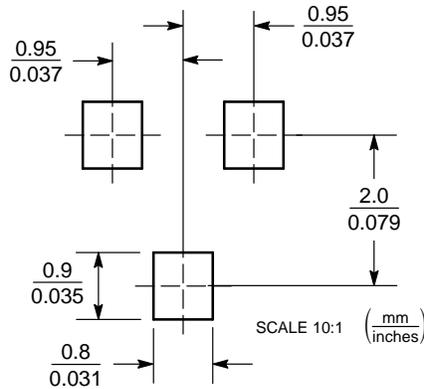
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.89	1.00	1.11	0.035	0.040	0.044
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.37	0.44	0.50	0.015	0.018	0.020
c	0.09	0.13	0.18	0.003	0.005	0.007
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.081
L	0.10	0.20	0.30	0.004	0.008	0.012
L1	0.35	0.54	0.69	0.014	0.021	0.029
HE	2.10	2.40	2.64	0.083	0.094	0.104
θ	0°	—	10°	0°	—	10°

STYLE 8:

1. ANODE
2. NO CONNECTION
3. CATHODE

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and the  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC) or its subsidiaries in the United States and/or other countries. SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com

Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative